Design And Implementation Of High Efficient And Performance Of Modified Adder Circuit Using 128 Bit CSLA And BEC Adder For Filter Design

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Abstract – Low Power VLSI is the major area in VLSI design to develop the product in smart way. High performance is the keystone of the designer's idea. Performance depends upon the speed, reduce-in-delay, less power consumption and majorly cost. In low power VLSI design, the contribution of adder is another platform. Design of an adder is to be more efficient and at the same time the internal parameters such as area, power, delay, cost to be monitor. Along with the benefits of super-fast performance the reduction of delay is a big advantage of using these types of adders. On the other hand, the formations of different inputs and to process those inputs are the difficult to implement. To overcome those difficulties, BEC based CSA are used. To process a complexity mathematical inputs like squaring of inputs some special circuit are to be use. Such a special circuit is the SQRT and along with CSLA it is called as SQRT-CSLA. Discussion is taken place how to implement the SQRT-CSLA to analysis the practical values. ASIC, SOC implementation is most popular in this type of implementation. In an existing methodology, it was analysed that the synthesis by ASIC results BEC-based SQRT-CSLA design involves 48% more ADP and consumes 50% more energy than the proposed SQRT-CSLA, on average, for different bit-widths. We are focusing on this point, how to maximize the efficiency by utilize the power less and maximum result in the output. Also, in an existing system the implementation is going with 64 bit widths as maximum and this clearly describes the factor how increase of the product efficiency took place. But in our proposed methodology, we are going to adopt the processing bits of the range 128 bits.

Keywords – Carry Select Adder, Binary to Excess Code, Area-Delay-Product.

I. INTRODUCTION

The rapid development of science and technology offers various benefits to enjoy an unlimited and uninterrupted application to us. But the common factor is to maintain the internal parameters as a significant one. Design of VLSI circuit's with low power, significant area, less delay etc. are some of the challenging tasks. It is also a notable point in our research. Coming to this paper, design of an Adder circuit with high efficient and performance when compared with Existing Adder circuits. When the words high efficient and performance took place, there is no doubt that the concept is developing of low power, less area and delay time. But to design and implement an adder is a key significant role. The adder circuit is to process the addition of binary numbers. The methodology adopts the technique of CSLA and BEC adder. For this purpose several adder circuits is to be create. Such types of adder circuits are Carry Select Adder, Carry Skip Adder and Carry Save Adder (3 CSA). On the other hand, the formations of different inputs and to process those inputs are the difficult

to implement. To overcome those difficulties, BEC based CSA are used. SQRT-CSLA brings nearly less area - delay product (ADP) than the BEC-based SQRT-CSLA.

II. CONCEPTS IN DESIGNING ADDER CIRCUIT

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research to perform arithmetic operations in VLSI design there is a scope for reducing area and delay. There is a scope of CSLA in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The circuit architecture is simple and area-efficient. However, the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready. On the other hand, Carry Look-ahead Adders (CSLAs) are the fastest adders, but they are the worst from the area point of view. Carry Select Adders have been considered as a compromise solution between RCAs and CSLAs because they offer a good tradeoff between the compact area of RCAs and the short delay of CSLAs. Reduced area and high speed data

path logic systems are the main areas of research in VLSI system design. High speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. There are many types of adder designs available (Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Skip Adder) which have its own advantages and disadvantages. The major speed limitation in any adder is in the production of carries and many authors considered the addition problem. To solve the carry propagation delay CSLA is developed which drastically reduces the area and delay to a great extent. The CSLA is used in many computational systems design to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. It uses independent ripple carry adders (for Cin=0 and Cin=1) to generate the resultant sum. However, the Regular CSLA is not area and speed efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input. The final sum and carry are selected by the multiplexers (mux). Due to the use of two independent RCA the area will increase which leads an increase in delay. To overcome the above problem, the basic idea of the proposed work is to use n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. This logic can be replaced in RCA for Cin=1 to further improves the speed and thus reduces the delay. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA will achieve lower area, delay which speeds up the addition operation. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure because the number of gates used will be decreased.

III. 16 BIT SQRT CSLA

CSLA compromises between ripple carry adder and carry look ahead adder. When compared to RCA CSLA is high speed and when compared to carry look ahead adder hardware complexity less. The main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. It is divided into five groups with different bit size RCA. From the structure of CSLA, it is evident that there is scope for reducing area, power and delay in CSLA. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer.

Like the CSA, this idea may be applied iteratively to achieve faster adders. Assume the bits of an *n*-bit adder are partitioned into *m* groups, where *m*=1 corresponds to the group containing the lease significant bits. P_i denotes the number of bits in group *i*. Using the assumptions made in the previous section, we first try to balance all critical paths from the inputs of the adders to *Cout*. Note that the first adder performs addition only once, while all other adders do it twice.
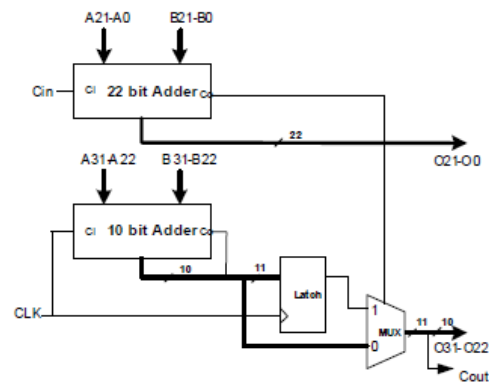
IV. MODIFIED CSLA USING BEC

Fig. 1 Architecture of CSLA

In this architecture, (transparent) latches are used to save the result of addition when C_{in} of the 10-bit (MSB) RCA is one. When the clock transitions to low, the 10-bit adder calculates the result of 10-bit addition for the case C_{in} is zero. Therefore, at the end of the clock cycle, the result of the addition of the 10 MSBs is available for both cases of the carry-in signal. Next, based on the actual value of the carry calculated by the LSB adder, a MUX selects the appropriate value, either from the output of the latch or the output of the adder. This value will be the result of the 32-bit addition. Referring the same figure, notice that the inputs of the adder are partitioned into two parts, one adding the first 22 bits (the LSB adder), while the other adds the last 10 bits (the MSB adder.) Note that the LSB adder has nearly twice as many bits as the MSB adder. Therefore, the MSB adder can calculate the sum of 10 high bits twice when the LSB adder calculates the addition of the lower 22 bits. This reduces the delay of adding 32 bits by a factor of 1/3 compared to RCA.
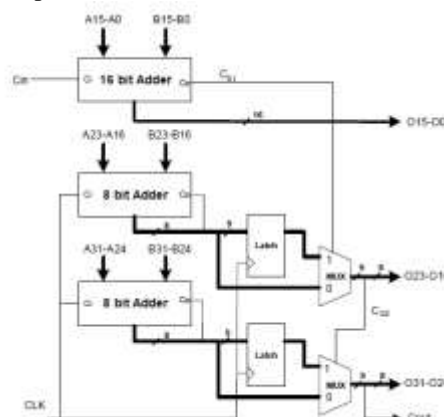

Fig. 2 Architecture of CSLA with m=3

As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n + 1-bit BEC is required. The Binary to excess one Converter (BEC) replaces the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSLA. The modified16-bit CSLA using BEC is shown in Fig.3. The structure is again divided into five groups with different bit size RCA and BEC.

One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Comparing the group 2 to 5

of both regular and modified CSLA, it is clear that BEC structure reduces the area and power.
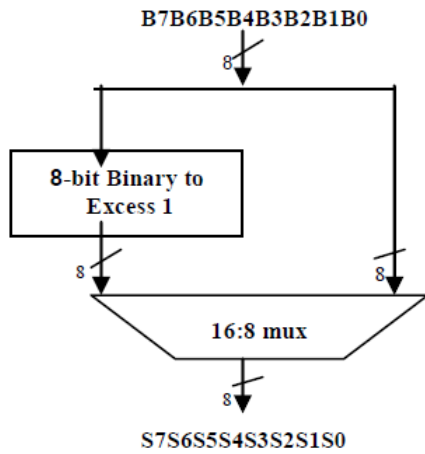

Fig. 3 8 bit BEC with 16:8 Mux

One input of the 16:8 mux gets as it input and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin.

The Boolean expression of 8-bit BEC is

$X0 = \sim B0$

$X1 = B0 \wedge B1$

$X2 = B2 \wedge (B0 \& B1)$

$X3 = B3 \wedge (B0 \& B1 \& B2)$

$X4 = B4 \wedge (B0 \& B1 \& B2 \& B3)$

$X5 = B5 \wedge (B0 \& B1 \& B2 \& B3 \& B4)$.

$X6 = B6 \wedge (B0 \& B1 \& B2 \& B3 \& B4 \& B5)$.

$X7 = B \wedge (B0 \& B1 \& B2 \& B3 \& B4 \& B5 \& B6)$.

B [5:0]	X [5:0]
000000	000001
000001	000010
000010	000011
…………..	……………
111111	000000

Table 1

V.   MODIFIED CSLA USING 128 bit BEC

In this method CSLA with cin=1 and multiplexer is replaced by the simple combinational circuit which consists of XOR and AND gates. By using this method area and power is reduced when compared to regular CSLA and modified CSAL(BEC). The modified 16-bit CSLA without using mux is shown in fig.7 REF[5]. The structure is again divided into five groups with different bit size RCA and Combinational.

Initially RCA structure is calculate for cin =0 the output of full adder is given to the combinational circuit and one of the input of that combinational circuit is previous stage carry then it will provide the proper output by using XOR and AND gates structure. The group 2to 5 of the modified 16-bit CSLA is shown Fig. 8.Comparing the group 2 to 5 of regular, modified BEC and without MUX CSLA. So, in this method, our statement is there is a chance to reduce the power and delay.
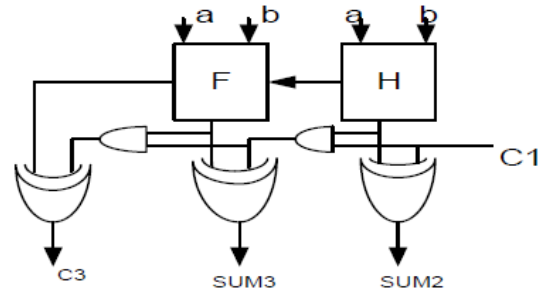

Fig 4 Modified CSLA without MUX

A 16-bit carry select adder can be developed in two different sizes namely uniform block size and variable block size. Similarly a 32, 64 and 128-bit can also be developed in two modes of different block sizes. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least significant bit to the most-significant bit. The various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry adders. The speed of a carry-select adder can be highly efficient.
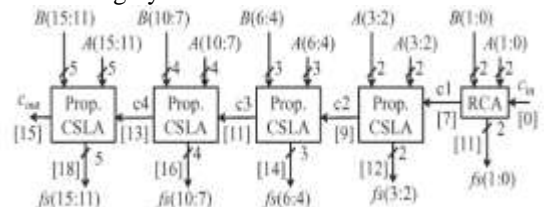

Fig. 5 16 Bit SQRT Structure

The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 8-bit BEC is listed improved up to 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay.

The structure of the 128-b regular SQRT CSLA is shown in Fig. 6. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig.6, in which the numerals within specify the delay values, e.g., sum2 requires 10 gate delays.

This architecture is similar to regular 64-bit SQRT CSLA, the only change is that, we replace RCA with Cin=1 among the two available RCAs in a group with a BEC. This BEC has a feature that it can perform the similar operation as that of the replaced RCA with Cin=1. Fig 7 shows the Modified block diagram of 64-bit SQRT CSLA. The number of bits required for BEC logic is 1 bit more than the RCA bits. The modified block diagram is also divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding mux. As shown in the Fig.7, Group 0 contain one RCA only which is having input of lower significant bit and carry in bit and produces result of sum[1:0] and carry out which is acting as mux selection line for the next group, similarly the procedure continues for higher groups but they includes BEC logic instead of RCA with Cin=1.Based on the consideration of delay values, the arrival.
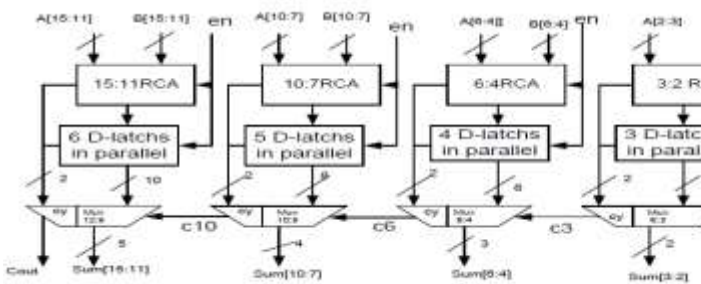
Fig. 6 128 Bit CSLA and BEC adder for filter design

VI. SIMULATION RESULTS

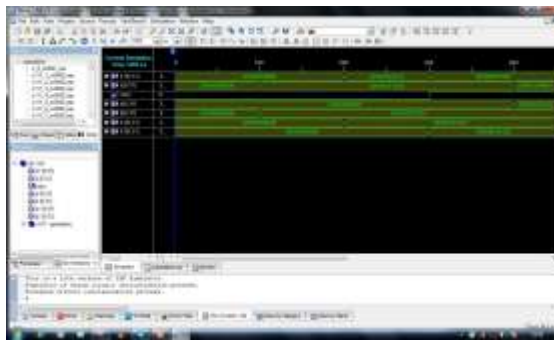The simulation results shown about the performance of the
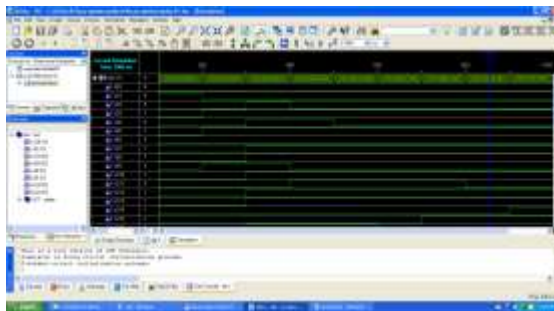

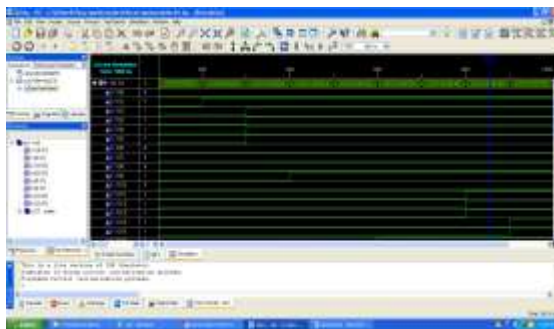**Fig. 7 (a) Input parameters**

Fig. 7 (b) Testbench waveform

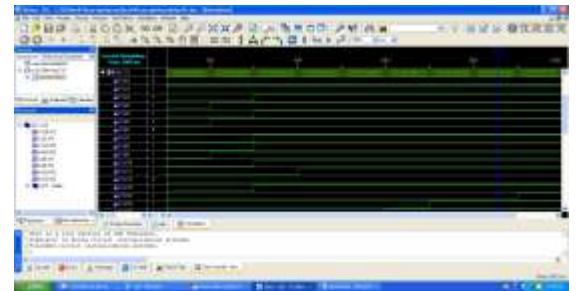**Fig. 7 (c) Testbench for selected CSLA set**

Fig. 7 (d) Output Testbench waveform

VII. CONCLUSION

The multipath carry propagation feature of the CSLA is fully exploited in the SQRT-CSLA, which is composed of a chain of CSLAs. CSLAs of increasing size are used in the SQRT-CSLA to extract the maximum concurrence in the carry propagation path. Using the SQRT-CSLA design, large-size adders are implemented with significantly less delay than a single-stage CSLA of same size. However, carry propagation delay between the CSLA stages of SQRT-CSLA is critical for the overall adder delay. Due to early generation of output-carry with multipath carry propagation feature, the proposed CSLA design is more favorable than the existing CSLA designs for area–delay efficient implementation of SQRT-CSLA. The cascaded configuration of (2-bit RCA and 2-, 3-, 4-, 6-, 7-, and 8-bit CSLAs) and (2-bit RCA and 2-, 3-, 4-, 6-, 7-, 8-, 9-, 11-and 12-bit CSLAs) respectively, for the 32-bit SQRT CSLA and the 64-bit SQRT-CSLA to optimize adder delay.

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