

# A Reduced Switch Count Dual Output Single Phase Inverter

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**Abstract-** Dual-output three-switch inverter topology is proposed in this paper. To supplying two single-phase ac loads independently with one inverter. Using reduced switch count topology which introduced in three phase converter. This configuration required less no of devices and provide dual output compared to conventional inverters. Which results in reduction in cost, size and switching losses. The proposed topology is introduced with its gate circuit for switching schemes is elaborated. Simulation model of proposed inverter is developed. Its output waveforms are analyzed. Total harmonic distortion and performances are compared with different PWM techniques.

**Key words-** Reduced switch count inverter, three-switch inverter legs.

## I. INTRODUCTION

Power Electronics is the viable solution to control the power and got more and more importance during the years due to the benefits they brought into electrical engineering fields. There are lots of advantages which Power Electronics brought, but the most meaningful is the possibility to control electrical machine and to manage the flows of electromagnetic power. Due to Power Electronics it was possible to build drives, active filters, static Var compensators, etc. In present trends the approach to fulfilling the demand for independently supplying a number of ac loads in several applications is using separate inverters for each of them. But, this may result in undesirable increase in system cost, size and weight.

Dual-terminal converters gives the researches freedom in realizing switch reduction of power converters resulting in system cost, size and weight.

A reduced number of power switches constitutes an important topic in power electronics these objectives could be achieved by reducing the number of active switches in power inverters. The resultant configurations are called reduced switch count inverters.

Dual output reduced switch count topologies has wide application in ac/ac converters(regulating voltage) [1-7].

Eight switches inverter introduced concept of replacing a leg with split capacitor and sharing it between two converters[1], to achieve reduced switch count.

Further this idea the idea of replacing a switch leg with a split-capacitor-leg and sharing it between the two stages of power conversion was implemented in many configuration to get reduced switch count concept.[4]. some topologies in

which there is no split-capacitor leg and switch reduction is realized by simply sharing a switch-leg are proposed in [2]. In bulk ac drives system Sharing a switch-leg is discussed in [8]. Three switch leg structure with nine switches [10] having dual output for two three phase loads is introduced. in which switch reduction is achieved by sharing switches between upper and lower part. Many researches has been done in this nine switch inverter and reduced switch count topology of this inverter called three phase dual output six switch inverter[15].

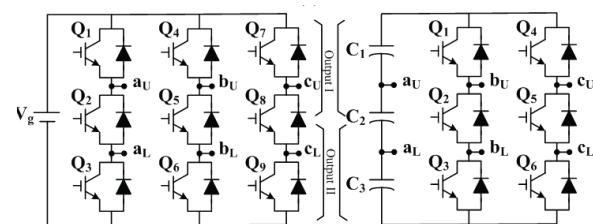


Fig 1. nine-switch inverter, three-phase six-switch inverter

Nine switch three phase inverter implemented by replacing a switch leg with series capacitor to get reduced switch count with dual output.[16]

It observed that implementing nine-switch inverter idea for utilization of three-switch inverter legs compared to the conventional two-switch inverter legs is a resolution in the direction for switch reduction in inverter topologies developed to supply two independent ac loads applications. This concept is modified in this paper for single-phase inverters,

To independently supply two single-phase loads in comparison with two full bridge inverters. Furthermore, dual-output single-leg inverter is developed by replacing a

leg of semiconductor switches with a series of capacitors, (Fig.2).

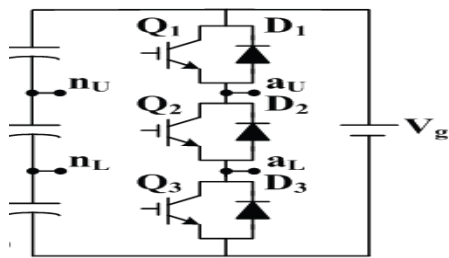


Fig 2. Proposed dual output inverter

This paper is divided in following sections. The proposed reduced switch count dual output inverter and PWM scheme for gate pulse triggering used in the structure is explained. The structure of Reduced switch inverter is presented and analysis of inverter output waveforms. The results of dual output inverter are displayed and discussed. Total harmonic distortion in different PWM scheme are compared.

Last section dedicated to conclusion.

II THREE-SWITCH INVERTER TOPOLOGY

The proposed reduced-switch inverter is actually developed by replacing a leg of the six-switch inverter with a series combination of capacitors at the cost of losing zero output voltage state so as to further economize the inverter cost by reducing the number of power switches. The single-leg topology which uses only three semiconductor switches for independently supplying two single phase loads is structurally comparable to two half-bridge inverters with a common row of switch and capacitor (middle row of the proposed structure). The output voltages of the three-switch inverter can be expressed as  $V_{ox} = (1/2)MxV_g\sin(\omega Xt+\phi X)$ , where x denotes upper or lower output similar to single phase half bridge inverter except that the modulation indices, M, frequencies,  $\omega$ , and phase difference,  $\phi$  of the output references face some .

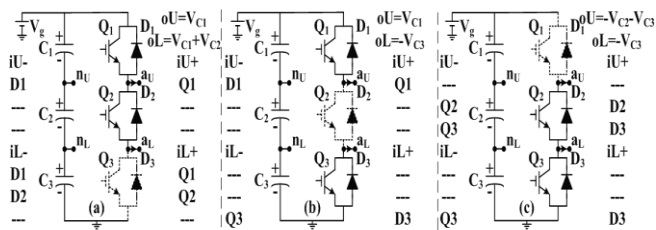


Fig 3. Switching states of proposed inverter

A. SWITCHING STATES

Three-switching states of Fig. 3 are possible for the three switch inverter. As illustrates in fig, there is no zero state for any of the inverter outputs . Furthermore, the low level of an output voltage may not be negative of its high level and voltage levels of the upper and lower outputs may not be equal depending on the capacitor voltage levels. When the lower switch is OFF , both outputs are positive, when the upper switch is OFF, both outputs are negative and when the middle switch is OFF, the upper output is positive and the lower output is negative.

Switching States	Q1	Q2	Q3
S1	OFF	ON	ON
S2	ON	OFF	ON
S3	ON	ON	OFF

Fig 4. Switching states for proposed inverter.

B. PULSE WIDTH MODULATION SCHEME FOR GATE SIGNAL GENERATION

The triggering for gate of semiconductor used in inverter is provided by generating a logic for pulses provided. By keeping in mind the required on-off position of devices as in (Fig 4). Sinusoidal pulse width modulation scheme is provided for gate triggering. The other two PWM schemes which developed for firing circuit are single pulse width modulation and double pulse width modulation.

The logic generated by using relation operator as following fig 5.

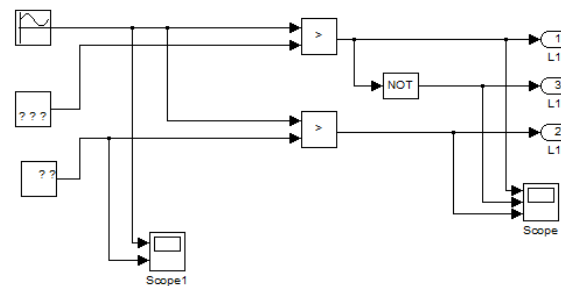


Fig 5.(a) Gate signal generation logic of three switch inverter

At a time two ports are on to provide gate pulse for two switches so that by applying this scheme at a time there is no zero state for any of the inverter outputs.

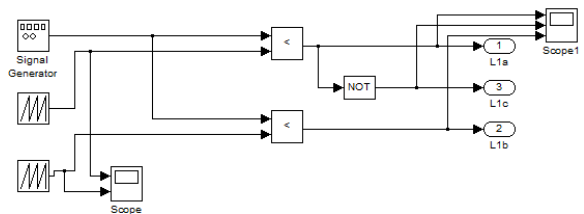
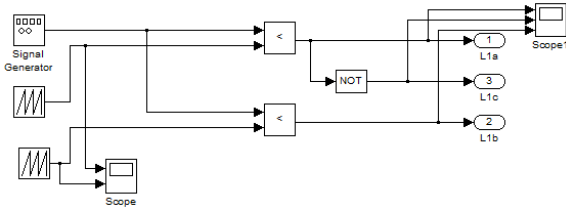


Fig 5 (b) Gate signal generation using SPWM



5 (c) Gate signal generation using DPWM

### C . ESTIMATION OF DC LINK VOLTAGE

In this part voltage sharing on dc-link capacitors is Discussed and it is shown that the offsets which added to the references determine the actual capacitors voltage levels. Dc-link voltages are estimated by replacing the switches with dependent voltage sources controlled by gate command signals. The equivalent circuit is depicted in Fig. 6. It is assumed that the natural time constants of the converter network are much longer than the switching period

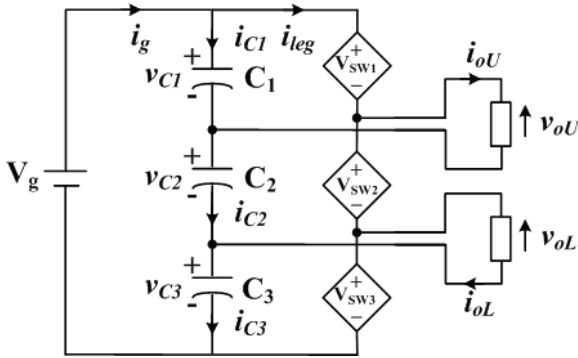


Fig 6. Circuit for voltage of dc link capacitor.

Voltage appear across each capacitor, As stated by equation dc voltage sharing on capacitors is not related to their size

$$V_{C1} = \langle \overline{V_{SW1}} \rangle = V_g (1 - \text{offset}_U) / 2$$

$$V_{C2} = \langle \overline{V_{SW2}} \rangle = V_g (\text{offset}_U - \text{offset}_L) / 2$$

$$V_{C3} = \langle \overline{V_{SW3}} \rangle = V_g (1 + \text{offset}_L) / 2$$

However, in following equation conclude that , the ac voltage component across the capacitors, i.e. voltage ripple, which depends on the size of capacitors, should be negligible.

$$v_{oU} = - \langle \tilde{V}_{SW1} \rangle = M_U V_g \sin(\omega_U t + \phi_U) / 2$$

$$v_{oL} = \langle \tilde{V}_{SW3} \rangle = M_L V_g \sin(\omega_L t + \phi_L) / 2$$

### III. STUDY OF PROPOSED INVERTER

In this section to reduce the semiconductor switches “Reduced switch count” theory is used to minimize the switching devices and switching losses Fig(2). study of simulink model with three switches by replacing a leg with

series of split capacitors of proposed dual output inverter is discussed. The simulated model of inverter (fig.7)

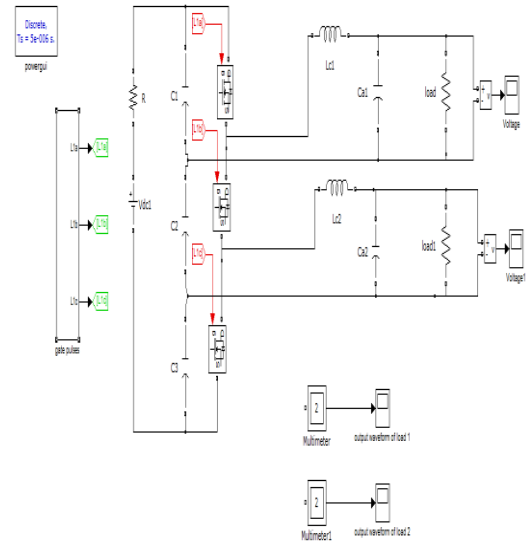


Fig 7. Simulink model of proposed inverter

The output waveforms if inverter is analyzed its THD for load of 100 ohms is analyzed. Three mosfet with gate triggering logics as explained before, are connected in one leg and three split phase capacitors connected in one leg. System is supplied by 100volts dc at 50 Hz frequency. Output voltage and current is measured . two load one for upper and one for lower side is used . both of same value i.e. 100 ohms are used. L-C filter used to remove ripple and smoothening and minimized total harmonic distortion.

Total harmonic distortion (THD) is analyzed and compared it with single pulse width modulation and double pulse width modulation.. It can be observed that for same frequency THD of proposed inverter is less than that of SPWM and DPWM

### IV. EXPERIMENTAL RESULTS

The results of proposed inverter topology are presented in this section. Its output waveforms total harmonic distortion are displayed and analyzed.

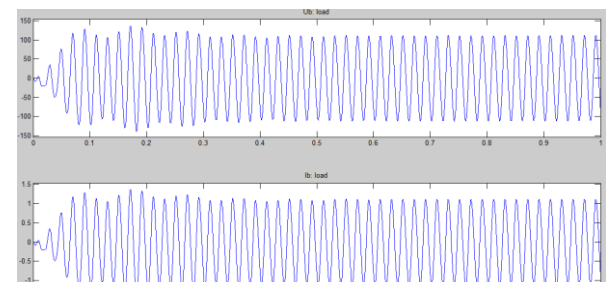


Fig 8. Output voltage and current of upper load

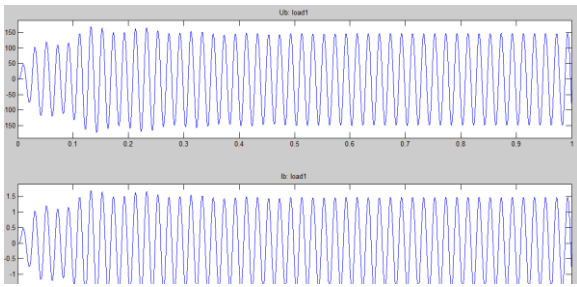


Fig 9. Output voltage and current of lower load

The output waveforms as if figs shows ac output of voltage and current corresponding to upper and lower loads.

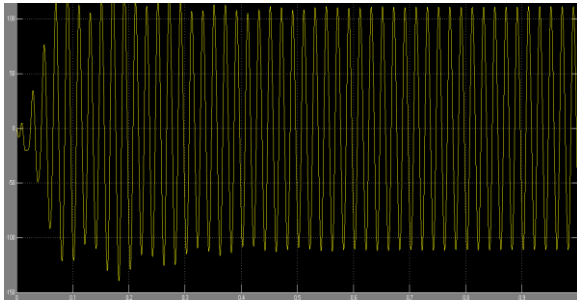


Fig 10. Output voltage of upper load

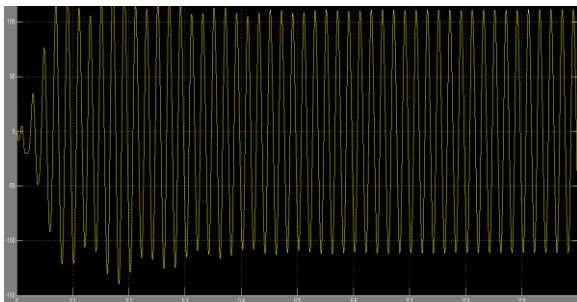


Fig 11. Output voltage of lower load

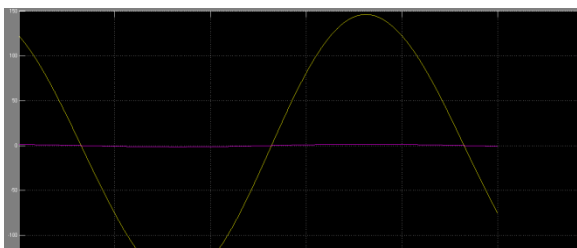


Fig 12. Output of proposed inverter

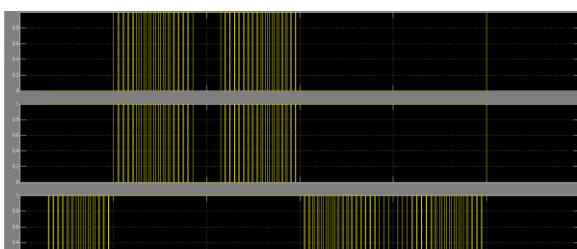


Fig 13 (a) Generated gate signal using sinusoidal PWM

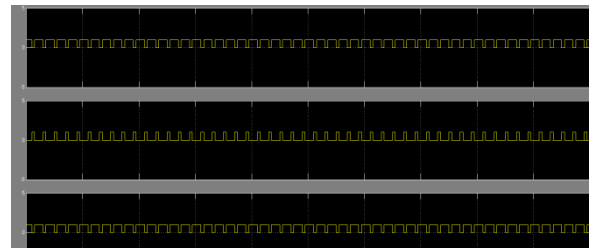


Fig 13 (b) Generated gate signal using single PWM

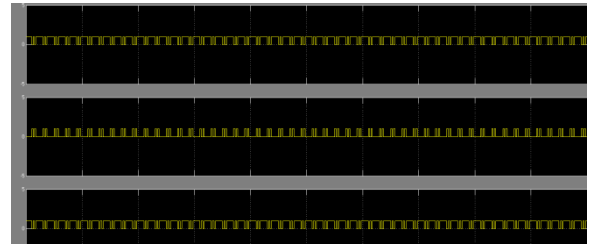


Fig 13 (c) Generated gate signal using double PWM

#### A. COMPARATIVE STUDY OF THDs IN DIFFERENT PWM SCHEMES

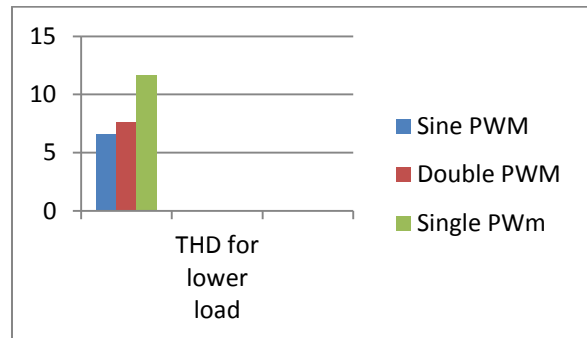


Fig. 14(a) THDs for  $V_{out}$  for lower load

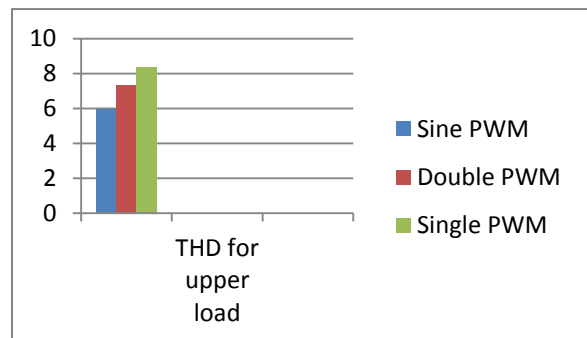


Fig. 14(a) THDs for  $V_{out}$  for upper load

## V. CONCLUSION

A reduced switch count dual-output inverter named “reduced switch count dual output single phase inverter” and its PWM scheme was proposed in this paper. The proposed inverter topology was introduced; its gate triggering scheme was developed; and output voltage and current waveforms analysis was carried out along with the total harmonic distortion.

compare the THDs of proposed inverter in different PWM schemes and observed that in sinusoidal PWM scheme THD is less than the other PWM schemes. Advantages of the proposed three switch inverter are

- The number of switches and hence drive circuits is reduced.
- Reliability
- Low switching losses
- Small size and weight

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