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Analysis of Three Level Diode Clamped Multilevel Fed Induction Motor Drive

Sadhana pandey, Sulochana Wadhwani, Praveen Bansal

[1]Electrical Engineering Department
Madhya Institute of Technology and Science
Gwalior, India
Sadhana.pandey13@gmail.com

[2]Electrical Engineering Department
Madhya Institute of Technology and Science
Gwalior, India

[3]Electrical Engineering Department
Madhya Institute of Technology and Science
Gwalior, India
pbansal444@gmail.com

Abstract- ***A multilevel inverter is a power electronic device that is widely applied in industries for high voltage and high power applications, with the added remuneration of low switching stress and lower total harmonic distortion (THD), hence dropping the size and volume of the passive filters. Multilevel inverter machinery has emerged recently as a very important alternative in the area of high power medium-voltage control and also for improving the total harmonic distortion by reducing the harmonics. Generally, the poor quality of voltage and current of a conventional inverter fed induction machine is obtained due to the presence of harmonics and hence there is a significant level of energy losses. The objective of this paper is to obtain a 3-level output, which is acquire by a three phase three level diode clamped multilevel inverter (MLI) fed induction motor drive. This paper presents the simulation result and implementation of three phase three level multilevel inverter (MLI) fed induction motor Drive.***

Keywords-Multilevel inverter, PWM Techniques, Total Harmonic Distortion, Diode Clamped Multilevel Inverter (DCMLI)

1. Introduction

Majority of industrial drives use ac induction motor because these motors are rugged, reliable, and relatively and expensive. Induction motors are mainly used for constant speed applications because of unavailability of the variable frequency supply voltage But many applications need variable speed operations Industrial applications have begun to require higher power apparatus in topical years. Some medium voltage motor drives and utility applications require medium voltage[1]. For a medium voltage grid, it is difficult to connect only one power semiconductor switch directly. As a outcome, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. The perception of multilevel converters has been introduced since 1975[2]. The main advantages of multilevel inverters include the increase of power, the diminution of voltage stress on the power switching devices, and the generation of high quality production voltages[3][4-8]. Multilevel converters are mainly utilized to synthesis a desired single or three-phase voltage waveform. The desired multi-staircase .The importance of multilevel inverters has been increased since last few decades. These new types of inverters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum and with less THD. Plentiful techniques have been introduced and widely studied for utility of non conventional sources and also for drive applications. e output voltage is obtained by combining several dc voltage sources[9].

An inverter convert DC power into AC power through waves called either sine waves or modified sine waves. a multilevel(MLI) uses a sequence of semiconductor power converters(usually two or three) thus generating higher voltage. While an inverter would have to flip several switches. An inverter is a device which receives dc supply for its input and produces ac output. A multilevel inverter is a more powerful inverter, in higher and medium voltage grid it is trouble to connect only one semiconductor switch directly, As a result multilevel inverter was introduced. A multilevel inverter is a power electronic device that is widely used in industries for high voltage and high power applications, with output harmonic content is reduced by using multilevel inverter (MLI)) One important application of multilevel converters is focused on medium and high-power conversion. Nowadays, there exist three commercial topologies of multilevel voltage-source inverters: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs)[2]. Among these inverter topologies, diode multilevel inverter(MLI) reaches the higher output voltage and power levels and the higher reliability due to its modular topology[9][12][11]. Diode clamped inverter is the most commonly used multilevel topology , in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Nabae, Takahashi, and Akagi were proposed neutral point converter in 1981 it was essentially a three-level diode-clamped inverter [13].

2. Different Topology Of Multilevel Inverter

2.1 Cascaded H-bridge multilevel Inverter

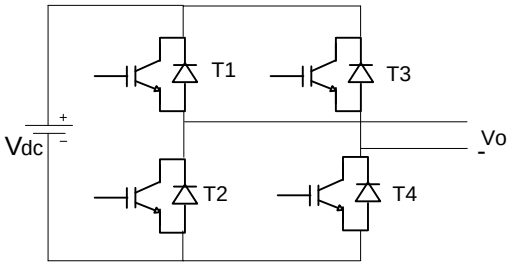

Figure1 Cascaded H-bridge multilevel inverter circuit topology for 3- level inverter.

One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. The series H-bridge inverter appeared in 1975[8].Cascaded multilevel inverter was not fully realized until two researchers, Lai and Peng. They patented it and accessible its various advantages in 1997. Since then, the CMI has been used in a wide range of applications.

The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By accumulation more H-bridge converters, the quantity of Var can simply amplified exclusive of redesign the power stage, and build-in severance against entity H-bridge converter failure can be realized. With its modularity and elasticity, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. A series of single-phase full bridges makes up a phase for the inverter. A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing. The converter topology is based on the series connection of single-phase inverters with separate dc sources. Figure 1 shows the power circuit for three-level cascaded inverter and it requires four semiconductor switches, one dc sources of fixed values.

2.2 Flying Capacitor Multilevel Inverter

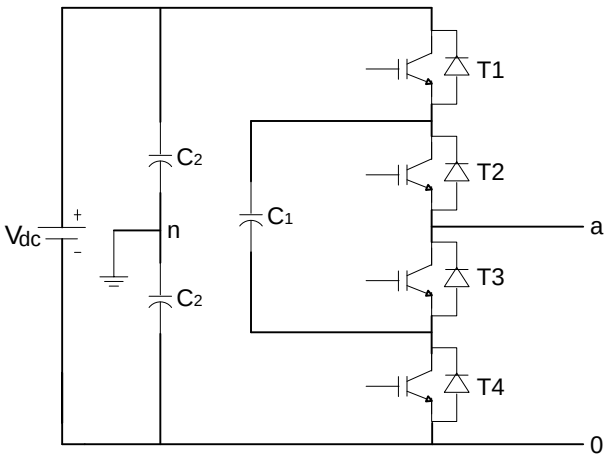

Figure2 Flying Capacitor multilevel inverter circuit topology for 3- level inverter

The capacitor clamped inverter alternatively known as flying capacitor was proposed by Meynard and Foch in 1992. The structure of this inverter is similar to that of the diode-clamped inverter. This is one of the alternative topology for the diode clamped inverter. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed except that instead of using clamping diodes, the inverter uses capacitors in their place. Figure 2 shows the three-level flying capacitor inverter. The charge of the capacitor can be balanced by proper selection of the zero states. In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states, which make up the level V3. The voltage synthesis in a three-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Furthermore, the flying capacitor inverter has switching redundancy within the phase, which can be used to balance the flying capacitors so that only one dc source is needed.

3. Proposed Topology

In this topology there are two pairs of switches and two diodes are consists in a three-level diode clamped inverter. All switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. The DC bus voltage is dividing into three voltage levels with the help of two series connections of DC capacitors, C1 and C2. With the help of the clamping diodes Dc1 and Dc2 the voltage stress across each switching device is partial to Vdc. It is supposed that the total dc link voltage is Vdc and mid point is synchronized at half of the dc link voltage, the voltage across each capacitor is Vdc/2 (Vc1=Vc2=Vdc/2). In a three level diode clamped inverter, there are three different feasible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. At any time a set of two switches is on for a three- level inverter. Fig.3. shows the three level diode clamped multilevel inverter (MLI).

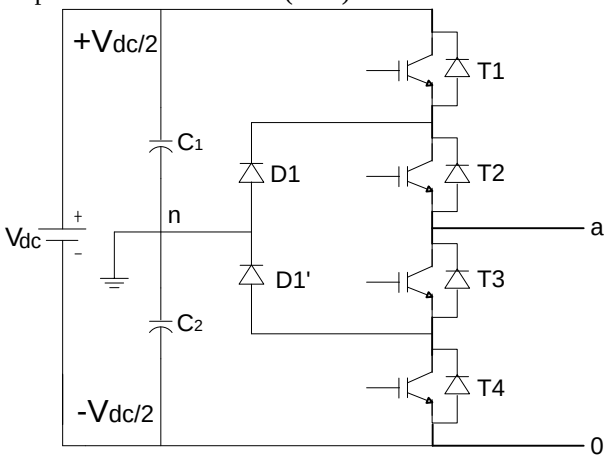

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Figure3 Diode clamped multilevel inverter circuit topology for 3-level inverter

Table.1 shows the switching states in one leg of the three-level DIODE CLAMPED INVERTER. In a three level diode clamped inverter, there are three different feasible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. At any time a set of two switches is on for a three-level inverter.

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TABLE1: Switching States In One Leg Of The Three-Level Diode Clamped Inverter

Switch State	*State*	*Pole Voltage*
T1=ON,T 2=ON T3=OFF,T 4=OFF	S=+ve	Vao=Vdc/2
T1=OFF,T 2=ON T3=ON,T 4=ON	S=0	Vao=0
T1=OFF,T2=OFF T3=ON,T 4=ON	S=-ve	Vao=-Vdc/2

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. The so-called "multilevel" starts from three levels. A three-level inverter, also known as a "neutral-clamped" inverter, consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three-level inverter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The output obtained from a three-level inverter is a quasi-square wave output if fundamental frequency switching is used. Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load.

The phase a output voltage Van has three states: Vdc/2, 0, -Vdc/2. The gate signals for the chosen three level DCMLI are developed using MATLAB-SIMULINK. The order of numbering of the switches for phase a is T1, T2, T3 and T4 and likewise for other two phases. The DC bus consists of four capacitors C1 and C2, acting as voltage divider.

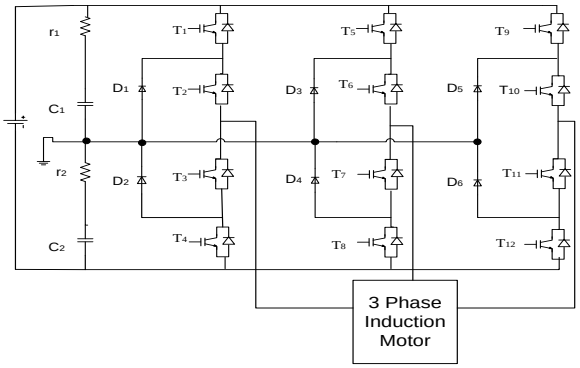

Figure 4 Diode clamped multilevel inverter circuit topology for 3-phase 3-level inverter fed induction motor drive

4. Modulation Techniques

Multilevel converters are mainly controlled with sinusoidal PWM extended to multiple carrier arrangements of two types: Level Shifted (LS-PWM), which includes Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM) and Alternative Phase Opposition Disposition (APOD-PWM) or they can be Phase Shifted (PS-PWM). In propose topology POD is used. Figure 5 shows the multilevel converter modulation methods.

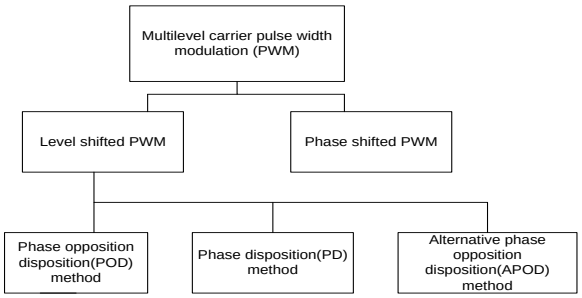

Figure 5 Block Diagram of Multicarrier Pulse Width Modulation

4.1 Level Shifted PWM (LSPWM)

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. LSPWM leads to less distorted line voltages since all the carriers are in phase compared to PSPWM.

4.1.1 Phase disposition (PD) technique

With the wide application in multi -level inverters, this technique has all carriers in phase. It requires four carrier waveforms. The zero reference is placed in the middle of the carrier sets.

4.1.2 Alternative phase opposition disposition (APOD) technique:

This technique requires four carrier waveforms, which are phase-displaced by 180^0 alternate.

4.1.3 Phase opposition disposition (POD) technique

This technique requires four carrier waveforms that are all in phase above or below the zero reference value. However, they are phase shifted by180o between the carrier waveforms above and below zero.

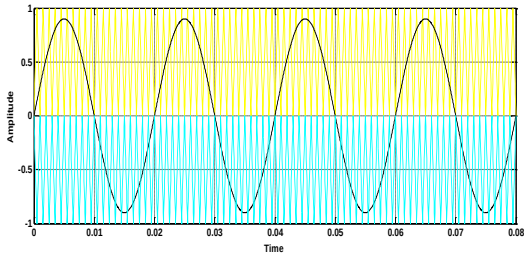

Figure 6 LS-PWM carrier arrangements: (b) POD

5. Simulation Results

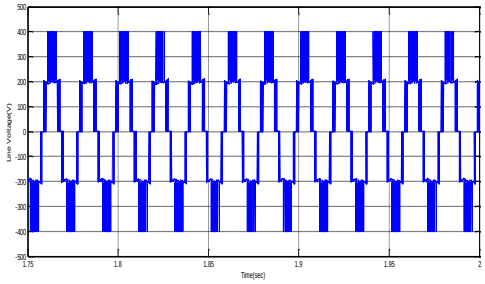

Figure 7 Output line voltage waveform V_{LL} for 3-level of DCMLI using PODPWM technique

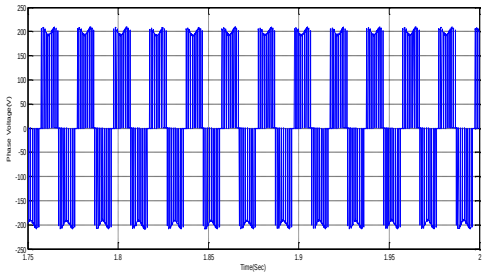

Figure 8 Output Phase Voltage Waveform Vph For 3-Level of DCMLI using PODPWM technique

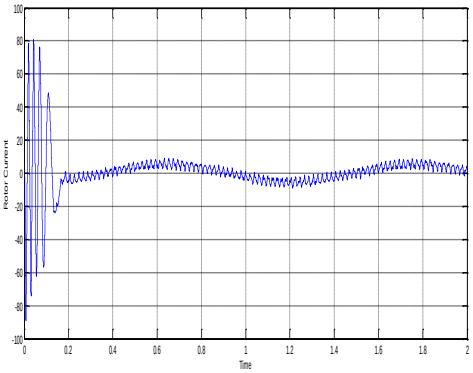

Figure 9 Rotor current characteristics of DCMLI fed IM drive

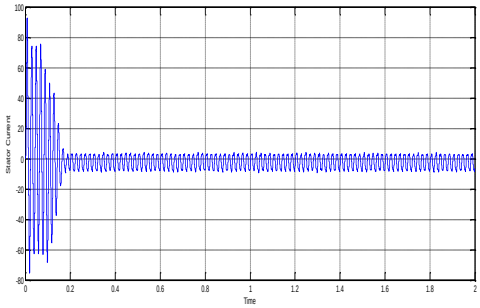

Figure 10 Stator current characteristics of DCMLI fed IM drive

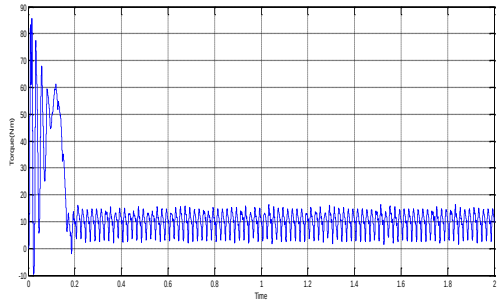

Figure 11 Torque characteristics of DCMLI fed IM drive

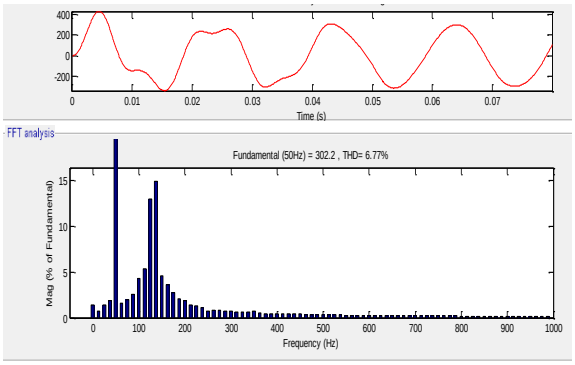

Figure 12 FFT plot for PODPWM strategy in 3-level for IM load

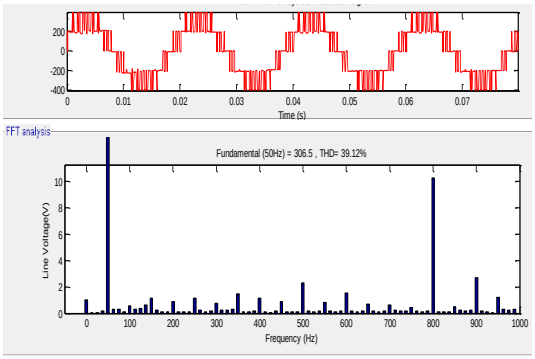

Figure 13 FFT plot for output phase voltage of PODPWM technique in 3-level DCMLL for IM load

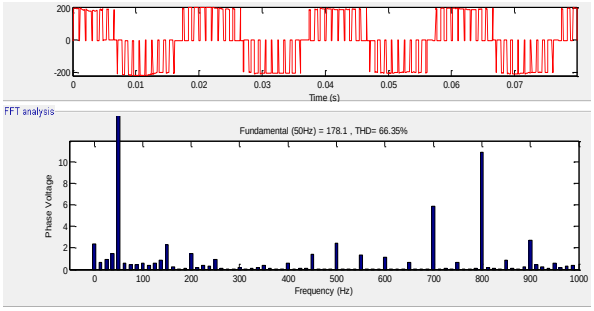

Figure 14 FFT plot for output phase voltage of PODPWM technique in 3-level DCMLI IM load

6. Conclusion

In this work the simulation results of three phase three level diode clamped multilevel inverter fed Induction Motor load with modulating strategy are obtained through MATLAB/SIMULINK. The simulation result shows that the harmonics have been reduced considerably. The three level inverter fed induction motor system has been successfully simulated. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The output quantities like phase voltage and line voltage, THD spectrum for phase

voltage and line voltage and torque, rotor current, stator current characteristics of induction motor are obtained

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A. First Author

Sadhana Pandey was born on February 13, 1991. Her graduation in Electrical Engineering from the Maharana Pratap College of Technology (MPCT) in Gwalior and pursuing M.E at Madhav Institute of Technology and Science (MITS) in Gwalior.

B. Second Author

Praveen Bansal obtained his bachelor of Engineering (Hon's) in Electrical Engineering from Madhav Institute of Technology and Science(MITS) ,Gwalior in 2009,MTech degree in Electrical Drives from Maulana Azad National Institute of Technology in 2012,Currently he is an Assistant Professor at MITS,Gwalior. His area of interests includes Multilevel level Inverters, Induction motor modelling ,PWM techniques.