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Design of 2.5 GHz Phase locked loop using 32nm CMOS technology.

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ABSTRACT

Nowadays, multi-band frequency synthesizers are very popular for their compatibility. Low power designs is a very hot topic in electronic systems. Phase locked loop is an excellent reserarch topic. Power is the amount to function or generating out energy. This means that it is way of measuring how fast a function can be carried out.So power is one of the important parameter

This paper presents the design and simulation of an area efficient chip layout of 2.5GHz fractional –N phase locked loop for bluetooth application using VLSI technology .This fractional N-PLL is designed using latest 32nm technology, which offers high speed performance at low power. Loop filter and sigma delta modulator are the most important factors in improving the performance of the system. Among variety of frequency synthesis techniques, phase locked loop (PLL) represents the dominant method in the wireless communications industry.

Keywords : VCO, phase detector, charge pump, sigma delta modulator , loop filter

I INTRODUCTION

PLL is an important analog circuit used in various communication appliations such as frequency synhesizer, radio computer,clock generation ,mioprocessors etc. A phase locked loop (PLL) is widely applied for different purposes in various domains such as communication and instrumentation. Phase-locked loop is commonly used in microproceesors to generate a clock at high frequency from an external clock at low frequency. PLL can be used to maintain a well-defined phase, and hence frequency relation between two independent signal sources. Monolithic phase locked loops have been used for clock-&-data recovery in communication system, clock generation & distribution in microprocessor and frequency synthesis in wireless application.A phase locked loop can be divided into two

architectures,an integer N- PLL and a fractional N-PLL.The fractional N-PLL offers a lower phase noise, hgher frequency resolution,and a larger loop bandwidth. The output frequency of the fractional N-PLL is $f_{out} = (N.\alpha)^* Fref$, where N is an integer, and α is the fractional part. A dual modulus divider is used to average many integer divider cycles over time to obtain the desired fractional division ratio. The main problem of this method is that by using the dual modulus divider periodically generates a spurious tones that is called fractional spur. The best method to remove the fractional spurs is using a Sigma-Delta Modulation technique. PLL is a feedback system composed of a phase detector, a loop filter and a voltage controlled oscillator (VCO) as shown in figure 1.

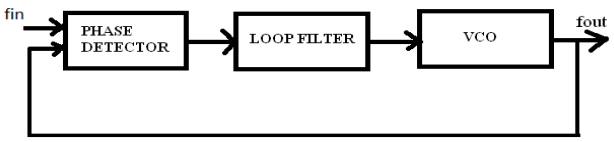

Figure.1 Basic Phase locked loop

Basic PLL is a feedback system composed of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO). The phase detector output voltage proportional to the phase difference between the VCO's output signal and the reference. The phase detector output produces a regular square oscillation when the clock input and signal input have one quarter of period shift or 90^0 (π /2). The phase error voltage controls the VCO's frequency after being filtered by the loop filter. Due to the current demand in communication technology, the proposed Fractional-N phase-locked loop or phase lock loop (PLL) is decided to design using 32 nanometre (nm) VLSI technology to achieve less area low power consumption and high stability. Microwind 3.1VLSI backend software is used. This software allows designing and simulating an integrated circuit at physical description level. For low power, low leakage transistors will be used and will Compromise on little bit frequency.

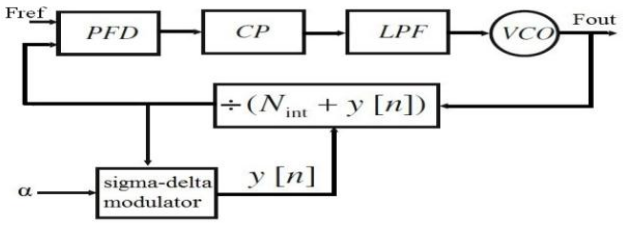

Figure 2: Block Diagram of PLL using Sigma-delta fractional –N frequency synthesizer

The proposed fractional N-PLL is shown in figure 2. It consist of Phase detector, low pass filter, charge pump, voltage controlled oscillator and Sigma delta modulator

II IMPLIMENTATION OF PHASE LOCKED LOOP USING 32 nm VLSI TECHNOLOGY.

The Phase locked loop consist of three elements.

1.Phase Detector. 2. Loop Filter. 3. Voltage controlled ocillator.

The first block of Phase Locked Loop is the phase detector. The phase detector of the PLL is the XOR gate. The output of XOR gate produces a regular square oscillation when the clock input and signal input have one quarter of period shift (90^0 or ∏/2). For other angles, the output is no more regular

2. Loop filter

Filters are the electronic circuits used alongwith rectifiers to get pure d.c. voltage. Loop filter is used to filter out the unwanted spur and also suppress noise of the control line for VCO. This helps the overall phase noise. Here the filter may simply be a large capacitor C charged and discharged through the R_{on} resistance of the switch. The R_{on}.C delay creates a low-pass filter.

3. Voltage controlled oscillator

A Voltage-Controlled Oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by a dc voltage. A voltage-controlled oscillator or VCO is an electronic oscillator

whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency.

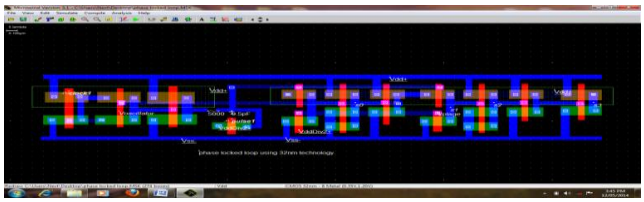

Figure.3: Layout of Phase locked loop using 32nm VLSI technology.

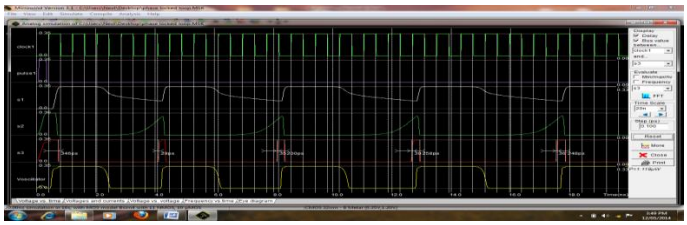

Figure.4 : Voltage vs time output of PLL

The complete PLL using 32 nm VLSI technology is shown in figure 3.This circuit is implemented with 11 NMOS transistor and 10 PMOS transistor. Technology used is CMOS 32nm with High K /Metal/Strain - 8 Metal copper. Supply VDD is DC supply of 0.32 volt. Input clkIn is pluseof 0.35volt (logic 1) and 0.00volt (logic 0) with tlow & thigh equal to 0.40nsec.and trise equal to 0.010nsec. This implementation includes a filter register of 5000.0ohm . The virtual capacitor C_{filter} is fixed to 0.5pf. This resistance and capacitance are easy to integrate on-chip. The input frequency is fixed to 2.1GHz. During the initialization phase, the precharge is active & control voltage Vc rapidly change to VDD/2. Then, the VCO outputs starts to converge to the reference clock.Then Vc tends to oscillate and stable where the PLL is locked and stable.

The proposed work consists of additional sigma delta modulator block with fractional input. The input of sigma-delta modulator is the desired fractional division number (α), where the output consists of a DC component y[n] that is proportional to the input (α) plus the quantization noise introduced due to using integer divider instead of ideal fractional divider.The frequency divider divides the output frequency of the VCO by N_{int} +y[n], where $N_{int}$is an integer value and y[n] is the output sequence of the modulator.

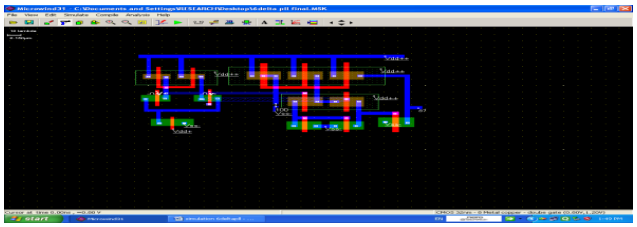

Figure 5: Layout of sigma delta modulator

Figure 6, shows the optimum, high efficient chip design of low power fractional-N PLL frequency synthesizer using sigma delta modulator using 32nm VLSI technology. This layout design is implemented using 23 NMOS along with 23 PMOS BSIM4 transistors with optimum dimensions of transistors and metal connections according to the Lambda based rules of microwind 3.1 software. For the proposed PLL, power supply VDD of 1 volt is used. Figure 8 shows the voltage versus time response of fractional-N PLL. Figure 7, is the frequency versus time response of PLL which shows that PLL is locked on 2.50 GHz frequency.

Figure.6: .Layout of low power fractional N-PLL

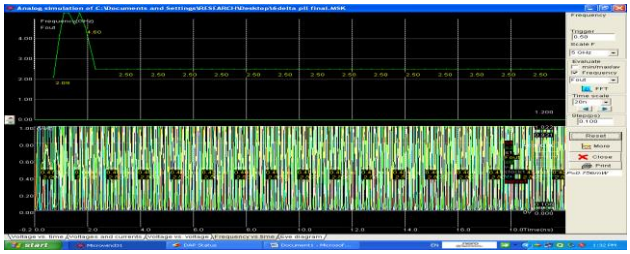

Figure7 : Frequency vs Time response

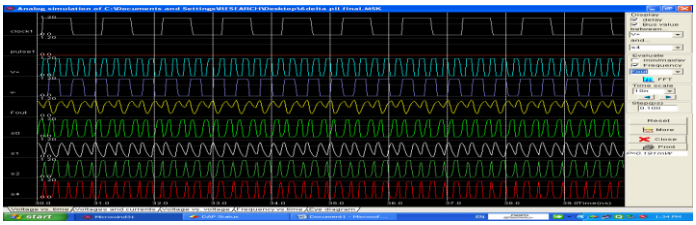

Figure 8: Voltage vs Tine Response

III CONCLUSION

Today, VLSI technology is the fastest growing field. Low power consumption is always the first demand of advanced VLSI technology. The layout architecture of proposed PLL is designed in a very compact and optimized way using microwind 3.1 VLSI Backend software.To Implement fractional N-PLL using VLSI technology, first each block of PLL such as Phase detector, loop filter and VCO had been implemented using 32nm CMOS technology with microwind 3.1 backend software of VLSI. Then sigma delta modulator is designed. Thus very efficiently Plase locked loop with sigms delta modulator is designed. For individual blocks of PLL, analog circuits are designed using CMOS transistor and power consumption found less. It is also found that power consumption of designed PLL is 57.16µw.

In this way high efficient, low power, optimum area chip is designed for fractional-N phase locked loop frequency synthesizer using sigma delta modulator.

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