www.ijecs.in
International Journal Of Engineering And Computer Science
Volume 14 Issue 07 July 2025, Page No. 27499-27507
ISSN: 2319-7242 DOI: 10.18535/ijecs/v14i07.5182

Development and optimization of a new charge integrator for reading very low energy beams

[1]Defo Njeuho Jean Rostand, [2]Wembe Tafo Evariste

[1,2]Department of Physics, Faculty of Science, University of Douala, P.O. Box 24157 Douala, Cameroon

Abstract

This work aims to make a scientific contribution to the reduction and development parasitic quantities linked to the measurement of very weak currents; in fact, the components electronics which constitute the measurement chain are imperfect in nature and present several faults such as offset voltage, bias current, injection charges, leakage currents and electronic noise. Failure to take charge of these quantities causes an error in the reading of the information. In the optics of wanting convert a current of the order of picoampere or a charge of the order of femtocoulomb, all elements of the measurement chain must be linear to maintain the relationship charge-voltage and current-voltage. However, the use of transistors in our integrator causes the injection of charge and leakage currents in the storage capacitor which disturb the useful signal. The major objective here will be to bring out these imperfections caused mainly by transistors and to propose a new integrator to reduce them. The simulation results show that the offset voltage has been reduced by $0{,}35mV$, the injection charge by $3{,}25 * 10^{-3}pF$ and the output noise by $0{,}7\,mV$. The integrator thus produced amplifies and integrates both with a cut-off frequency of 40 MHz and a linearity coefficient of 0,66%.

Keywords : Noise, Gated Integrator, Injection charge, Leakage Current Prevention, offset adjutment

1. Introduction

A detector is an instrument able to detect the passage of a particle and deducing its various characteristics, including its mass, energy, momentum or even its electrical charge. Knowing that the signal from the detector is very weak in nature, a conditioning chain must be associated with it for shaping in order to make the signal usable. Indeed, a signal acquisition chain generally consists of a sensor, a charge preamplifier, a filter, a gated integrator and an analog-to-digital converter [1][3]. The schematic diagram of an acquisition chain is shown in Figure 1 [5]

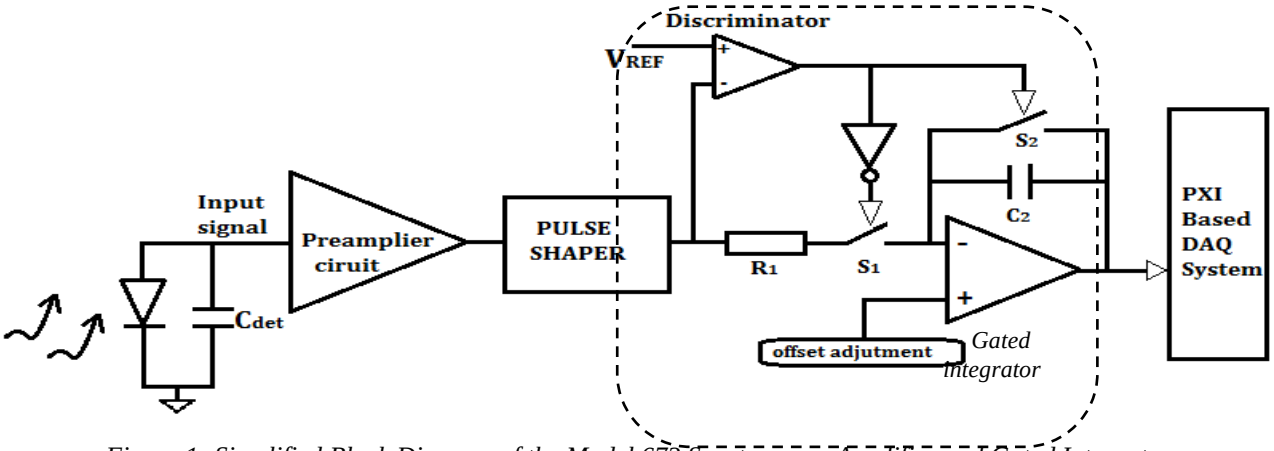

Figure 1: Simplified Block Diagram of the Model 673 Spectroscopy Amplifier and Gated Integrator

The objective here is to simplify this chain in order to build a gate integrator capable of amplifying and integrating the signal at the same time. Processing large amplitude signals of the order of tens of millivolts does not pose any problem; but as the amplitude of the input signal approaches magnitudes of influences such as the offset voltage and the charge injection , the reading of the signal becomes erroneous;

Different structures have been developed to solve this problem; these structures were designed to reduce offset voltage[9], leakage currents and charge injection during the integration of the input signal [1][5]. In this paper, we propose a new compensation scheme of the offset voltage, the injection charges and the leakage currents to simultaneously amplify and integrate a signal and we will make a comparative study between our proposed model and two other existing schemes.

2. Literature review

The integrator is a low pass filter that detects energy peaks left by a particle as it passes through the sensor. In order to reduce the components of the acquisition chain, and reduce energy consumption, various researchers have developed devices that have both the integration and amplification function using CMOS transistors as resistor feedback; but only that these structures pose a problem of charge injection which disturbs the useful signal in the storage capacitor. The reduction of the injection charge cannot be done correctly if the offset voltage has been reduced because these two imperfections are of the same order of magnitude; a symetrisor [9] or track and hold circuit [7]can be used to reduce the offset voltage:

- The Integrator 1 uses an integrator with a T-feedback, it was designed with to reduce charge injections and leakage currents [5].This is valid for the transistors S_2 and S_3, but poses a problem for the transistor S_1; in fact, when the transistor S_1 is turned off, the charges are distributed between the drain and the source; transistor S_3 cancels the charges going to the drain while the charges leaving the source are added to the useful signal in capacitor C.
- The integrator 2 compensates for structure 1, the charge injected by the channel and by the clock is very much reduced [10] but the structure is limited by the presence of the voltage d 'offset at the output of the integrator; therefore it is impossible for this integrator to correctly process a signal of the same order of magnitude as the offset voltage. Much more, the addition of the compensation block increases the power consumed and the output noise due to the integration.
- This integrator 3 is similar to the structure 2; the charge injected by the clock and the channel of the SR transistor are reduced, but a leakage current flows through the SR transistor during the accumulation phase. When this transistor is turned off, the injected charges are distributed proportionally between the capacitors Cc and C_f; Therefore a perfect compensation is obtained by taking $C_C \gg C_f$ [1][3].

3. Design of Proposed Dynamic gated integrator

We therefore propose to build a charge integrator that will simultaneously amplify and integrate the signal present at the detector input. This integrator will operate in two phases, namely an accumulation phase (where the signal present at the input is stored in the capacitor C through the transistor T_1) and a restitution phase (where the stored signal is returned to the output through the transistors T_2 and T_3). We relied on two basic models of the gated integrator namely:

- The gated integrator with one feedback transistor : its main drawback is that its conversion gain is low and the charge injection is maximum.

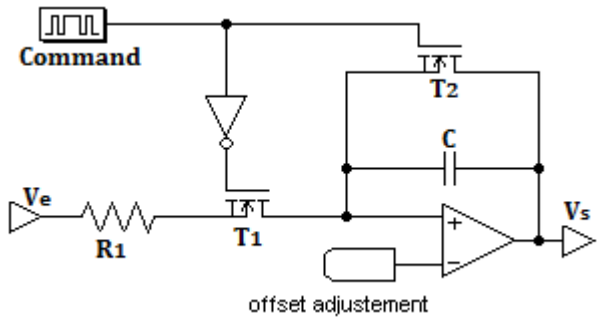

Figure 2 : basic structure of gated integrator using one transistor Switch in feedback

- The gated integrator using two feedback transistors structure in T to increase the conversion gain and reduce the charge injection. It is on this second model that will build a new compensation structure for the charge injection and leakage current.

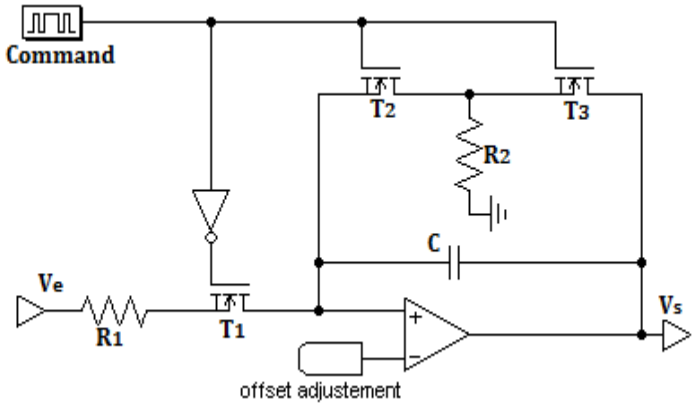

Figure 3: basic structure of gated integrator using dummy Switch in feeback

3.1. Charge injected by the clock

When the clock is switching from the high to the low state, the capacitive coupling between the gate and the storage capacitor C via the recovery capacitor C_{ov} causes the injection charge q_{ck} into C [7][8]This injection therefore disturbs the useful signal. In the absence of the compensation transistor T_0, the charge injected by the clock (Figure 6, 7, 8, 9 and 10); and the voltage error in the capacitor C are respectively:

$$q_{ck} = \frac{WC_{ov} * C}{WC_{ov} + C} V_{Ck} \quad and$$

$$\Delta U = \frac{q_{ck}}{C} = \frac{WC_{ov}}{WC_{ov} + C} V_{Ck}$$

Where $C_{ov}, W \; and \; V_{Ck}$ represent the gate source recovery capacitance, the channel width and the potential difference across the gate during the transition respectively.

3.2. Load injected by the channel

To study this charge injection phenomenon,it is necessary to consider the difference the state of the in channel between the two operating modes: open and closed. When open, the voltage on the gate of an NMOS transistor is low state. The transistor is then in the low inversion or sub-threshold regime, its operation in this case is similar to the BJT transistor; it is said to be blocked, so there is no electrical charge in the channel. The MOS resistance is of the order of giga ohm.

When the transistor is closed, the voltage at the gate of the NMOS is high, the transistor is then in a strong inversion state, its operation is similar to that of a resistor [6][11]. The charges accumulate in the channel thus ensuring an electrical connection between the drain and the source; we say that the transistor is on. The expression of the resistance of the transistor is given by the following relation

$$R_d = \frac{1}{\mu \frac{W}{L} \mathrm{C_{ox}} (V_{GS} - V_{th})}$$

Where I_{D0} is the saturation current, W and L respectively the width and the length of the transistor, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, C_{ox} is the capacitance of the oxide, V_{th} the threshold voltage, V_T, μ is the mobility of charge carriers, η is the slope factor in the sub-threshold regime.

When the transistor is on, the charges accumulate in the channel, forming an electrical connection between the drain and the source; blocking the transistor causes charge to be injected into both side of the channel: the general expression for the charge injected into the channel is:

$$q_C = -WLC_{ox}(V_{GS} - V_{th})$$

Where the gate-source voltage V_{GS} is positive for the NMOS and negative for the PMOS [6]; we

therefore retain that the injection charge q_C will be negative for NMOS and positive for PMOS.

We use a T-shaped feedback resistor made of two NMOS transistors T_2, T_3 and a resistor R_2, to increase the voltage gain and a transistor T_1 to avoid the stacking of energy in the storage capacitor C during information processing. The transistor T_1 and T_3 have no effect on the storage capacity C because they are located between 2 sources. The transistor responsible for injecting charge into capacitor C is transistor T_2 (Figure 6, 7, 8, 9 and 10);. If the clock signal is slow, the loads are distributed rationally according to the impedances on both sides of the channel. For a fair distribution between the drain and the source, the slew rate of the clock must be very high. The total induced charge and the voltage error in the capacitor C are respectively [6]

$$Q = \frac{WC_{ov} * C}{WC_{ov} + C} V_{Ck} - \frac{\mathrm{WLC_{ox}(V_{GS} - V_{th})}}{2}$$

$$\Delta V = \frac{WC_{ov} * C}{WC_{ov} + C} V_{Ck} - \frac{\mathrm{WLC_{ox}(V_{GS} - V_{th})}}{2 * C}$$

with $V_{GS} = V_{DD} - V^-$ where V_{DD} is the high-level voltage of the clock and V^- the inverting voltage of the AOP.

3.3. Charge Injection Compensation

The idea here is to use a PMOS type T_0 transistor to connect it to the inverting input of the AOP.

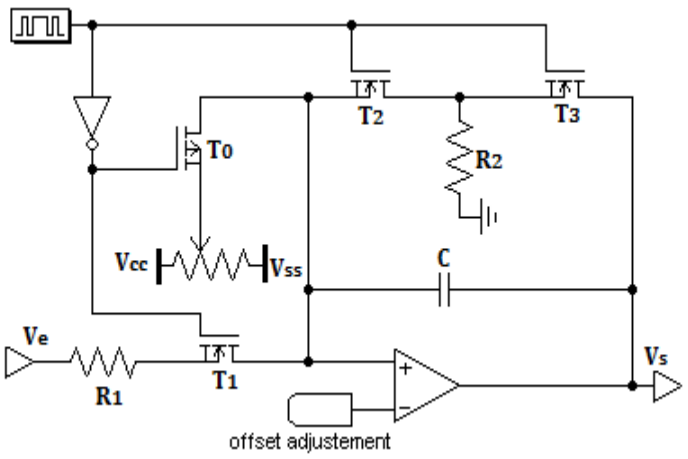

Figure 4 : Schematics of the gated integrator for charge injection compensation

Knowing the charge injected into the capacitor C by the transistor T_2 of the NMOS type, a fourth transistor T_0 of the PMOS type is added which will turn off at the same time as T_2; capacity C will therefore receive two injection charges (Fig 11); one coming transistor T_2 and the other from transistor T_0. The charge injected by T_2 is then:

$$Q_2 = \frac{WC_{ov} * C}{WC_{ov} + C} V_{DD} - \frac{\mathrm{WLC_{ox}(V_{DD} - V^- - V_{thN})}}{2}$$

And the one injected by T_0 is therefore:

$$Q_0 = \frac{WC_{ov} * C}{WC_{ov} + C} V_{SS} - \frac{\mathrm{WLC_{ox}(V_{SS} - V^- - V_{thP})}}{2}$$

The injection charge can be reduced if and only if

$$Q_2 + Q_0 = 0, \qquad then$$

$$\frac{WC_{ov}*C}{WC_{ov}+C}\left(V_{DD} + V_{SS} - \frac{\mathrm{WLC_{ox}(V_{DD}+V_{SS}-2V^- - V_{thN} - V_{thP})}}{2}\right) = 0.$$

The offset adjustement network connected to the plus terminal of the amplifier cancels the offset voltage specific to the operational amplifier and brings the potential V^- to zero; perfect compensation is only possible if and only if:

- The threshold voltages of the two transistors obey the equality $V_{thN} = -V_{thP}$
- The clock levels are configured such that $V_{DD} = -V_{SS}$.

3.4. Compensation Leakage Current

Since we operate in electronic instrumentation, a small current called leakage current flows through it and has the following expression [1][11].

$$I_f = \frac{w}{L} I_{D0} * \exp\left(\frac{V_{GS} - V_{th}}{\eta * V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{\eta * V_T}\right)\right)$$

$$with\ I_{D0} = \mu C_{ox}(\eta - 1)V_T^2\ ;$$

Considering the reduced offset voltage, the source of transisitor T_2 is virtually grounded masse ($V_S = V^- = 0V$); a transistor T_3 is therefore mounted in parallel with the resistor R_2 which closes when the transistors T_2 are blocked; on will therefore have the drain of transistor T_2 connected to ground $V_D = 0V$ **;** that is visible about Figure 12,13 and 14; The leakage current will therefore be reduced to use the figure 6:

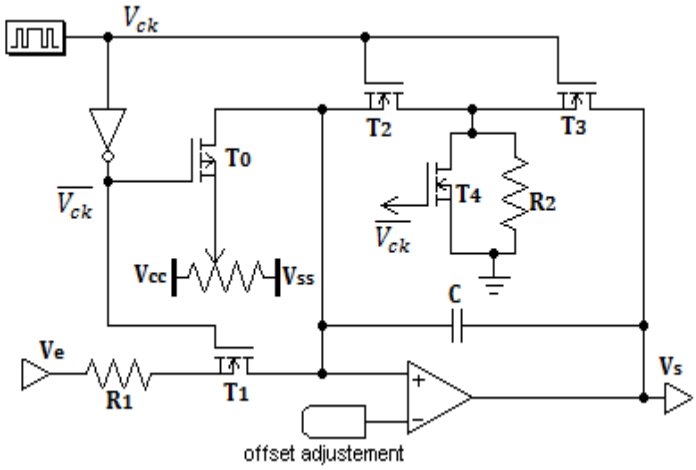

Figure 5 : Schematics of the gated integrator for

Compensation Leakage Current

3.5. Frequency analysis of the integrator

This involves studying the frequency range admissible by the charge integrator. To do this, we determine the transfer function linking the output voltage and the input voltage of our integrator (figure 16). Let us pose [9]

$$K_1 = R_1 + Z_{T1}, K_2$$

$$= Z_{T3} + \frac{Z_{T2} * Z_{T4} * R2}{Z_{T2} * Z_{T4} + Z_{T2} * R_2 + Z_{T4} * Z_{T2}}$$

The transfer function is given by:

$$H(w) = \frac{V_e}{V_S} = -\frac{K_2}{K_1} * \frac{1}{1 + jK_2Cw}$$

Where Z_{T1}, Z_{T2}, Z_{T3} *and* Z_{T4} respectively represent the impedances of transistors T_1, T_2, T_3 and T_4

4. Results and interpretations.

4.1. Output of integrator using one feedback transistor (figure 2)

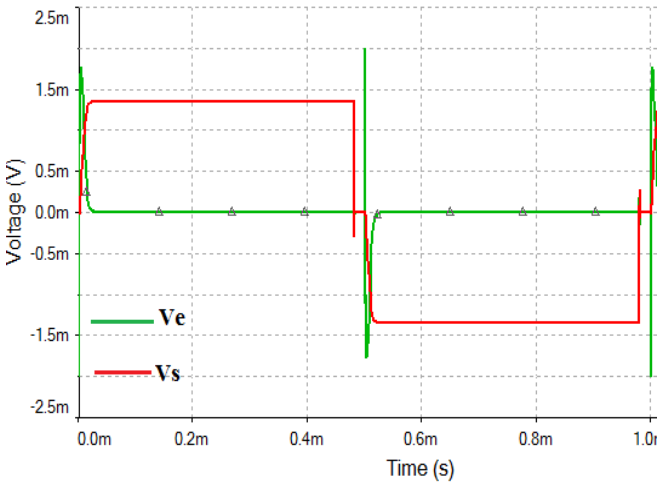

Figure 6 : Response for an impulse input

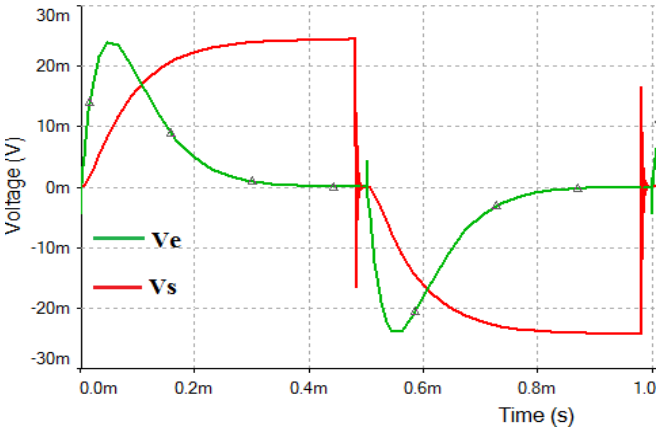

Figure 7 : Response for a bidirectional Gaussian input

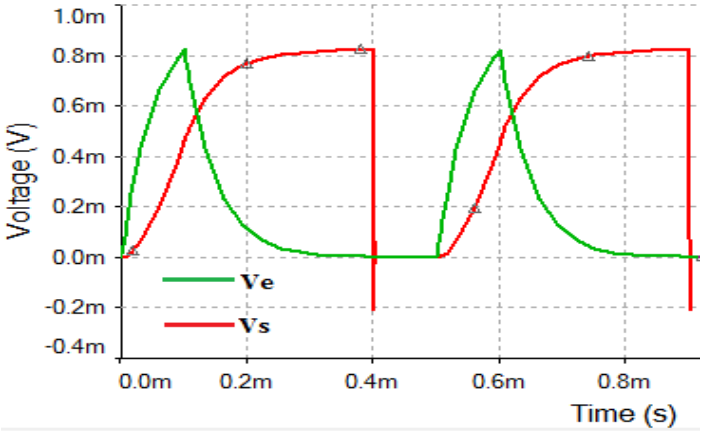

Figure 8 :: Response for unidirectional Gaussian input

4.2. Output of integrator using two feedback transistors (figure 3)

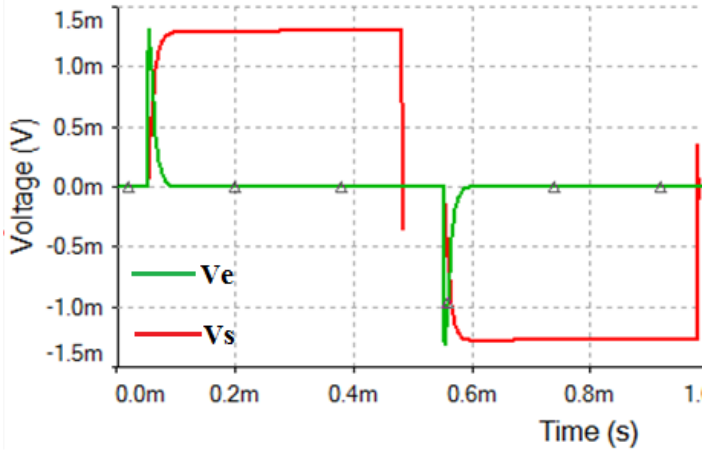

Figure 9 : Response for an impulse input

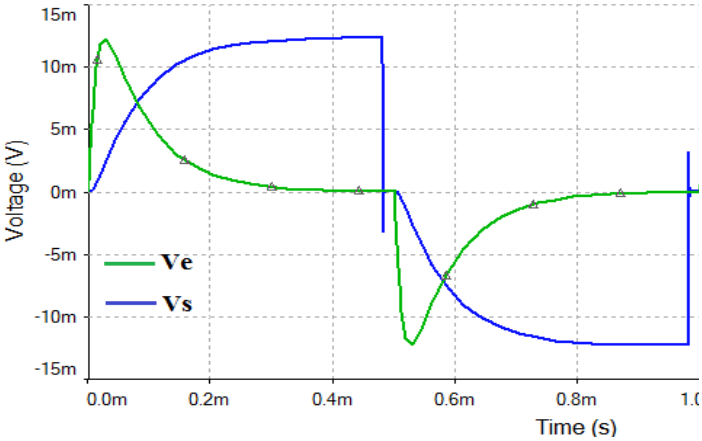

Figure 10 : Response for a bidirectional Gaussian input

4.3. Compensation of charge injection (figure 4).

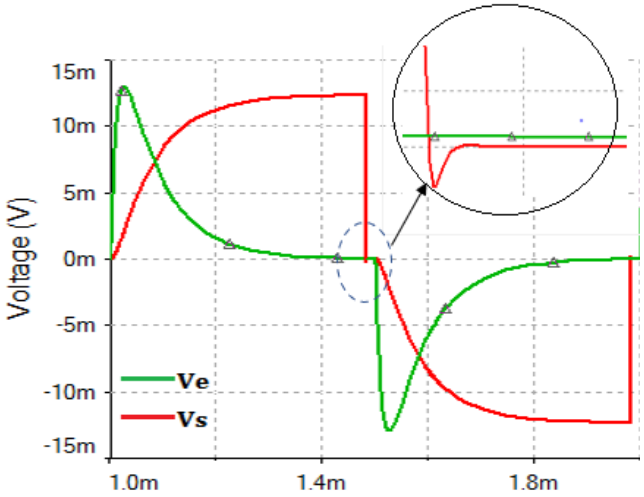

Figure 11 : Response for a bidirectional Gaussian input

4.4. Compensation of charge injection and leakage current (figure 5).

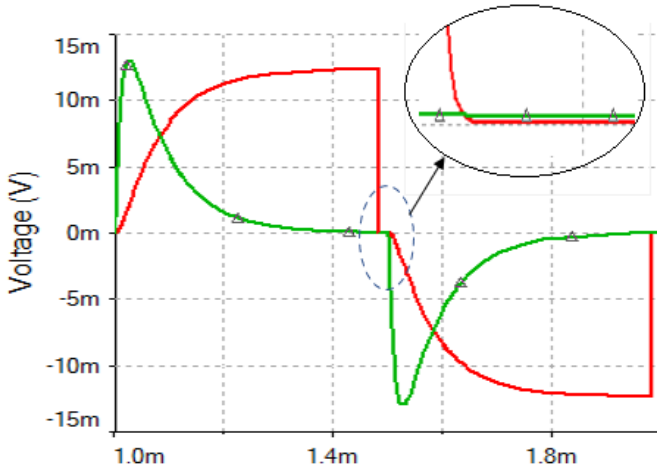

Figure 12 : Response for a bidirectional Gaussian input

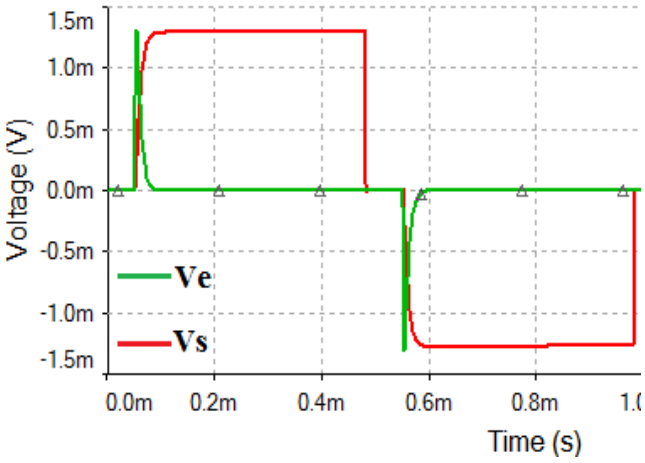

Figure 13 : Response for an impulse input

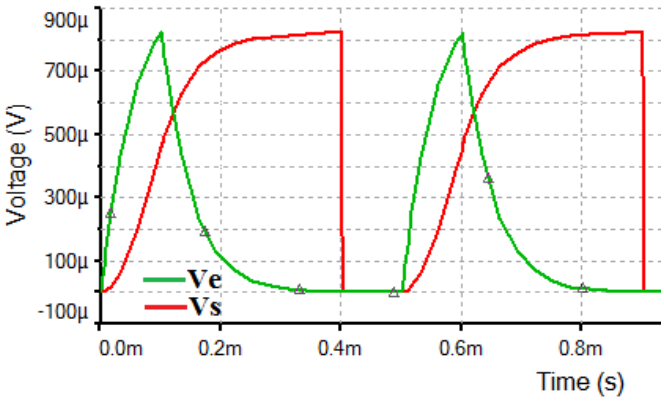

Figure 14 : Response for unidirectional Gaussian input

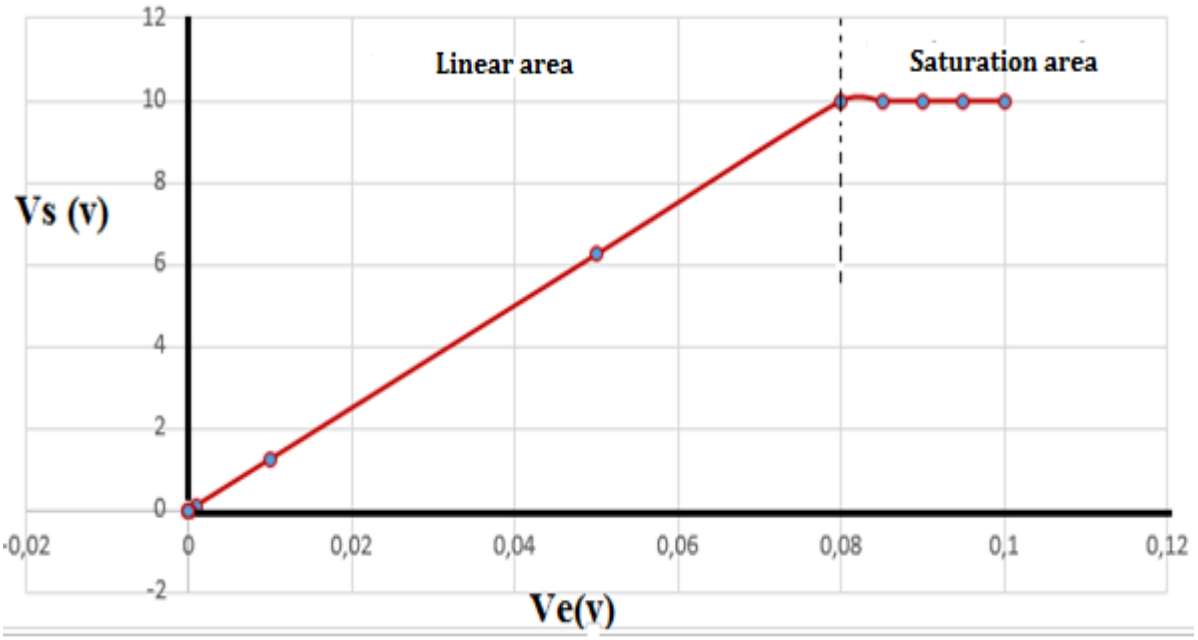

Figure 15: Linearity of the gated integrator: $10^{-6}V < V_e < 10^{-2}V$ *or* $10^{-11}A < i_e < 10^{-7}V$

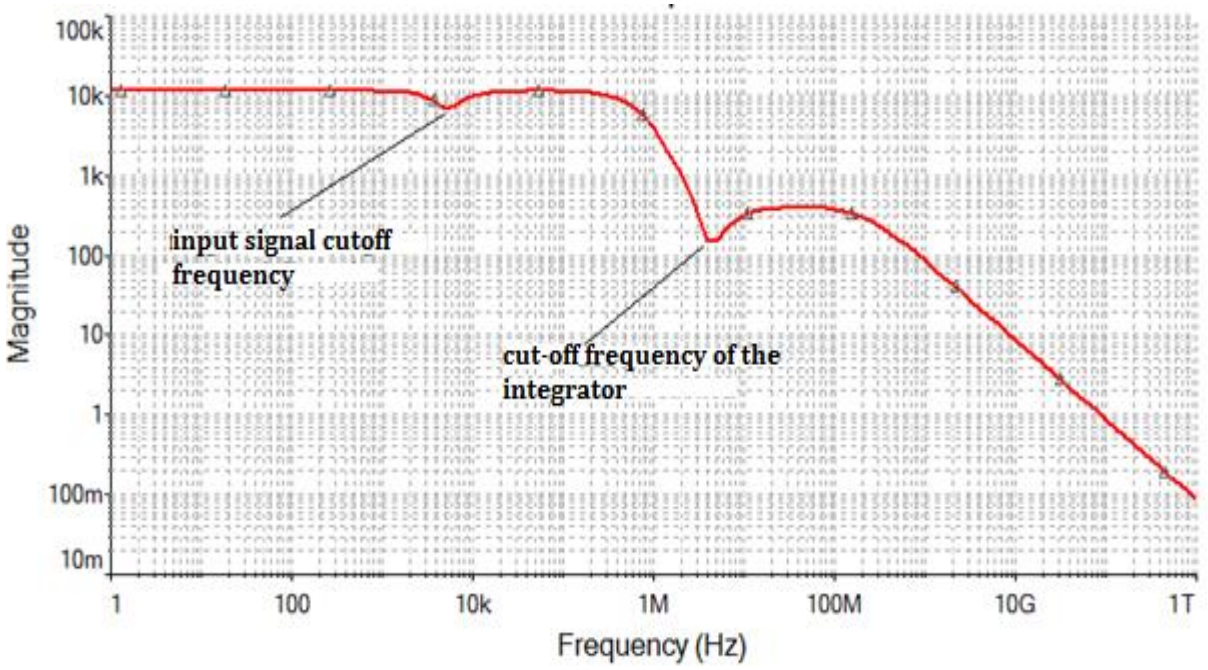

Figure 16: Frequency response of the integrator feedback impedance

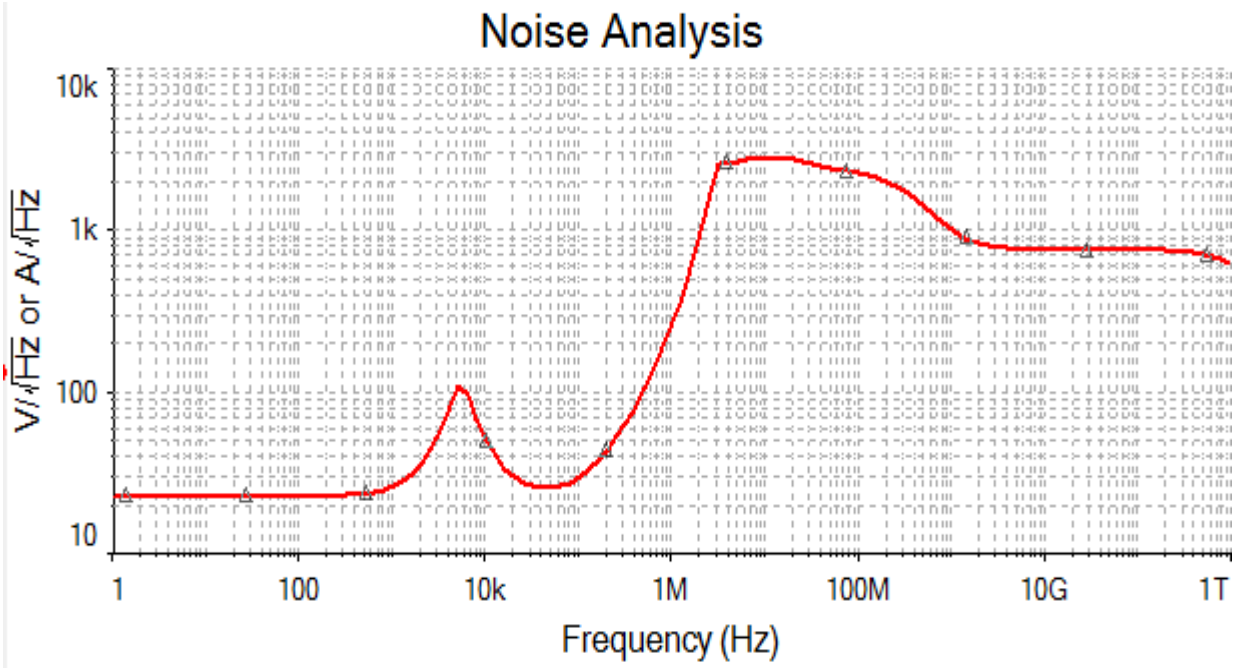

Figure 17: Frequency response of the noise at the output of the integrator

Table 1 : Characteristics of gated integrator

Settings	Value
Cutoff frequency	≈ 40 MHz
Saturation voltage	±10
Offset voltage reduiced	350 μV
Conversion gain	-125 V/V
Linearity error	≤ 0,0066
Voltage caused by injection charge	3,25 mV
Injection charge	$\leq 3{,}25 * 10^{-3} pF$
Output voltage Noise	$\leq 0,7\ mV$
Operating temperature	-40°C à 125°C

Table 2 : Comparative study of the different structures of gated integrator

	[1]	[5]	[10]	This work
Output offset voltage	2,2 mV	0,5 mV	0,5 mV	0,35 mV
Injection charge	$2 * 10^{-6}\ pC$	50,4 pC	116 pC	$3{,}25 * 10^{-3} pC$
Linearity error	0.14 %	0.03 %	0.06 %	0.66 %
Voltage conversion gain	$-1.63V/fc$	$-1V/V$	$-1V/V$	$-125V/V$
Output voltage noise	$1{,}6mV$	$0{,}6mV$	$0{,}7mV$	$2{,}75mV$

5. Conclusion

The objective here is to design a charge reading or integration circuit to detect fast particles at low energies. Knowing that the input signal was weaker than the offset voltage and the injection charge, a method had to be found to reduce the offset voltage and subsequently the injection charge and leakage currents. generated by transistors. The study and design of the charge integration circuit was carried out in National instrument's Multisim and Psipe simulators. We see that the integrator is linear (figure 15) and allows us to convert a charge of the order of $3{,}25 * 10^{-3} pF$ without loss of information. The simulation results show that the offset generated by the injection load has been reduced by 3.25mV, the offset voltage and currents are also reduced so as not to disturb the input signal. Given the comparison established, the charge integrator thus produced has simplicity in implementation, is less sensitive to noise, and the power consumed by the compensation circuit is less.

Author's Contributions

- **Defo Njeuho Jean Rostand :** Design and simulations model. Also, contribute to the writing of the paper.
- **Wembe Tafo Evariste:** Data interpretation and contribute Revise and improve the final drafts of the paper.

Ethics

The corresponding author confirms that all of the other authors have read and approved the manuscript and no ethical issues involved.

References

1. Chao-Yang Zhou,Hong S., Rui-Shi M., Cheng-Fu D., Y. Qian, J. Kong "An accurate low current measurement circuit for heavy iron beam current monitor" Nucl. Instrum. Meth. Phys. Res. B 280 (2012) 84–87.
2. Wembe T. E., Djamet Y. A., Essimbi Z. B. Novel Approach to Build a Gated Integrator for High-Resolution Energy Spectroscopy Systems. IOSR Journal of Electrical and Electronics Engineering, Vol. 12, Issue 2 Ver. III (Mar. - Apr. 2017), PP 51-57. DOI: 10.9790/1676-1202035157
3. Kong, J., S. Hong, ChenZ.Q.,Dong C.F, Qian Y.et al., 2010. Development of multi-channel gated integrator and PXI-DAQ system for nuclear detector arrays. Nucl. Instrum. Meth. Phys. Res. A, 622: 215-218. DOI: 10.1016/j.nima.2010.07.030
4. Wembe, T.E., I.A. Moukengue, D. Teko and Y.A. Djamet, 2014. Noise optimization of readout front ends in CMOS technology with PS circuit. Asian J. Applied Sci., 2: 752-761.
5. Folla Kamdem Jérôme, Wembe Tafo Evariste, Djamet Yimga Arnaud and Essimbi Zobo Bernard,. An Optimal Gated Integrator Circuitry based On Dummy Switch For High-Resolution Energy Spectroscopy . Mar. – Apr. 2018, Volume 13, Issue 2 Ver., PP 63-69,University of Yaoundé I,
6. Jaymin M. Patel, Prof. Mehul L. Patel. Charge Injection & Clock Feed through Reduction Technique in Switched Capacitor Circuit. Volume 2,Issue 4, April -2015
7. Shirin Pourashraf, Jaime Ramirez-Angulo et Al. An Amplified Offset Compensation Scheme and its Application in a Track and Hold Circuit ». DOI 10.1109/TCSII.2017.2695162.
8. Weize xu and Eby g. Friedman. Clock feedthrough in cmos analog transmission gate switches. Department of Electrical and Computer Engineering, University of Rochester, Rochester, New York 14627-0231, May 28, 2004
9. Bakoune Pierre Hypolite1, Wembe Tafo Evariste, Moukengue Imano Adolphe1, Kana Kemgang Lucas, Mouen Mouangue Arlette Joelle.An Accurate Low Current Measurement Circuit for High-Resolution Energy Spectroscopy Systems. Asian Journal of Applied Sciences (ISSN: 2321 – 0893) Volume 03 – Issue 06, December 2015.
10. Djamet Yimga Arnaud, Wembe Tafo Evariste and Essimbi Zobo Bernard. Design

and Simulation of Novel Gated Integrator for the Heavy ion Beam Monitors System.

11. Ken Ueno, Tetsuya Hirose, Tetsuya Asai and Yoshihito Amemiya , JULY 2009 « A 300 nW, 15 ppm/°C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold. Department of Electronics and Information Engineering, Hokkai-Gakuen University, Sapporo, Japan 2002.