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A New Family of CMOS Inverter Based OTAs for Biomedical and Healthcare Application

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Abstract
Inverter-based Operational Transconductance Amplifiers (OTAs) are versatile and friendly scalable analog circuit blocks. Especially for the new CMOS technological nodes, several recent applications have been extensively using them, ranging from Analog Front End (AFE) to analog-to-digital converters (ADC). This work tracks down the current advances in inverter-based OTAs design, comparing their basic fully differential structures, such as Nauta (N), Barthelemy (B), Vieru (V) and Mafredini (M) ones, and, in addition, mixing them up to propose new fully differential single-ended and two-stage hybrid versions. The new herein-proposed fully differential hybrid OTAs are the composition of Barthelemy/Nauta (B/N), Barthelemy/Manfredini (B/M), Nauta/Vieru (N/V), and Manfredini/Vieru (M/V) OTAs. All OTAs were designed using the same Global Foundries 90 nm Tanner 16.30 and their performances are compared for post-layout simulations.

Keywords: CMOS, ADC, Common Drain Devices

1. Introduction

The development of wearable devices, particularly in the biomedical and healthcare field of applications, has grown much especially during the last two decades. The sensors used in this field have special design and development restraints: the portability, the size and weight, the longevity, ergonomics and the power consumption in parallel with the energy-efficiency are among the most important aspects to take in consideration. The devices must have small form factor and active area with low power consumption, enabling comfortable, unobtrusive and long-time monitoring, hence, suitable for daily use. Sensing amplifiers usually dominate the power and the noise of the recording front end, therefore significant research activity has been focused on designing this block, taking into consideration the need for high gain and high energy-efficiency, with proposals of new strategies to overcome the challenges of modern CMOS technologies.

Particularly, the design of operational transconductance amplifiers (OTAs) in modern CMOS technologies, face now additional and special design challenges. Among these, it is perhaps the most important trade-off to be considered, which opposes gain improvement techniques in a way that complies with a high energy-efficiency demand, under low biasing voltages and, furthermore, with a low noise impact. In fact, it is well known that the intrinsic gain (gm/gds) of CMOS technologies is suffering a considerable decrease to an estimate value smaller than 20 dB, i.e., 10 V/V, while the variability of the intrinsic gain may be in the range of 10 dB, predominantly below standard 65 nm technological nodes [9]. Therefore, new strategies must be proposed.

In particular, two configurations are proposed, addressing both high and low voltage supplies, i.e., supplies above 1.8 V and below 1 V. In the first case, a voltage-combiners biased inverter-based OTA is proposed

with complete freedom from static current sources, by properly biasing the devices in voltage through the usage of two pairs of cross-coupled voltage-combiners, improving the gain and energy-efficiency of the basic structure. In the latter case, in order to operate with a nominal voltage supply source spanning from 1.2 V to 0.7 V without any stacking issues and maintaining proper DC biasing, which otherwise would not be possible for lower supply voltage values, e.g., below 1.8 V, a doublet of folded voltage-combiners bias the core structure, which improves the performance furthermore at the cost of higher active-area, since, in fact, a higher number of active devices is employed.

The performance of such inverter-based dependent systems not only relies on their own topologies but is also dependent on the underlying Operational Transconductance Amplifiers (OTA) schematics. If such a system's basic analog blocks can be improved in any aspect, the whole system can benefit from it. Unfortunately, not all the performance characteristics can be improved simultaneously, as there are always trade-offs that must be considered and decided during the OTA design.

The OTA includes a pair of input inverters for receiving differential input signals, a common-mode voltage control circuit for controlling the DC voltage levels of the inverters, and a Q-control circuit for adjusting the OTA's output conductance. The common-mode voltage control circuit has a pair of compensating current sources and a feedback loop acting as a high-gain amplifier. The high-gain amplifier has a pair of comparators for respectively comparing the DC voltage levels of the inverter outputs with a reference voltage. The Q-control circuit includes a current source coupled to a crossed-coupled NMOS transistor pair such that the OTA's output conductance may be controlled by adjusting the current source.

Many techniques have been proposed for frequency compensation in three-stage OTA, most of them based on the conventional nested Miller compensation. With the rising deep submicron technology and growing demand for reduced power supply in recent CMOS designing, different innovative techniques are required to be consider, which must be competent in working with reduced power supply without sacrificing for speed and dynamic range of the circuit. However, the accuracy of various analog and mixed-signal designs depends on the fast-switching capability of the amplifier's output voltage which should not be affected by the slew-rate

2. Literature Review

In this work, low power high-performance dynamic threshold MOSFET based two stage OTAs using area efficient biasing technique has been proposed. This DTMOSFET based OTAs operates at low voltage of ±0.5 V and suitable for designing various low power analog and mixed-signal applications. Simulation results obtained with TSMC 0.18μm level 53 CMOS technology using Mentor Graphics Eldo spice are discussed and compared with other relevant work in literature. This signifies that unlike conventional OTA, DTMOSFET based OTAs offers very high slew-rate along with improved performance parameters and low static power dissipation. The temperature and Monte Carlo analysis of the DTMOSFET OTAs demonstrates its outstanding performance against the variations in temperature and device parameters. The universal voltage mode filters simulated as an application confirms the workability of the proposed designs

3. Existing Work

3.1 Topological description

A new family of inverter-based OTAs biased by voltage-combiners for gain and energy-efficiency improvement. This Fig. 3.1. Standard VCs: a) PMOS based; b) NMOS based. Fig. 3.2. Inverter-based OTA biased by standard VCs. Ohm impedance matching. The schematic of a voltage-combiner in its standard configuration is shown in Fig. 3.1, for both PMOS and NMOS flavors. A mixture of two common-drain (CD) devices and two common source (CS) devices have a frequency-response similar to that of a first order low-pass filter . The gain of a voltage-combiner (VC) can be expressed as in (1) where, with proper sizing, additional 6 dB can be obtained for each configuration. family encompasses a standard and a folded configuration. In the first case, i.e., the standard configuration, the biasing of the proposed Av VC 1 gm CS (1) gm CD inverter-based OTA is carried out by two pairs of cross-coupled PMOS and NMOS voltage-combiners. In the second case, i.e., in the folded configuration, the biasing is carried out also by two pairs of

voltage combiners, yet in a folded configuration biased in current, for proper DC point in lower voltages, e.g., supplies below 1V.

This section, presents the functional and analytical description of the circuits. Voltage combiners are known and used in radio-frequency circuitry designs, for converting fully-differential signals to single-ended ones, for 50- and 75-Ohm impedance matching.

The schematic of a voltage-combiner in its standard configuration is shown in Fig.3.1, for both PMOS and NMOS favors. A mixture of two common-drain (CD) devices and two common frequency-response similar to that of a first order low-pass filter. The gain of a voltage-combiner (VC) can be expressed as in (1) where, with proper sizing, additional 6 dB can be obtained for each configuration

On the other hand, it is possible to extract the complete gain response of the complete OTA, shown in Fig. 3.2, by evaluating only on half of the circuit, and taking advantage of the intrinsic symmetry. The DC gain can be obtained as in (2), while the GBW expression is given by (3). Through (2), the gain depends mainly on the gm of the devices in the inverter block and rises as the gm of M3 increases as well as when the gm of M2 and M5 decreases, the output noise small-signal equivalent circuit is shown in Fig.3.3. The output noise can be given by (4) and the input refer red noise is in (5). The noise contributions are detailed in Fig.3.3, and considering that gmCS gmCD, it is fair to approximate the noise impact to a factor of nearly two, which is comparable with that of standard cascade OTAs, since the noise impact is dominated by the structural CMOS inverter contribution. The body-effect is neglected for simplicity.

The appropriate response to voltage supplies below 1 V relies on a Topology in which the CD and CS devices are folded and are, furthermore, biased by current sources in a fully-differential configuration. The corresponding circuit schematic is shown in Fig.3.4, where a doublet of folded voltage-combiners is designed to operate with a nominal supply spanning from 1.2 V down to 0.7 V without stacking issues, i.e., maintaining proper DC biasing. Furthermore, an implementation using low-voltage devices and the intrinsic biasing strategy of the circuit allow for a low current draining with operating point establishment, which otherwise would not be possible for lower supply voltages, e.g., below 1.8 V, using the standard VC approach.

The circuit in Fig.3.4 employs two PMOS devices in a CS configuration and two folded NMOS devices in a CD configuration, combined with differential input and output. This structure is biased in current by the top and bottom current sources. The gain of the fully-differential folded VC circuit is given by (6), neglecting the body-effect. Considering that gmCS and gmCD » (gdsCD$^{\circ}{}^{\circ}$gdsCS$^{\circ}{}^{\circ}$ gdsBN) is a fair approximation of the gain in (6), the expression can be simplified into (7).

When comparing a basic source-follower device with the folded voltage-combiner, the advantage of the latter is clear: the gain can be made higher by properly sizing gmCS > gmCD. The GBW and the output resistance of the folded voltage-combiner structure are given by equations (8) and (9), respectively, and the thermal input-referred noise equation considering exclusively drain-source contributions, can be given as in (10), where k represents the Boltzmann constant, T is the temperature and γ is a function of basic transistor parameters and bias conditions of the devices.

3.2. Standard VC biased CMOS inverter-based OTA

The optimization results of the OTA shown in Fig.3.2 a represented in this sub-section. After an evolution of 128 individuals through 150 generations, the results are obtained in the form of the Pareto Optimal Fronts (POFs). It is worth noticing that the achieved performances are post-layout extracted (XRC) results after 6 h in an Intel-Xeon-CPU E5-2630-v3 @ 2.40 GHz and 64 GB of RAM workstation, using 8 cores for parallel simulation. This process automatically generated layouts for every solution presented, i.e., all have ready-to-fabricate layouts. Gain values between 56 and 50 dB, FOM values between 1278.7 and 1842.3 MHz pF/mA and areas between 0.062801 and 0.08608 mm2 have been achieved. The sizing of an intermediate circuit solution. This OTA drains approximately50μAfroma2Vsupplysource, with again above53 dB and a GBW value around 81 MHz

3.3. Folded VC biased CMOS inverter-based OTA

The results of the optimization procedure of the OTA shown in Fig.3.5 are presented in this sub-section. This circuit is designed for low voltage supply sources thus prior optimization at sizing level only shows the potential of the topology. A throughout exploration in depth is carried out, showing that the circuit is able to properly operate under voltage supplies down to 0.7 V, considering the UMC 130 nm technology node. This procedure considered an evolution of 256 individuals through 3000 generations. Accurate model-based simulation results show FOMs of 2875, 2867 and 2324 MHz pF/mA, or gains of 67, 65 and 60 dB, under 1.2, 1 and 0.7 V, jointly.

A layout-aware optimization is carried out for the folded VC biased CMOS inverter-based OTA, supplied by a 0.7 V source. After an evolution of 128 individuals through 200 generations, the results are obtained in the form of the POFs depicted, after 10 h. Again, all solutions have feasible and ready-to-fabricate associated layouts, automatically designed with AIDA. The achieved performance metrics are

Post-layout XRC results with a high-fidelity index since technology model cells are used while the extraction is carried out using Mentor Graphics' Caliber. Gain values between 60 and 50 dB, FOM values between 2091.5 and 1013 MHz pF/mA and occupied areas between 0.0822769 and 0.112300 mm2 have been achieved with this topology and optimization procedure. The sizing of an intermediate circuit solution is detailed in Table 2. This circuit solution drains approximately 36 μA from a 0.7 V voltage supply source, with a gain above 50 dB and a GBW of approximately 76 MHz for a 1 pF load. This optimization considered the maximization of the gain, competing with the maximization of the FOM as in (12), and the minimization of the active-area, which has been estimated considering the active-area of the devices and the input and output pads, following the previous case without any loss of precision.

4. Proposed Work

4.1. Basic Inverter-Based OTAs

The first inverter-based OTA was proposed by Nauta in 1989 [2,9]. Figure 4.1 shows its schematic. It is made of six inverters, has only four nodes, and is completely symmetrical. It is composed of two parts: the Trans conductor itself (inverters A) which is responsible for the OTA transconductance, and the common-mode rejection circuit, made of inverters B and C. This topology is essentially attenuated positive feedback that works differently for differential and common-mode signals. Inverters C are cross-coupled and result in positive feedback for differential signals attenuated by inverters B, which are connected as loads. For common-mode signals, both inverters B and C are seen as loads by inverters A.

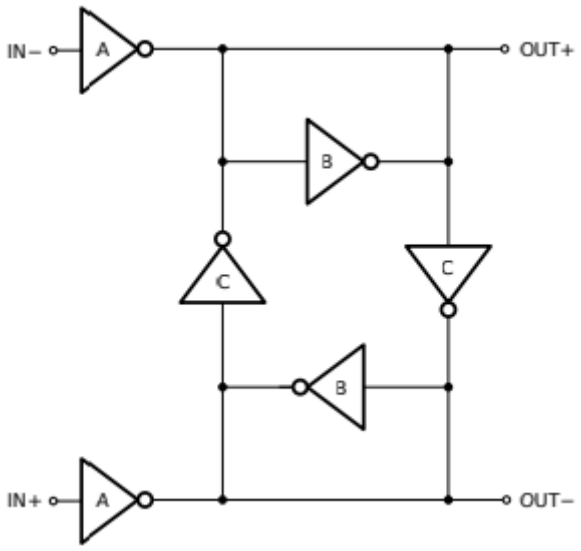


Figure 4.1. Nauta (N) OTA circuit diagram

The small-signal low-frequency (DC) differential AVDF and common-mode AVCM voltage gains are functions of the inverters transconductances GmX and output conductance's GoX. Considering that the equivalent transconductance (output conductance) GmX(oX) of parallel inverter cells is proportional to the

transconductance (output conductance) of a single inverter cell Gm0(o0) and the inverter cell voltage small-signal voltage gain is equal to AV, then for the special case where the inverter cell multipliers A = 2B = 2C

Ideally, GmC should be designed to be slightly larger than GmB, so that we would have GmC − GmB = GoA + GoB + GoC and infinite differential voltage gain. To achieve this, inverters B and C could be designed with different sizes or biased independently. However, the inverter transconductance is not linear and voltage gain would be only infinite for a point in the curve. Even if the inverter transconductances were perfectly linear, any variation due to PVT or local mismatch would decrease voltage gain or lead to hysteresis. For this reason, voltage gain improvement by this positive feedback technique is limited by a few dB, even using automatic biasing circuits. As an alternative to the Nauta OTA, Figure 4.2a shows another inverter-based OTA based on the CM input feedforward rejection technique. This OTA topology main advantage is its output voltage headroom, as the Nauta topology greatly reduces it, even considering that the inverter cell output voltage headroom is almost rail-to-rail, the common-mode input signal is extracted from the differential signals using inverters B and C. Then, this signal is fed forward to each output with inverted polarity, thus cancelling the common-mode component of which is also amplified by inverter A, leaving the remaining input output differential signal. However, this common-mode cancellation is not perfect, as it is limited by the finite inverter voltage gain.

In this case, the common-mode voltage gain in the intermediate node is also unity. Other inverter multiplier ratios can be used but this one was selected so that it can have the same differential and common-mode voltage gain as the (N) OTA. Additionally, this OTA could be designed with A B for maximum power efficiency as it does not affect either AVDF and AVCM. However, this could lead to severe voltage offset problems due to transistor local mismatch.

A variant of Barthelemy OTA is the Vieru OTA as depicted in Figure 4.2b. It is composed of the same number of cells and nodes, but the common-mode signal path direction is reverted so that the CM signal is fed back to the input. This topology is not advantageous alone, once it depends on the OTA input load. However, it can be useful as a cascaded two-stage OTAs.

Another approach is to adopt a CM feedback technique which can be used in a standalone single-stage amplifier, as proposed in Mafredini by adding another node so that the output CM signal is fed back to the output nodes without going through the input nodes as done in the Vieru OTA topology. Figure 8 shows the Manfredini OTA. As in the Nauta OTA the output signal is fed back to itself but without positive feedback. As in the Vieru OTA, the output common signal is extracted from the differential output signals by inverters B and C. Inverters D and E invert the common-mode signal polarity, and inverters F feed the common-mode signal back to the output canceling it. For differential signals, the circuit is ideally transparent. This common-mode technique is limited by the inverter cell low-frequency voltage gain, as shown in the small-signal analysis

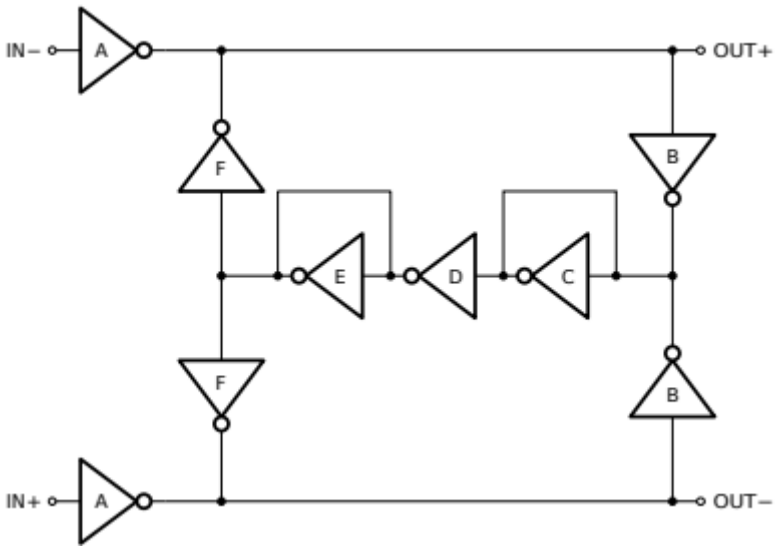


Figure 4.3. Mafredini (M) OTA circuit diagram, the small-signal differential and common-mode voltage gains are similar to the previous topologies, once the common-mode path voltage gain is unity. Other inverter multipliers could be used to improve either the common-mode rejection or power efficiency, but this would result in the detriment of other OTA performance.

Hybrid Inverter-Based Amplifier Topologies

The previously presented OTA topologies can be merged to create hybrid versions. The OTA shown in Figure 4.4 combines the common-mode feed forward and attenuated positive feedback techniques from Barthelemy and Nauta OTAs. The Barthelemy /Nauta (B/N) small-signal low-frequency voltage gains are

For the special case, where (D/A) = (B/2C)

As result, in this proposed B/N OTA, the common-mode voltage signal is further attenuated by a factor proportional to the inverter voltage gain. This is great for applications that need high common-mode rejection such as instrumental and biomedical signal amplifiers. However, B/N OTA suffers from the same drawback seen in the Nauta OTA; the output voltage excursion reduction.

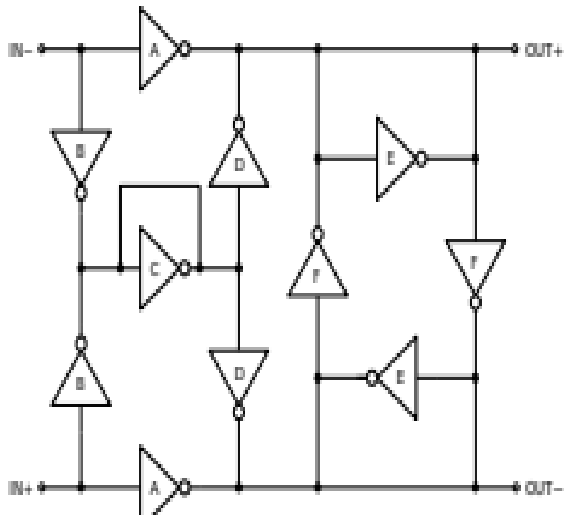


Figure.4.4. Barthelemy/Nauta (B/N) hybrid OTA circuit diagram

A solution to keep the high common-mode rejection while having a reasonable output voltage signal headroom is to combine the Barthelemy and Manfredini (B/M) OTA topologies. Figure 4.5 shows the second hybrid topology, which uses both CM input feedforward and output feedback techniques, by sharing the CM signal path to save area and power. Then, the B/M small-signal low-frequency voltage gains are. As seen in B/N, in B/M OTA the common-mode signal is attenuated by approximately the inverter voltage gain. This topology has the same number of intermediate nodes as the Manfredini OTA; however, it needs extra inverters, increasing this way its power consumption and the silicon area.

The basic and hybrid single-stage inverter-based OTAs seen so far are inherently stable once they do not have intermediate nodes in their differential signal path and there is no voltage gain in their common-mode signal path. Multi-stage amplifiers, on the other hand, need a frequency compensation circuit, if they are used within negative feedback networks. One of the simplest frequency compensation circuits is the Miller compensation capacitor, which implements the pole-splitting technique, which is normally followed by a zero-cancelation technique, mostly implemented with resistors. Another alternative is to use the so-called Nested Transconductance-Capacitance Compensation technique (NGCC), which is an approach that replaces the zero-canceling resistor with an active transconductance, and can be adapted to fully differential two-stage OTAs

n = 2.where gmA and gmB are the transconductance, goA and goB are the equivalent conductance of the first and second nodes across the Miller capacitor Cc, respectively. Figure 4.6 depicts a two-stage amplifier comprised of two distinct Nauta stages with different strengths, and a Gm-C feed-forward compensation

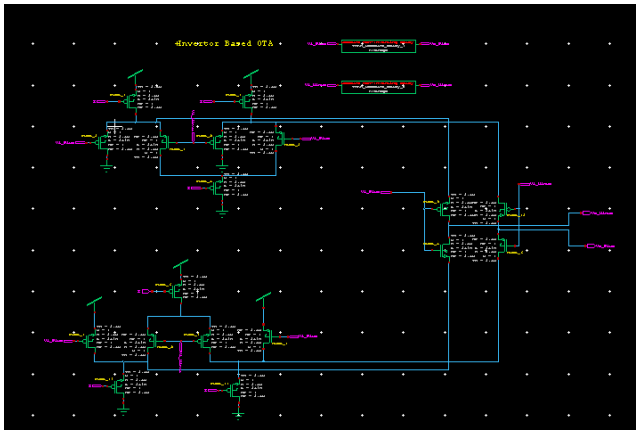
path as described by Equation (21) and in the Figure 4.6. Given that all the design requirements to keep the circuit stable are considered according to Equation (21), then the Nauta/Nauta (N/N) low-frequency small-signal gains are and, for the special case where A = 2B = 2C, D = 2E = 2F, and 2A = D = G

therefore, the differential voltage gain is proportional to two cascaded amplifiers, and the common-mode voltage gain is further attenuated as an effect of the feedforward path used for frequency compensation. However, the N/N OTA also suffers from the same degraded output voltage excursion of standalone N OTA.Variants of N/N are also herein proposed considering the current advances in inverterbased OTA designs. Therefore, The N/N second stage can be replaced by the Vieru OTA from Figure 4.2b, which implements output common-mode feedback to the inner nodes, as shown in Figure 4.8. Considering the circuit is stable, the Nauta/Vieru (N/V) OTA have as low-frequency gains for the differential and common-mode signals, respectively.

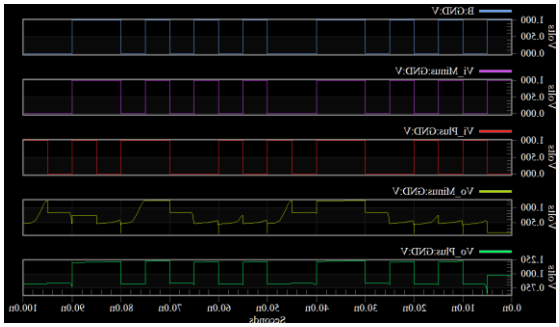
For A = 2B = 2C = G, 2E = F, and 2A = D = H

5. Results And Discussion

5.1. Schematic Diagram for Invertor based OTA design



5.2. Output for Invertor based OTA design



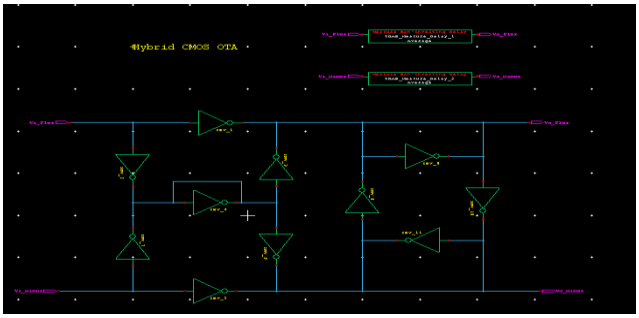
5.3. Power Results for Invertor based OTA design

```
V1 from time 0 to 1e-007
Average power consumed -> 9.237712e-004 watts
Max power 5.571528e+000 at time 4e-008
Min power 5.538570e-004 at time 4.00609e-008
```

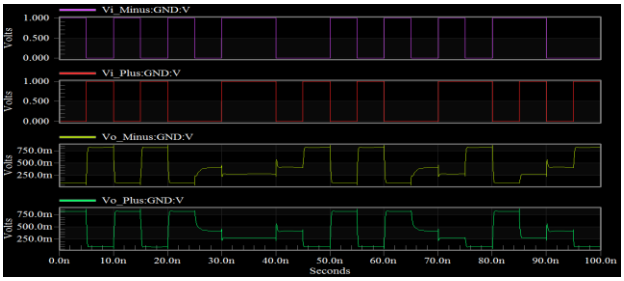
5.4. Delay results for Invertor based OTA design

```
Measurement result summary
   TRAN_Measure_Delay_1 =  121.9300p
   TRAN_Measure_Delay_2 =  121.9854p
```

5.5. Schematic Diagram for Hybrid Invertor based OTA design



5.6. Output for Hybrid Invertor based OTA design



5.7. Power Results for Hybrid Invertor based OTA design

```
Power Results

V1 from time 0 to 1e-007
Average power consumed -> 7.997866e-005 watts
Max power 5.527753e+000 at time 3e-008
Min power 9.139906e-011 at time 1.11e-012
```

5.8. Delay results for Hybrid Invertor based OTA design

```
Measurement result summary
   TRAN_Measure_Delay_1 =      not found
   TRAN_Measure_Delay_2 =   -1.7223n
```

5.9. Parameters Comparison

S.No	parameters	Existing Method	Proposed method
1	Power in Watts	9.24E-04	6.59E-05
2	Delay in ns	1.22E-07	1.72E-09
3	transistor Count	22	24

6. Conclusion

Hybrid topologies merge those techniques and share paths, to save power and area while retaining the output swing of those alternative basic topologies. Using both Barthelemy and Nauta techniques increases the common-mode rejection; however, it also decreases the output voltage excursion, which is not a problem for the Barthelemy/Manfredini hybrid OTA. Single-stage inverter-based OTAs output voltage excursion does not include the supply voltages, but their multi-stage counterparts have rail-to-rail output voltage excursion. Finally, feedforward active frequency compensation makes two-stage amplifiers stable, and as a bonus, it can also improve common-mode rejection.

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