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"Study of Performance Enhancement and Optimizing Various Parameters of Lateral IMOS"

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Abstract— MOSFETs have been the most popular devices for past five to six decades because of its excellent scalability. But during past few years semiconductor industry is facing various challenges related to scaling. These challenges are related to several fundamental and practical of underlying physics of device such as leakage currents, mobility, reliability, sub threshold swing and in turn degrading the device performance. MOSFET is most uses in inverter, power amplifier and switching devices for electronics. As IMOS will be a good alternative for small scale devices due to its good electrical performances. Its low sub threshold swing property will be very beneficial for high switching devices but this device faces a very critical issue of high operating voltage to operate in ON state and as device is scaled down chances of band to band tunneling is high which increase the leakage current in the device. This paper focus on the problem to reduce the required supply voltage and thresh-old voltage by optimizing its various physical parameter like its Gate length, Intrinsic length and Oxide thickness etc. Apart from this we propose some novel structure of device called Ultrathin IMOS and Silicide based UTIMOS based on the optimization result. These devices have better performance as compare to conventional LIMOS structure.In this paper, a detailed analysis has been done for Lateral impact ionization MOS.

Keywords—LIMOS (Lateral Impact MOS), G for gate,D for Drain, S for Source ,SUTIMOS (Silicide based Ultrathin Impact Ionization MOS),UTIMOS(Ultrathin Impact Ionization MOS).

1.0 INTRODUCTION

MOSFETs have been the most popular devices for past five to six decade's because of its excellent scalability. Therefore, researchers accelerated its scaling as it showed excellent performance with scaling. But during past few year semiconductor industry is facing various challenges related to scaling, as per ITRS the scaling of CMOS device and its process technology is expected to end at the 16-nm node by the year 2019.These challenges are related to several fundamental and practical of underlying physics of device such as leakage currents, mobility, reliability, sub threshold swing and in turn degrading the device performance. To solve these issues, researchers came up with new ideas like use of innovative fabrication techniques, new device structures were proposed, new alloy materials like SiGe, Strained Si, GaAs, Silicide etc are used to fabricate the device and moreover innovative and novel device concept are proposed.

1.1Lateral Impact Ionization MOS (LIMOS)

1.1.1 Device structure and operating principle

The schematic of lateral IMOS is shown in Figure 1.1.1 IMOS is a gated p-i-n diode, unlike conventional MOSFET it has the source and the drain with opposite kind of dopants and there exists an i-region which is not completely overlapped by the gate. The purpose of i-region is to induce avalanche breakdown between the source and channel and to suppress unwanted band-to-band tunneling. Because,

carrier are induced entirely on the intrinsic length and the gate length both make the path between source and drain so that channel region of IMOS is defined as the summation of intrinsic length and gate length.

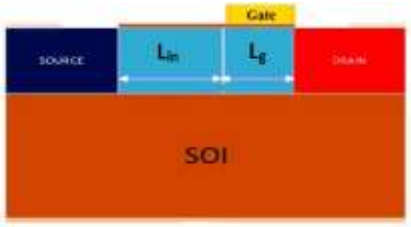


Figure 1.1.1: Structure of LIMOS.

1.1.2 Simulation results and discussion

To obtain accurate device simulations for impact ionization device, simulations included all models used to describe common device behavior including both impact-ionization and the band-to-band tunneling model, along with the band gap narrowing model. Shockley-Read-Hall and Auger recombination model at 300K are also used for accountability of leakage current. Table 1.1.2 enlists the various device parameters used during LIMOS device simulations and optimization.

Table 1.1.2: Parameters used during the device simulation.

Parameters	LIMOS structure
Channel length (L_{ch})	100nm
Gate length (L_g)	60nm
Intrinsic length (L_{in})	40nm
Doping N_d	$10^{20}cm^{-3}$
Doping N_a	$10^{20}cm^{-3}$
Substrate doping N_{sub}	$10^{15}cm^{-3}$
Gate thickness (t_{ox})	3nm
Gate work-function	4.17eV
Gate bias	0V to 2V

1.1.3 Doping profile

IMOS device has different dopant in source and drain region to support the p-i-n diode structure. Figure 1.1.3.1 and Figure 1.1.3.2 shows the doping pro le of N-type Lateral IMOS device.

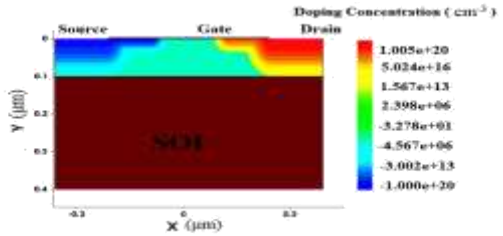


FIGURE 1.1.3.1: DOPING PRO LE OF N-TYPE LIMOS

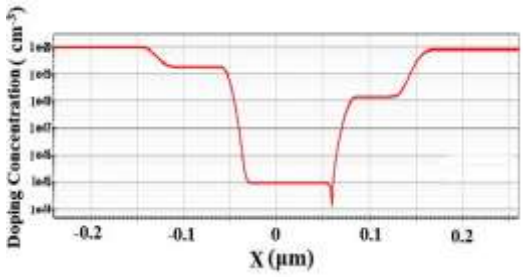
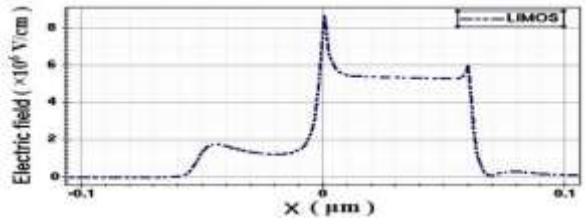


Figure 1.1.3.2: Doping pro le variation along X-axis.

1.1.4 Electrostatic potential and electric field

IMOS, when gate voltage is applied most of the voltage is dropped across the intrinsic region due to the high resistivity. So that a very high electric field is observed in this region and this will cause the impact ionization process in the device. Electrostatic potential pro le and electric field prolie of device are shown in Figure 1.1.4.1 and Figure 1.1.4.2.



In figure 1.1.4.1: Potential pro le for LIMOS.

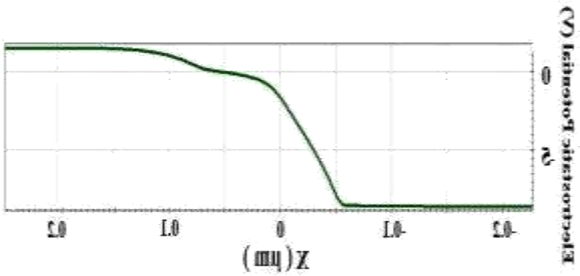


Figure 1.1.4.2: Electric field variation along X-axis.

1.1.5 Impact ionization rate

As electric field crossed the value of critical electric field of material, Impact ionization process of carrier generation started. Rate of generation of carriers is maximum at channel region of device and reached the maximum value up to 9e + 30. Figure 1.1.5.1 and Figure 1.1.5.2 shows the impact ionization profile and variation in impact ionization

rate along the x-axis.

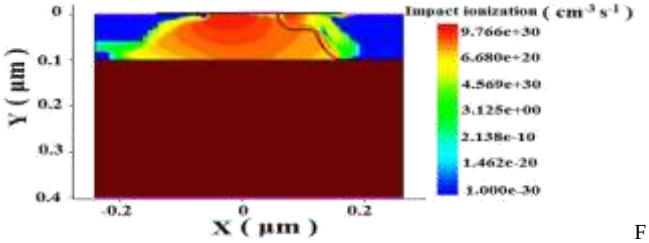


Figure 1.1.5.1: Impact ionization rate of LIMOS.

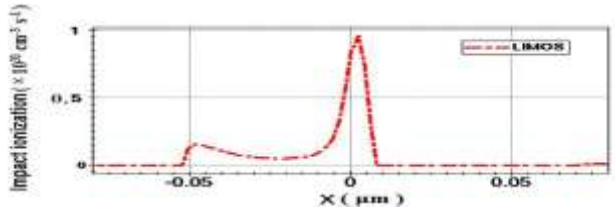


Figure 1.1.5.2: Impact ionization pro le along x-axis.

1.1.6 Current voltage characteristics

In this section by using above mention model, n-type IMOS structure is simulated. Device parameters such as channel length of 100 nm and oxide thickness of 3 nm are used so that short channel effect like DICE and GIBL can also be analyzed. Other parameters are same as mention in Table 1.1.2 . The n channel IMOS input I-V characteristic for n-channel device is shown in Figure 1.10. Initially at lower gate voltage very low leakage current is flow but as gate voltage reaches at particular voltage called threshold voltage(V_{th}), avalanche breakdown occurs and suddenly a number of charge carriers available at channel region which cause the flow of current between source and drain.

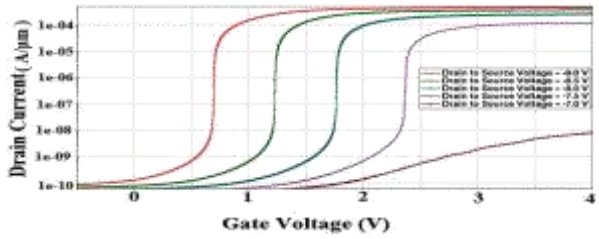


Figure 1.1.6.1: Simulated input I-V characteristics of n-type LIMOS.

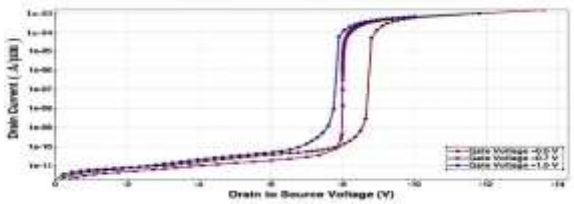


Figure 1.1.6.2: Simulated output I-V characteristics of n-type LIMOS.

1.2 PARAMETER OPTIMIZATION OF LATERAL IMPACT IONIZATION MOS

better appreciation, various LIMOS device performance parameters are evaluated. Figure 1.2.1 shows the LIMOS architecture used for the simulation modeling and optimization. It is a silicon-on-insulator (SOI) implementation. The parameters such as drain current (I_d), On-current (I_{on}), O -current (I_{off}), On-current to O -current ratio (I_{on}=I_{off}), DICE, GIBL, sub-threshold slope (SS), and transcon-ductance (g_m) for the LIMOS are investigated using Synopsys TCAD Sentaurus simulator version VG-2012.06 [7]. various device parameters used during LIMOS device simulations and optimization.

1.2.1 Device structure and simulation

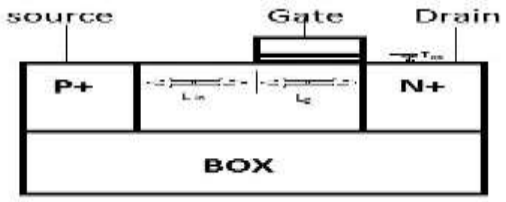


Figure 1.2.1: Structure of LIMOS

Table 1.2 : Parameter used during device simulation.

Parameters	LIMOS structure
Channel length (L_{ch})	100 nm
Gate length (L_g)	20, 50, 60, 70 & 80 nm
Intrinsic length (L_{in})	80, 50, 40, 30 & 20 nm
Doping N_d	10^{20} cm- ^{3}
Doping N_a	10^{20} cm- ^{3}
Substrate doping N_{sub}	10^{15} cm $^{-3}$
Gate thickness (t_{ox})	3 nm
Gate work-function	4.17 eV
Gate bias	0 V to 2 V

1.3 ULTRATHIN IMPACT IONIZATION MOS

1.3.1 Device structure and simulation

UTIMOS has very much lower breakdown voltage hence its operating voltage reduced to a great extent. Simulation results claims that UTIMOS has much better device performance parameters as compared to LIMOS.

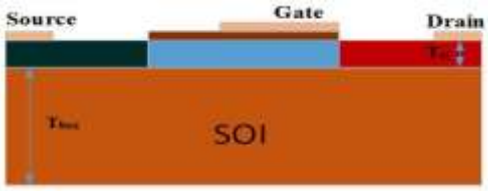


Figure 3.1: Structure of UTIMOS.

Table 3.1.1: Parameters used during the simulation of UTIMOS structure

Parameters	LIMOS structure

Channel length (L_{ch})	100 nm
Gate length (L_g)	60 nm
Intrinsic length (L_{in})	40 nm
Silicon Thickness (T_{si})	15 nm
SOI Thickness (T_{box})	100 nm
Doping N_d	$_{10}20$ cm^{-3}
Doping N_a	10^{20} cm^{-3}
Substrate doping N_{sub}	10^{15} cm^{-3}
Gate thickness (t_{ox})	3 nm
Gate work-function	4.17 eV
Gate bias	0 V to 2 V

1.4 SILICIDE BASED ULTRATHIN IMPACT IONIZATION MOS

After optimization of LIMOS and introducing new device concept of UTIMOS, there are still some chances to achieve lower operating voltage by using new material engineering. In this chapter, A novel device concept called Silicide based UTIMOS (SUTIMOS) is proposed. This device claims better device performance in terms of reduced operating voltage, lower threshold voltage and higher I_{on}/I_{off} ratio.

1.4.1Device structure and simulation

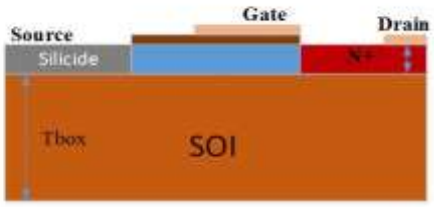


Figure 4.1: Schematic of n-type SUTIMOS.

Table 1.4.1: Parameters used during simulation of SUTIMOS structure

Parameters	LIMOS structure
Channel length (L_{ch})	100 nm
Gate length (L_g)	60 nm
Intrinsic length (L_{in})	40 nm
Silicide length	200 nm
Doping N_d	10^{20} cm -3
Gate thickness (t_{ox})	3 nm
Gate work-function	4.17 eV
Gate bias	0 V to 2 V

1.5 FUTURE WORKS AND SCOPE OF THE WORK

Application level analysis of UTIMOS and SUTIMOS structure such as inverter designing can be done using mix mode simulation mode of Sentaurus device simulator. A comprehensive analysis and comparison of transient and RF behavior of all the three structures can be done.

1.6 CONCLUTION

In this paper, a detailed analysis has been done for Lateral impact ionization MOS. First we saw the impact of some physical parameter on the performance of device and concluded that betterment should be done in device dimension to achieve the best results. The L_g=L_{in} ratio should be near to one for working as a perfect IMOS device. Oxide thickness is another parameter which controls the leakage current in the device so it must also be tuned to achieve better result in terms of higher I_{on}/I_{off} ratio.

A brief study was done for the AC transient analysis of LIMOS device and its dependency on operating voltage and it was seen that IMOS has good capability to operate in high frequency applications. To reduce operating voltage of LIMOS, novel device structures called UTIMOS and SUTIMOS has also been proposed and a comprehensive analysis and comparison of all three structure has been carried out. Simulation results claims that SUTIMOS has lower operating voltage with high I_{on}/I_{off} ratio and steep subthreshold slope of 1.372 mv/dec.

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