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32nm Based High-Speed Low-Power Calibrated Flash ADC comparator with improved ENOB

[1]P.Chandrayudu, [2]P.Tejashwini
[1]II M.Tech VLSI SD Student, CR Engineering College, Tirupathi, Chittoor (Dist) A.P, India,
[2]Assistant Professor of ECE Dept., CR Engineering College, Tirupathi, Chittoor (Dist) A.P, India,
[1]chandu.chandra409@gmail.com [2]tejaswini.412@gmail.com

Abstract

with this document, we have proposed a low power high speed CMOS Comparator using Dual Mode Logic (DML) for Flash type Analog to Digital Converter, the simulation model of DML based CMOS logic simplification is to identify a system that improves the hardware utilization rate from 57.14% to 100% by improving the delay and power consumptions occurred in data converter circuits. The proposed technique whose layout simulation with extended DML logic is implemented and its performance characteristics are studied using Microwind simulator

Key Words:

CMOS Comparator, Flash-type ADC, DML, performance characteristics.

I.Introduction

For current trends and swift in technology numerous ADC architectures for low power application are fashioned. Especially some requirements designed with deep sub micron technology it is always a greedy desire to have a good resolution, having high speed and consumes low power and midrange resolutions are always on a hunt. But it is familiar that the CMOS implementation of ADC for wideband applications depends mainly on achieving a very small input capacitance or large bandwidth at the desired accuracy is always a critical issue. Therefore demanding to reduce the input capacitance supplementary side effects are accompanied by huge offset voltage, and the input capacitance directly trades with the exactness. In addition, since necessary input calibration accuracy is less than quite a few mV without the preamplifier, so high-precision DACs are necessary for all comparators. However, high-precision DACs circuits always consume a large amount of power and data conversion becomes delayed as per target conversion time, as a consequence the data converters are suffering with drawbacks of Comparator circuits being implemented with ADC and this become more critical if the ADC operated with more speed , this leads to a great challenge to high speed data converters with low-power characteristics.

To promote low power applications of data converters, Comparators must model in such a way that it can support for a good trade-off between speed, area and power consumption. The VLSI architectures for such comparator is developed as followsThe VLSI architecture of low power, high speed comparator for the CMOS data converter is considered to be implemented along with Dual Mode Logic (DML) . It is implemented in 32nm CMOS technology and its highly recommendable for Flash type ADCs.

II.Modeling OF CMOS comparator unit with DML

Dual Mode Logic (DML):

DML gates are existing with two possible topologies: 1) Type A and2) Type B, as shown in following figure consequently. In the static mode of operation, the transistor M1 is turned off by

smearing the high Clk signal for Type A and low Clk for Type B topology. So, the gates of both topologies operate in like way to the static logic gate, which now is a standard CMOS operation. To activate the gate in the dynamic mode, the Clk is allowed, allowing for two discrete phases: 1) pre-charge and 2) evaluation. Throughout the pre-charge phase, the output is charged to VDDin Type Agates and discharged to GND in Type B gates. Through evaluation, the output is assessed allowing to the values at the gate inputs. DML gates demonstrate a very robust process in both static and dynamic modes in process variation at low supply voltages. The toughness in the dynamic mode is mainly achieved by the in-built active restorer (pull-up in Type A/pull-down in Type B) that also allowed glitch sustaining, charge drip, and charge distribution. It is also exposed that the suitable sizing methodology is the crucial factor to achieve fast operation in the dynamic mode. Differing to CMOS gates, every DML gate can be executed in two ways, only one of which is effective. The ideal topology is such that the pre-charge transistor is positioned in parallel to the stacked transistors, i.e., NOR in Type A is favored over NAND, and NAND in Type B is desired over NOR. In this event, the evaluation is executed through the parallel transistors and hence it is faster. The DML log elements are shown in Figure1.

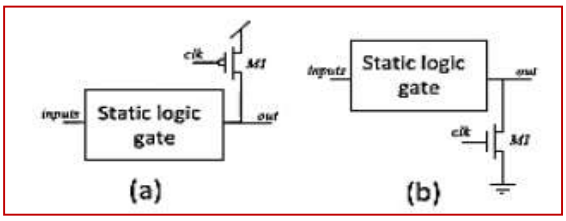

Figure1: DML Topology

Existing architecture:

Generally, the nonlinearity of a flash ADC more often than not results from the random static and dynamic offset in the comparators. The offset in comparators becomes not as good as when the designed size of input transistors is small for saving power. Therefore, many digital calibration methods with good calibration range and accuracy are considered. Most of them augmented the infinitely small capacitance in the ac signal path because the effect of the extra capacitance will gives rise to extra power to retain the same data rate. As the prerequisite for input calibration precision is less than several mV without the preamplifier, high-precision DACs are essential for all comparators. But these DACs always put away a large amount of power and this is not favourable to the design of low-power characteristics. According to above reasons, we propose a simple and useful comparator as shown in the firure2.

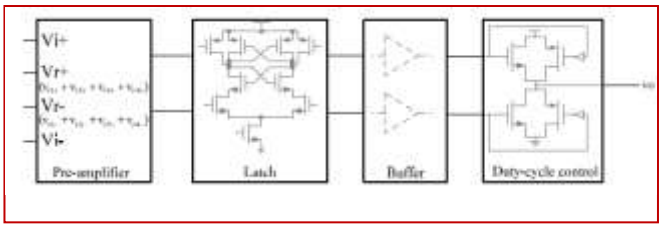

Figure2: Proposed Architecture

Improved architecture with DML technique

The proposed technique combines with more sophisticated Dual Mode Logic (DML) to get rid of power dissipation problems at deep submicron era of ADCs and so as to improve the speed of operation. And the proposed architecture is shown in the figure3.

block diagram

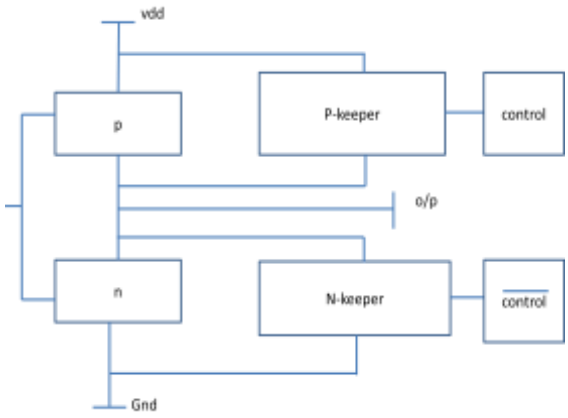

Figure3: Proposed Architecture with DML

Back-End Modeling:

The logic functions of proposed system can be realized by various logic families. Each logic family optimizes one or more electrical performance, such as area, power, or speed, from circuit topology perspective instead of architecture perspective. Since it is familiar that the key CMOS ingredients are inverter structures and with these structures target blocks are designed

with CMOS 32 nm technology as both units must combine each other and counterpart each drawback by other one the final target may suffer with switching delays and path sensitization delay to overcome this Dual Mode Logic has been proposed which drastically increased the speed of operation with reduced power consumption. The lay out designs are as shown in figure4 and figure5.

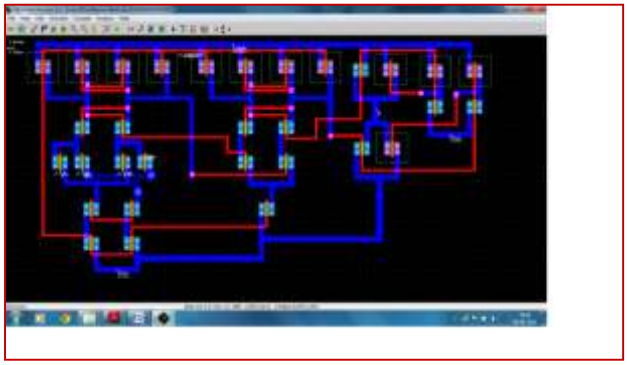

Figure4: Comparator layout design without DML

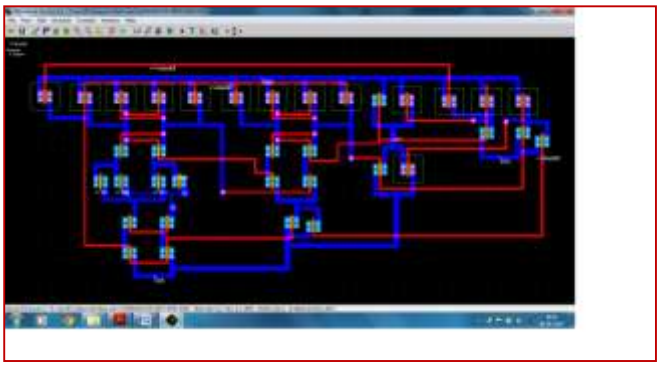

Figure5: Comparator layout design with DML

III.SIMULATION RESULTS

The physical design layout results are observed separately with and without implementation of DML logic, it is noticed that at some instance of simulation time the power and time delays are greatly improved with the implementation of Dual Mode Logic the various results are shown in figure6 and figure7.

Figure6: Simulation output – Comparator without DML

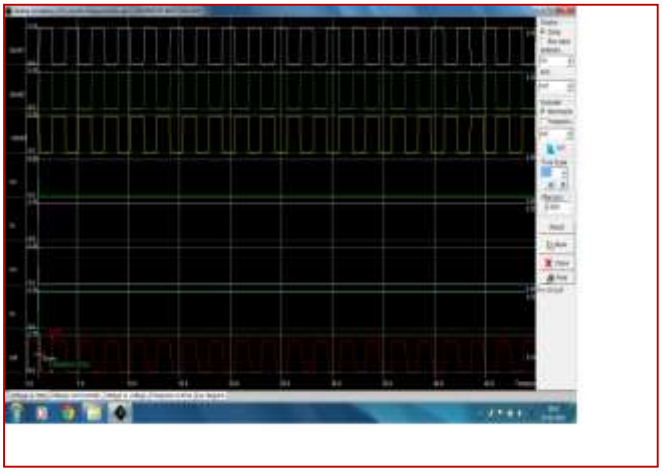

Figure7: Simulation output – Comparator with DML

The performance metrics are summarized in the following Table1.

TABLE1
SUMMARY OF PERFORMANCE REPORT

parameter	Comparator without DML	Comparator with DML
Power	1.533 µW	1.500 µW
Delay	230 Ps	169 pS
I_{dd} Max.	0.026 mA	0.025mA
V_{dd} Max.	0.35 V	0.35 V
W/L	1/0.04	1/0.04

IV.CONCLUSION

This paper analyzes the need for high speed; low power VLSI modeling of DML based Comparator Design for flash type ADCs especially for deep submicron technologies. The proposed work eliminates the problem of unwanted power dissipations at comparator circuits of data converters. The relevant layouts are analyzed and various physical

parameters are studied at 32 nm Technology. Such designs are suggested to exhibits a competitive performance with current work.

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AUTHORS

PENETI.CHANDRAYUDU received his B.Tech degree in Electronics & Comm., Engineering from Chiranjeevi Reddy Institute of Technology College Ananthapuram (A.P), India, in the year 2012. Currently pursuing his M.Tech degree in VLSI System Design at ChadalawadaRamanamma Engineering College,Tirupati(A.P), India.. His area of research Includes in low power vlsi design.

Puchala Tejashwini is currently working as Associate professor in the Dept.,of elcetronics&communication engineering at Chadalawada Ramanamma Engineering College, near Tirupati, India. She has nearly 04 years of teaching experience. She extensive education includes B.tech. From Chadalawada Ramanamma Engineering College, Tirupati, India, plus M.tech. in Seetham Engineering College, Thirupati, India. In addition to this, She is making research in the field of Communication System Process.