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pGate: An Introduction to A Novel Universal Gate and Power Drop Calculation of QCA circuits

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Abstract: ***Quantum Dot Cellular Automata is an emerging nanoscale transistorless computational technology, which permits the logic gate designing schemes to be tinier and extremely faster by dint of high-speed quantum tunneling. The tunneling occurs at a speed of light, which causes the circuit operative speed very faster and operating time in some picoseconds. In this letter one new universal gate designing technique have proposed, which is shaped with five quantum cells. This paper initially covers some basic layouts like two input pNAND and four input pNAND gate. In purpose of physical verification of the proposed pGate one 2 bit multiplexer has proposed which is implemented by 14 cells, which provides 33.70% area optimization compared to previously best reported designs. In this paper, one novel methodology of QCA circuit power drop computation have introduced with brief algorithm. Previous nine 2x1 MUX layouts have undertaken and their power drops have been calculated and provided in a tabulation manner. The commenced designs are compared with other existing techniques significantly in terms of cell uses, AUF, effective area, power dissipation etc. Proposed designs are simulated and approved by QCADesigner 2.0.3. This paper conveys a new information regarding quantum logic gate designing and power computation technique to the nanoelectronic science.***

Keywords: Universal pGate, Partial polarization, Multiplexer, Central clocking, QCA.

1. INTRODUCTION

CMOS technology has its fundamental limit in terms of device speed and power utilization in the case of several logic gates. But the technology doesn't have any limit, it always deserves the improvement and development beyond of all complications. The Quantum-dot Cellular Automata is a revolutionize invention since 1992 which permits the technology to work at or lesser than nanometer scale [1]–[5].

Quantum scale implementation of the logic gates offers the designer to work in nanometer scale, that extends the device compactness and provides lighting speed of operation through fastest quantum tunneling. One tiny quantum cell consists of two electrons within four quantum dots at each corner of the square cell, mutually separated by columbic repulsion force [2], [3]. In one quantum cell, there can have maximum two spaces for one electron to be occupied, fig. 1. Orientation and position of the electrons are controlled by providing the polarization externally. The electrons have the ability to be interchanged into the quantum dots (cavities) through thequantum tunneling. When the polarization is sufficiently applied to the electrons, then they receive the ability for tunneling through the tunnel junctions, fig. 1. These polarizations constitute different positioning of the electrons inside the existing quantum dots.

The Majority gate implementation is a basic concept in the sense of QCA technology. This gate consists of five cells. MV gate is made with two input cells A & B and one control polarization i.e. fixed polarization cell C. This FP cell is used to provide a unique polarization influence to the gate, which always remains to be constant at the time of logic operation. Mathematically the majority gate expression is written as, Y=AB+BC+CA [5], [6].

Here Y denotes the target cell, which drives the output signal. The entire characteristic of the gate is controlled by the FP cell C. If cell C is fixed with +1 polarization (+1 polarization represents the binary logic state 1), then the output comes out as, Y=A+B [2]–[7]. This proofs that the gate works as an OR gate under the influence of positive fixed polarization. In this case, the majority expression changes into an OR gate expression. The OR gate is denoted as P+(A,B) because of positive polarization influence.

On the other side, if the FP cell is polarized with negative polarization -1 (-1 represents the binary logic state 0), then the majority gate expression changes to, Y= AB. Which implies the gate behavior matches with an AND gate. This gate is mathematically noted as P-(A,B).

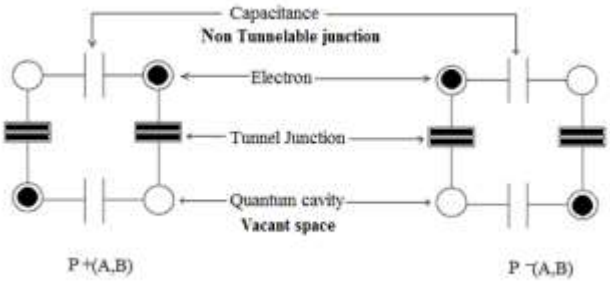

Fig. 1: Quantum cell internal architecture under different polarizations

In this paper, one new NAND and NOR gate designs are propounded along with its performance verification, which utilizes a very few cells to achieve the proper output of the universal pGate without causing any misbalance in the standard NAND or NOR output. This gate enables the easier gate designing techniques by replacing the complex design methodologies. By this gate one two input multiplexer layout is

proposed, for the better verification of this pGate performance. This MUX is simulated by the QCADesigner. The output waveform is verified according to the standard outputs of the 2x1 multiplexer circuits.

2. PROPOSED UNIVERSAL PGATES

The proposed pGate consists of six quantum cells oriented in a particular fashion to comprise the pGate. The main working method of this gate is the dual clocking. In the layout of the gate, the entire gate is under the zero clock except the driver cell, fig. 2 (a, b). The main working contrivance of this gate is to have the inverted output of AND and OR gate, to achieve the desired output as the universal gates. If the whole gate is subjected to the clock zero then positively should the driver cell (C3) to be under clock 2 and if all cells are under clock 1 then the driver cell should be under clock 3, fig. 2. This exhibits that, the clocking sequence should be skipped in nature by a single clock. The central clock of the device cell always to be skipped by 1 clock from other four cells. By this fact, this gate is nomenclature as pGate. Hence, p stands for partial, due to the partial clocking application this is said to as pGate. This establishes the dual clocking in the 5 cells majority gate. In this methodology, the driver cell is fixed under clock 2 and reaming four others are under clock 0. Systematically the input cells are connected with the two inputs A & B consecutively and the most left-handed cell is fixed with the polarization value 0.20 or -0.20. Therefore, the output of this gate comes out as a NAND/NOR gate. This gate works as a NAND gate properly within 0.20 to 0.60 polarization range and similarly from -0.20 to -0.60 works as an NOR gate, fig. 2 (a, b).

2.1 Concept of partial polarization

In the sense of QCA the quantum tunneling occurs under any particular polarization effect. It is often been found that, in the case of majority gates, AOI, UQCALG etc., the fixed polarization cells are always to be polarized with a positive or negative unit polarization. But in the proposed technique a different polarization method is used i.e. partial polarization [8]–[10]. On the above paragraphs, it is already explained that this gate works within the range of polarization i.e. ±0.20 to ±0.60. These polarizations are partially applied to configure this gate in a perfect manner for working it out as a pGate.

The concept of this partial polarization was proposed by Yuhui Lu *et al* [9]. If any sinusoidal waveform is clipped at a particular level, then the partial polarization could be achieved, as stated in that paper [9].

2.2 Proposed pNAND gate

NAND is a universal gate which has the ability to construct any combinational and sequential logic circuits. In the proposed design the base of this gate is comprised of one majority voter 5 cells gate and as an extension of one extra cell at the output which is subjected to Y, as fig 2 (a). In the sense of polarization this gate works as a NAND gate in the polarization range of 0.20 to 0.60. This gate follows this mathematical expression, $Y=\overline{AB}$, which provides the inverted output of the anding result of A, B. This simulation result shows that the maximum output amplitude is 9.51e-001 and the minimum output amplitude is -9.50e-0.001, which implies the correct output characteristics of NAND gate. It is found that in the case of majority voter gate the output waveform amplitude of NAND is entirely same with this proposed pNAND gate. Hence, no error is detected in output waveform strength.

2.3 Proposed pNOR gate

Consequently, if the polarization is reversed then the NOR output phenomena is noticed intently. NOR gate works in the reverse polarization region. While negative polarization is applied to the gate then, as an outcome the NOR gate waveform is achieved. This gate works as a NOR gate within -0.20 to -0.60 polarization range. This gate follows the mentioned expression $Y=\overline{A+B}$. Accordingly, the output signal strength of the NOR waveform emulates the previously shown pNAND output. The layout of this gate is shown in fig. 2 (b), which displays very less number of cell uses criteria in the designing field of universal gates. Below fig. 2 (a, b) shows the pGate schematics perfectly.

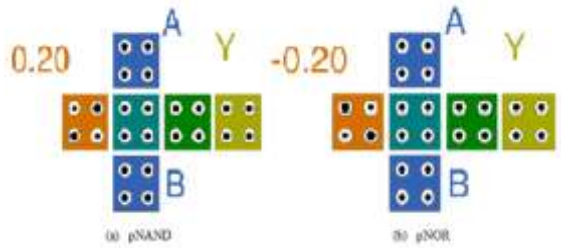

Fig. 2: pGates (a) pNAND layout , (b) pNOR layout

2.4 Proposed 4 input pNAND gate

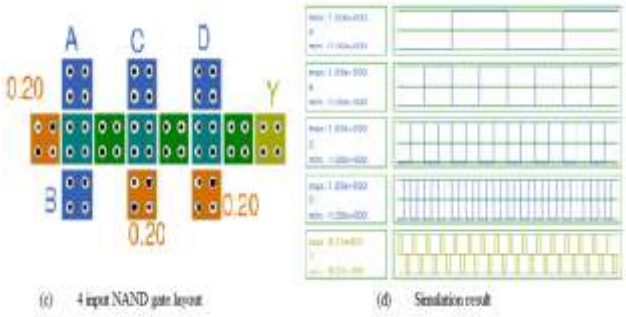

Fig. 3: (c) 4 input pNAND layout, (d) Output waveform

This combinational circuit generates the NAND output of these 4 inputs sequentially A, B, C, D. The mathematical expression is $Y=\overline{ABCD}$ which is followed by this designed 4 input pNAND gate. This gate occupies 9600 $nm^2 \sim 0.01\ \mu m^2$ area entirely associated with 14 cells upon the cell bed. This verifies the utility of pGate in the design of complex combinational and sequential circuits.

If the partial polarization (0.20) is replaced by the positive or the negative polarization (+1.00 / -1.00) then the uniformity of the NAND and NOR outputs remains unchanged. By the help of this configuration (central clocking) this is possible to design the universal gates with very efficient effective area.

3 AREA UTILIZATION AND DESIGNING EFFETCIVITY OF PGATE

This layout expresses the physical design of the pGate, which clearly mentions the all the segments with definite scaling [9]. The manually sketched layout emulates the scaling of this pGate in an apparent manner, where the whole area utilization is shown apparently along with the area of cells and their displacements from each point of the terminal wall upon the cell bed, fig. 5 [11]–[13].

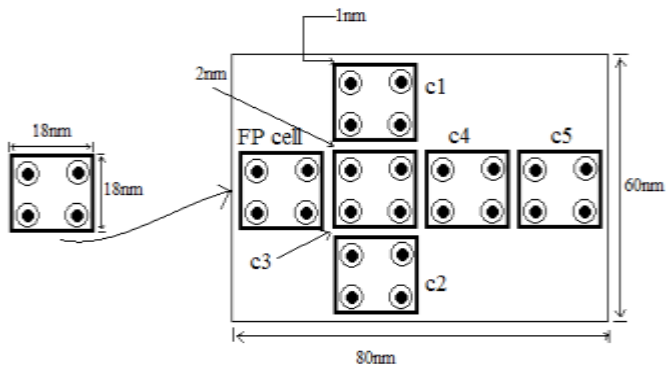

Fig. 5: Layout sketch of pGate

Area utilization factor is defined as the ratio between the total area and the area is occupied by the all used cells. Here the AUF of the pGate is mathematically calculated according to the standard rule.

The area of pNAND gate is computed below according to the fig. 5 [13]–[15].

The length of the used rectangular area is,

L= (1+18+2+18+2+18+2+18+1) = 80 nm

The breadth of the rectangular area is,

W= (1+18+2+18+2+18+1) = 60 nm

Therefore, the total area is utilized by pNAND gate is 80×60 nm^2= 4800 nm^2. This illustrates the total area uses for the implementation of this gate is given by 4800 nm^2. Similarly the area of pNOR gate is also remain be same with the pNAND gate, fig. 2, 5 [14]–[18].

This layout in fig. 5, emphasizes that the each cell occupies 18×18 nm^2 area. Hence, the total number of used cells are 6, so, the net area occupied by all the cells is 6×18×18 nm^2 Apparently 6 quantum cells are installed at their own positions which cover totally 6×18×18 nm^2 area out of 4800 nm^2. Eventually, the area utilization factor is given by AUF= $\frac{4800}{6\times18\times18}$ = 2.46

One of the important part of designing efficiency is to have the minimum area utilization by the cells upon the cell bed [19]. In that sense the area reduction is to be maximum along with every new proposals. The entire area reduction information over other design schemes are implicated in the table I.

TABLE I: COMPARISONS OF AREA REDUCTION WITH OTHER EXISTING DESIGNIGN TECHNIQUES

SEVERAL DESIGNING TECHNIQUES	USED AREAS	AREAS COMPARED TO PROPOSED GATE	AREA REDUCTION PERCENTAGE %
UQCALG [14]	72000	$15A_t$	–
AOI [15]	12296	$2.56A_t$	17.07
MV gate [14]	8460	$1.76A_t$	68.80
pGate	4800	A_t	56.73

This table explains the area reduction factors along with the percentages. The pGate is compared with other existing designing techniques, whereas the area 4800 is taken as the unit area, A_t for comparing with other mentioned designs.

In case of MV gate, the used area is (141×60)= 8460 nm^2, which is $\frac{8460}{4800}$ = 1.76, times higher than the pGate. This factor is mathematically related to the pNAND gate by 1.76 A_t [8]–[12].

Hence, after comparison, it is found that the pGate utilizes the total area which is 56.73% lesser than the Majority Voter (MV) gate. It proofs pGate can be implemented in 53.73% lesser area than the MV NAND gate, which provides sufficient positive strength in case of logic circuit designing. According to the current QCA technology MV gate is the very effective one among all the techniques like UQCALG, AOI etc. In terms of the area reduction, the pGate gets higher priority among all the designs in this field. The fewer uses of the area refers to the less circuit complexity and high efficiency of this gate. It utilizes fewer numbers of cells, which enhances the performances of the circuits by means of fastest quantum tunneling [20]–[22].

4 PROPOSED MULTIPLEXER

The NAND and NOR gate these two are widely known as the universal gates, those are able to constitute any kind of logic gates. The complex logic circuits deserve a lot of circuit elements like adders, multiplexers, DE multiplexers, latches etc., for the fulfilment of the complete need of the circuit. These all the discrete elements are very much essential for the implementation of the complex circuits [23], [24]. As well as the complexities of the circuitries are also to be lesser rather than the previous circuits along with the development of technology. In this section one 14 cells 2x1 MUX is proposed, which is implemented by the universal pGate.

This multiplexer is shaped by 14 quantum cells, by implementing the cells under suitable clocking, fig 6. Here the clock zero and the clock 2 is used according to the QCADesigner. It is found that this multiplexer circuit works within 0.20 to 0.45 polarization range, see fault analysis. The output of the designed 2x1 MUX is properly concluded with table II.

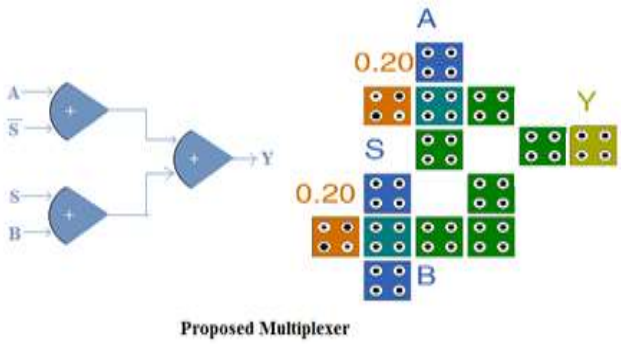

Fig. 6: Proposed 14 cells two bit pMUX

TABLE II: LIST OF OUTPUT WAVEORM STRENGTH ACCORDING TO THE POLARIZATION CHANGE OF pMUX

SR. NO	SAMPLE POLARIZATIONS	OUTPUT WAVEFORM STRENGTHS	
		MAXIMUM	MINIMUM
1	0.45	7.92e-001	-8.04e-001
2	0.40	7.93e-001	-8.03e-001
3	0.35	7.93e-001	-8.03e-001
4	0.30	7.94e-001	-8.02e-001
5	0.25	7.95e-001	-8.02e-001
6	0.20	7.96e-001	-8.01e-001
Average	0.32	7.93e-001	-8.02e-001

5 POWER DROP CALCULATION

In the case of multi clocking schemes in the cells, the power drop is a crucial factor to be calculated properly. The design strategy of the circuits is also very much dependent

upon the power dissipation in the gates [25]–[29]. The propagation of the signals requires the interconnection among the cells, whereas the intermediate gaps of the quantum cells are not filled by any dielectric. The medium remains to be air. Hence, the signal propagates through the air medium by occurring a very little power drop [11], [12].

Here some fixed conditions have undertaken in the purpose of calculation. Those conditions are as follows,

- All the used cells are completely to be identical.
- The switching time among the cells is $t_s = C^{1.16}$. C stands for the number of cell used in a linear wire [11], [12].
- The kink energy is considered as equals to the dissipated energy of tharmalized bits. $E_k \cong E_T \cong kT$
- The kink energy is taken as $E_k = 3.14577\times10^{-20}$ Jules [13].

5.1 Algorithm for computing power drop

If : **{ A** coplanar wire with maximum cells is found) **{**

Step 1: Take the maximum number of cells existing in a co-planner wire.

Step 2: Apply the above mentioned formula to find out the minimum switching time among all the cells in the wire.

Step 3: Apply this formula to find the power drop within the cells i.e. $P_d = \frac{C\times E_k}{C^{1.16}\times10^{-12}}$ Watts. **}**

Else : **{** Step 4: Take the individual cells and find out the minimum switching time. In case of individual cells the switching time should always to be undertaken in a pair of cells.

Step 5: Again compute the minimum switching time by applying $t_s = 2^{1.16}$ psec (Pico seconds).

Step 6: Find out the power drop according to the below formula;

$P_d = \frac{C\times E_k}{2^{1.16}\times10^{-12}}$ Watts. **}**

Step 7: Find the summation of all calculated powers by above procedure. This results the total power drop of any designed circuit by QCA technology.

5.2 Power drop for proposed Universal pNAND gate

The below power estimation is done for the p-NAND gate. Which provides, the total power that would be dropped at the time of logic operation, in this gate, fig. 2 (a).

Due to fixed switching time among the cells the power drop in the cells is computed by following methodology according to the above algorithm.

The power drop for four cells wire is computed as,

$P_{dC4} = \frac{4\times3.14577\times10^{-20}}{4^{1.16}\times10^{-12}} \cong 25.19$ nWatts

The power drop for reaming two individual cells is given by,

$P_{dC2} = \frac{2\times3.14577\times10^{-20}}{2^{1.16}\times10^{-12}} \cong 28.15$ nWatts

Therefore, as the step 6 of the algorithm, the total power drop is given by,

P_{dT}=25.19+28.15= 53.34 nWatts

This denotes the plenary power which is dropped due to cell to cell switching.

Hence the total number of used cells from the above calculation is given as, C_t= (4+2)= 6. Therefore, if the power drop equations of a QCA circuit are known, then the total number of cells can easily be calculated which is used in respective circuit.

TABLE III: COMPARISONS OF THE POWER DISSPATIONS AMONG DIFFERENT EXISTING UNIVERSAL GATE DESIGN TECHINIQUES

SR. NO.	EXISTING TECHNIQUES	NUMBER OF USED CELLS	POWER DROP (nW)
1	UQCALG [14]	58	393.82
2	MV gate [14]	12	95.57
4	pNAND	6	53.34

6 RESULTS AND CONCLUSION

This paper introduces one new universal gate designing methodology which is named as pGate i.e. partial gate. This paper targets the design of a novel universal gate for constructing the digital circuits efficiently against all the major problems and challenges of the quantum circuit designing. The proposed paradigm of the novel universal pGate is shaped by only six cells. The background analysis of the QCA universal gates provides that, pGate reduces down 56.73% area over the 12 cells Majority Voter universal gate. One 2 bit MUX is proposed where only 14 cells are nominated for shaping this multiplexer. This layout doesn't involve any crossover, therefore the circuit complexity reduces. In table II, all the output waveform strengths of the pMUX achieved from the simulation result are mentioned briefly. Secondly, power drop calculation methodology which is presented adequately with the proper algorithm. Table III, serves the power drops of universal gates designed by MV, UQCALG and pGate methodology. Consequently, table IV provides all the information individually of the previously proposed nine 2x1 multiplexer designs including their power drops.

TABLE IV- COMARISON WITH EXISTING 2 BIT 2x1 MUX DESIGNS

Sr. No	Previous design proposals	Effective Area E_A (nm^2)	Percentage Optimized %	O-Cost (in cell count)	Layer Used	Number of used gates	Latency	Power drop (nW)
1	In [17]	121764	-	75	1	MV-4	0.75	272.04
2	In [23]	90000	26.08	48	0	MV-3	0.75	226.52
3	In [18]	45924	48.97	41	1	MV-3	0.75	289.10
4	In [19]	40764	11.23	34	0	MV-3	0.75	292.68
5	In [11]	40714	0.12	-	-	-	-	-
6	In. [20]	28124	30.92	27	0	MV-3	0.75	225.60
7	In. [21]	22400	20.35	28	0	MV-3	0.75	209.99
8	In [22]	22400	0	23	0	MV-3	0.75	200.47
9	In [24]	19200	14.28	19	0	MV-3	0.75	175.47
10	Proposed pMUX	12000	33.70	14	0	pGate-2	0.50	120.18

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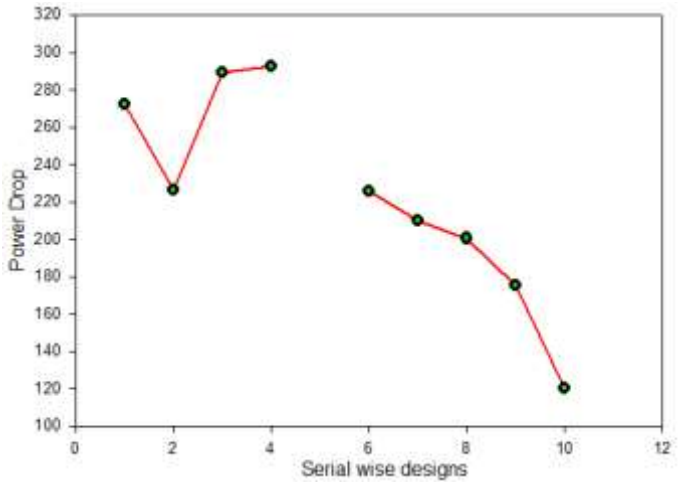
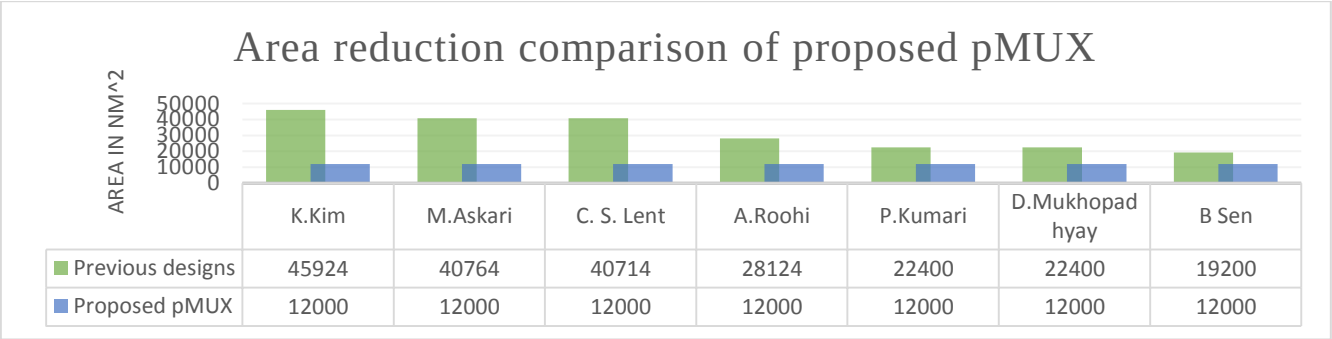


Fig. Power drop graphical illustration (data from table IV)

This table shows that, T. Teodosio *et al.* proposed the design of 2X1 MUX with 121764 nm^2 effective area. Later B. Sen *et al* proposed a MUX which had 19200 nm^2 effective area. Proposed 14 cells multiplexer design has 12000 nm^2 effective area, which is (19200–12000)= 7200 nm^2 lesser than the MUX mentioned in serial no. 9 in table IV. It is found that the pMUX requires the least area among all the mentioned designs in above table. Furthermore, the power drop through the pMUX circuit is very less as reported in table IV. This paper directs a new horizon in the emerging field of quantum-dot cellular technology for the better and prominent future of the nanotechnology science.



	K.Kim	M.Askari	C. S. Lent	A.Roohi	P.Kumari	D.Mukhopadhyay	B Sen
Previous designs	45924	40764	40714	28124	22400	22400	19200
Proposed pMUX	12000	12000	12000	12000	12000	12000	12000

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