Reduction Of Switching Activity In Noc By Using Data Encoding Schemes

Y.Supraja, R.S.Pratap Singh

P .b .r visvodaya institute of technology and science

Kavali, s.p.sr.nellore, india

Ysupraja4@gmail.com

P .b .r visvodaya institute of technology and science

Kavali, s.p.sr.nellore, india

rpsvits@rediffmail.com

Abstract*: As technology shrinks, the power dissipated by the links of a network-on-chip (NOC) starts to compete with the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces (NIs). In this paper we present a reduction of switching activity in network on chip (NOC) by using data encoding schemes. In proposed schemes there is no need to change link architecture and it will reduce transitions (i.e. nothing but switching activity contains both switching transitions and coupling transitions).due to these transitions lot of power consumption is presented at the network on chip and routers so that by using data encoding schemes we can save consumption of energy and dissipation of power without any degradation of performance .*

Keywords: Coupling switching activity, data encoding, low power, network-on-chip (NoC), power analysis.

1. INTRODUCTION:

Global interconnect length does not scale with smaller transistors and local wires. Chip size remains relatively constant because the chip function continues to increase and RC delay increases exponentially. At 32/28 nm, for instance, the RC delay in a 1-mm global wire at the minimum pitch is $25\times$ higher than the intrinsic delay of a two-input NAND fan out of 5 [1]. If the raw computation horsepower seems to be unlimited, thanks to the ability of instancing more and more cores in a single silicon die, scalability issues, due to the need of making efficient and reliable communication between the increasing number of cores, become the real problem [3]. The network on- chip (NOC) design paradigm [4] is recognized as the most viable way to tackle with scalability and variability issues that characterize the ultra deep sub micron meter era. Nowadays, the on-chip communication issues are as relevant as, and in some cases more relevant than, the computation related issues [4]. In fact, the communication subsystem increasingly impacts the traditional design objectives, including cost (i.e., silicon area), performance, power dissipation, energy consumption, reliability, etc. As technology shrinks, an ever more significant fraction of the total power budget of a complex many-core system-on-chip (SOC) is due to the communication subsystem.

In this paper, we focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales [5]. In particular, we present a set of data encoding schemes operating at flit level and on an end-to-end basis, which allows us to minimize both the switching activity and the coupling switching activity on links of the routing paths traversed by the packets.

The proposed encoding schemes, which are transparent with respect to the router implementation, are presented and discussed at both the algorithmic level and the architectural level, and assessed by means of simulation on synthetic and real traffic scenarios. The analysis takes into account several aspects and metrics of the design, including silicon area, power dissipation, and energy consumption. The results show that by using the proposed encoding schemes power and energy can be saved without any significant degradation in performance and with area overhead in the NI.

II. OVERVIEW OF THE PROPOSAL

The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity and the coupling switching activity in the links traversed by the flits. In fact self-switching activity and coupling switching activity are responsible for link power dissipation. In this paper, we refer to the end-to-end scheme. This end-to-end encoding technique takes advantage of the pipeline nature of the wormhole switching technique [4].Note that since the same sequence of flits passes through all the links of the routing path, the encoding decision taken at the NI may provide the same power saving for all the links. For the proposed scheme, an encoder and a decoder block are added to the NI. Except for the header flit, the encoder encodes the outgoing flits of the packet such that the power dissipated by the inter-router point-to-point link is minimized.

III. PROPOSED ENCODING SCHEMES

In this section, we present the proposed encoding scheme Whose goal is to reduce power dissipation by minimizing the coupling transition activities on the links of the inter connection network. Let us first describe the power model that contains different components of power dissipation of a link. The dynamic power dissipated by the interconnects and drivers is

$$P_g = [T_{0\to1} (Cs + Cl) + TcCc] V^2dd Fck \qquad (1)$$

Where $T_{0\to1}$ is the number of $0 \to 1$ transitions in the bus in two consecutive transmissions, Tc is the number of correlated switching between physically adjacent lines, Cs is the line to substrate capacitance, Cl is the load capacitance, Cc is the coupling capacitance, Vdd is the supply voltage, and Fck is the clock frequency. One can classify four types of coupling transitions as described. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high while the other makes transition from high to low .A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change.

The effective switched capacitance varies from type to type, and hence, the coupling transition activity, Tc, is a weighted sum of different types of coupling transition contributions.
Therefore

$$Tc = K_1T_1 + K_2T_2 + K_3T_3 + K_4T_4 \qquad (2)$$

where Ti is the average number of Type i transition and Ki is its corresponding weight.
we use $K_1 = 1$, $K_2 = 2$, and $K_3 = K_4 = 0$.
The occurrence probability of Types I and II for a random set of data is 1/2 and 1/8, respectively. This leads to a higher value for K_1T_1 compared with K_2T_2 suggesting that minimizing the number of Type I transition may lead to a considerable power reduction. Using (2), one may express(1) as

$$P_g = [T_{0\to1} (Cs + Cl) + (T_1 + 2T_2) Cc] V^2dd Fck. \qquad (3)$$

According to [3], Cl can be neglected

$$P_g \propto T_{0\to1}Cs + (T_1 + 2T_2)Cc. \qquad (4)$$

Here, we calculate the occurrence probability for different types of transitions. Consider that flit $(t - 1)$ and flit(t) refer to the previous flit which was transferred via the link and the flit which is about to pass through the link, respectively. We consider only two adjacent bits of the physical channel. Sixteen different combinations of these four bits could occur. Note that the first bit is the value of the generic ith line of the link, whereas the second bit represents the value of its $(i +1)$th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively. In the rest of this section, we present three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder.

A. Scheme I
In scheme I, we focus on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compares the current data with the previous one to decide whether odd inversion or no

inversion of the current data can lead to the link power reduction.

1) Power Model:
If the flit is odd inverted before being transmitted, the dynamic power on the link is

$$P_o \propto T'_{0\to1} + (K_1T_1' + K_2T_2' + K_3T_3' + K_4T_4')Cc \qquad (5)$$

where $T'_{0\to1}$, T_1', T_2', T_3', and T_4' are the self transition activity and the coupling transition activity of Types I, II, III, and IV, respectively. Table I reports, for each transition, the relationship between the coupling transition activities of the flit when transmitted as is and when its bits are odd inverted. Data are organized as follows. The first bit is the value of the generic ith line of the link, whereas the second bit represents the value of its $(i + 1)$th line. For each partition, the first (second) line represents the values at time $t - 1$ (t).

As Table I shows, if the flit is odd inverted, Types II, III, and IV transitions convert to Type i transitions. In the case of Type I transitions, the inversion leads to one of Types II, III, or Type IV transitions. In particular, the transitions indicated as T_1^x, T_1^{xx}, and T_1^{xxx} in the table convert to Types II, III and IV transitions, respectively. Also, we have $T'_{0\to1} = T_{0\to0}(odd) + T_{0\to1}(even)$ where odd/ even refers to odd/ even lines. Therefore (5) can be expressed as

$$P_g \propto (T_{0\to0}(odd) + T_{0\to1}(even))Cs$$
$$+ [K_1(T_2 + T_3 + T_4) + K_2T_1^{xxx} + K_3T_1^x + K_4T_1^{xx}]Cc. \qquad (6)$$

Thus, if $P_g > P_o$, it is convenient to odd invert the flit before transmission to reduce the link power dissipation. Using (4) and (6) and noting that $Cc/Cs=4$, we obtain the following odd invert condition

$$1/4T_{0\to1} + T_1 + 2T_2 > 1/4(T_{0\to0}(odd) + T_{0\to1}(even))$$
$$+ T_2 + T_3 + T_4 + 2T_1^{xxx}.$$

TABLE I
EFFECT OF ODD INVERSION ON CHANGE OF TRANSITION TYPES

Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
	01, 10			01, 10		
t	10, 01			11, 00		
$t-1$	Type III			Type I		
	00, 11			00, 11		
t	11, 00			10, 01		
$t-1$	Type IV			Type I		
	00, 11, 01, 10			00, 11, 01, 10		
t	00, 11, 01, 10			01, 10, 00, 11		

Fig 1. The first encoder block

Also, since $T_{0\to1} = T_{0\to1}(odd) + T_{0\to1}(even)$, one may write

$$\tfrac{1}{4}T_{0\to1}(odd) + T_1 + 2T_2 > \tfrac{1}{4}T_{0\to0}(odd) + T_2 + T_3 + T_4 + 2T_1^{xxx} \qquad (7)$$

which is the exact condition to be used to decide whether the odd invert has to be performed. Since the terms $T_{0\to1}(odd)$ and $T_{0\to0}(odd)$ are weighted with a factor of $1/4$, for link widths greater than 16 bits, the miss prediction of the invert condition will not exceed 1.2% on average . Thus, we can approximate the exact condition as

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1^{xxx} . \qquad (8)$$

Of course, the use of the approximated odd invert condition reduces the effectiveness of the encoding scheme due to the error induced by the approximation but it simplifies the hardware implementation of encoder. Now, defining

$$Tx = T_3 + T_4 + T_1^{xxx}$$

and

$$Ty = T_2 + T_1 - T_1^{xxx} \qquad (9)$$

one can rewrite (8) as

$$Ty > Tx. \qquad (10)$$

Assuming the link width of w bits, the total transition between adjacent lines is $w - 1$, and hence

$$Ty + Tx = w - 1. \qquad (11)$$

Thus, we can write (10) as

$$Ty > (w - 1)/2 \qquad (12)$$

This presents the condition used to determine whether the odd inversion has to be performed or not.

2) Proposed Encoding Architecture: The proposed encoding architecture, which is based on the odd invert condition defined is shown in Fig. 1. We consider a link width of w bits. If no encoding is used, the body flits are grouped in w bits by the NI and are transmitted via the link. In our approach, one bit of the link is used for the inversion bit, which indicates if the flit traversing the link has been inverted or not. More specifically, the NI packs the body flits in $w - 1$ bits [Fig. 1]. The encoding logic E, which is integrated into the NI, is responsible for deciding if the inversion should take place and performing the inversion if needed. The generic block diagram shown in Fig. 1 is the same for all three encoding schemes proposed in this paper and only the block E is different for the schemes. To make

the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose w bits are the concatenation of $w - 1$ payload bits and a "0" bit, represents the first input of the encoder, while the previous encoded flit represents the second input of the encoder [Fig.1]. The $w - 1$ bits of the incoming (previous encoded) body flit are indicated by Xi (Yi), $i = 0, 1, . . . , w - 2$. The wth bit of the previously encoded body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). In the encoding logic, each Ty block takes the two adjacent bits of the input flits (e.g., $X1X2Y1Y2$, $X2X3Y2Y3$, $X3X4Y3Y4$, etc.)and sets its output to "1" if any of the transition types of Ty is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation (Table I).The Ty block may be implemented using a simple circuit. The second stage of the encoder, which is a majority voter block, determines if the condition given in (12) is satisfied (a higher number of 1s in the input of the block compared to 0s). If this condition is satisfied, in the last stage, the inversion is performed on odd bits. The decoder circuit simply inverts the received flit when the inversion bit is high.

B. Scheme II

In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction.

1) Power Model: Let us indicate with P_g, P_o, and P_f the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, and full inversion, respectively. The odd inversion leads to power reduction when $P_o < P_f$ and $P_o < P_g$. The power P_f is given by

$$P_f \propto T_1 + 2T_4^{xxx} . \qquad (13)$$

Neglecting the self-switching activity, we obtain the condition $P_o < P_f$ as [see (7) and (13)]

$$T_2 + T_3 + T_4 + 2T_1^{xxx} < T_1 + 2T_4^{xx} . \qquad (14)$$

Therefore, using (9) and (11), we can write

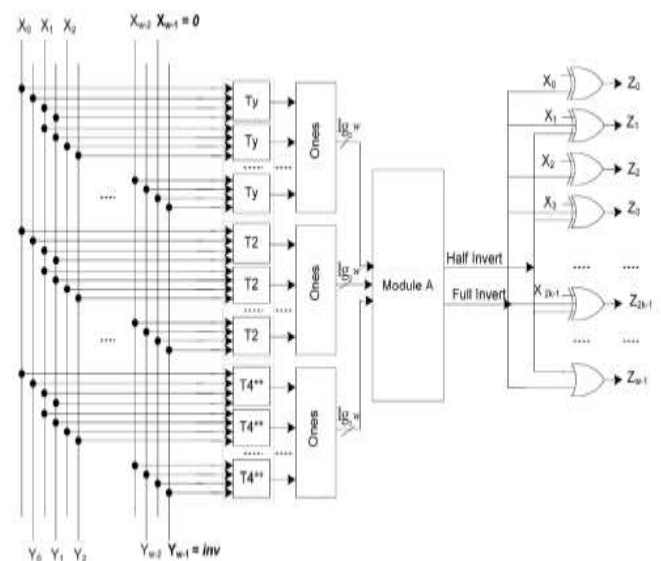$$2(T_2 - T_4^{xx}) < 2Ty - w + 1. \qquad (15)$$

Fig 2. Encoder architecture scheme II

Based on (12) and (15), the odd inversion condition is obtained as

$$2 (T_2 - T_4^{xx}) < 2Ty - w + 1 \quad Ty > (w - 1)/2. \quad (16)$$

Similarly, the condition for the full inversion is obtained from $P_f < P_g$ and $P_f < P_o$. The inequality $P_f < P_g$ is satisfied when $T_2 > T_4^{xx}$. (17)

Therefore, using (15) and (17), the full inversion condition is obtained as

$$2 (T2 - T4^{xx}) > 2Ty - w + 1 \quad T2 > T4^{xx} \quad (18)$$

When none of (16) or (18) is satisfied, no inversion will be performed.

2) Proposed Encoding Architecture: The operating principles Of this encoder are similar to those of the encoder implementing Scheme I. The proposed encoding architecture, which is based on the odd invert condition of (16) and the full invert condition of (18), is shown in Fig. 2. Here again, the *w*th bit of the previously and the full invert condition of (18) is shown in Fig. 2. Here again, the *w*th bit of the previously encoded body flit is indicated with inv which defines if it was odd or full inverted (inv = 1) or left as it was (inv = 0).In this encoder, in addition to the Ty block in the Scheme I encoder, we have the T_2 and T_4^{xx} blocks which determine if the inversion based on the transition types T_2 and T_4^{xx} should be taken place for the link power reduction. The second stage is formed by a set of 1s blocks which count the number of 1s in their inputs. The output of these blocks has the width of $\log2 w$. The output of the top 1s block determines the number of transitions that odd inverting of pair bits leads to the link power reduction. The middle 1s block identifies the number of transitions whose full inverting of pair bits leads to the link power reduction. Finally, the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power. Based on the number of 1s for each transition type, Module A decides if an odd invert or full invert action should be performed for the power reduction. For this module, if (16) or (18) is satisfied, the corresponding output signal will become "1." In case no invert action should be taken place, none of the output is set to "1." Module A can be implemented using full-adder and comparator blocks.

C. Scheme III

In the proposed encoding Scheme III, we add even inversion to Scheme II. The reason is that odd inversion converts some of Type I (T_1^{xxx}) transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions indicated as T_1^{xx}/T_1^{xxx} in the table are converted to Type IV/Type III transitions. Therefore, the even inversion may reduce the link power dissipation as well. The scheme compares the current data with the previous one to decide whether odd, even, full, or no inversion of the current data can give rise to the link power reduction.

1) Power Model: Let us indicate with P_o, P_f, and P_e the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, full inversion, and even inversion, respectively. Similar to the analysis given for Scheme I,we can approximate the condition $P_e < P_g$ as

$$T1 + 2T2 > T2 + T3 + T4 + 2T_1^x \quad (19)$$

Defining

$$Te = T2 + T1 - T_1^x \quad (20)$$

we obtain the condition $P_e < P_g$ as

$$T_e > (w - 1)/2 \quad (21)$$

Similar to the analysis given for scheme II, we can approximate the condition $P_e < P_o$ as

$$T_2 + T_3 + T_4 + 2T_1^x < T_2 + T_3 + T_4 + 2T_1^{xxx} \quad (22)$$

Using (9) and (20), we can rewrite (22) as

$$Te > Ty \quad (23)$$

Also, we obtain the condition $P_e < P_f$ as [see (13) and (19)]

$$T_2 + T_3 + T_4 + 2T_1x < T_1 + 2T_4^{xx} \quad (24)$$

Now, define

$$Tr = T_3 + T_4 + T_1^x$$

and

$$Te = T_2 + T_1 - T_1^x \quad (25)$$

Assuming the link width of w bits, the total transition between adjacent lines is $w - 1$, and hence

$$Te + Tr = w - 1 \quad (26)$$

Using (26), we can rewrite (24) as

$$2 (T_2 - T_4^{xx}) < 2Te - w + 1 \quad (27)$$

The even inversion leads to power reduction when $P_e < P_g, P_e < P_o$, and $P_e < P_f$. Based on (21), (23), and (27), we obtain

$$Te > (w - 1)/2, Te > Ty, 2(T_2 - T_4^{xx}) < 2Te - w + 1 \quad (28)$$

The full inversion leads to power reduction when $P_f < P_g$, $P_f < P_o$, and $P_f < P_e$ Therefore, using(18) and (27), the full inversion condition is obtained as

$$2 (T_2 - T_4^{xx}) > 2Ty - w + 1, (T_2 > T_4^{xx})$$
$$2 (T_2 - T_4^{xx}) > 2Te - w + 1. \quad (29)$$

Similarly, the condition for the odd inversion is obtained from $P_o < P_g$, $P_o < P_f$, and $P_o < P_e$. Based on (16) and (23), the odd inversion condition is satisfied when

$$2 (T_2 - T_4^{xx}) < 2Ty - w + 1, Ty > (w - 1)2Te < Ty \quad (30)$$

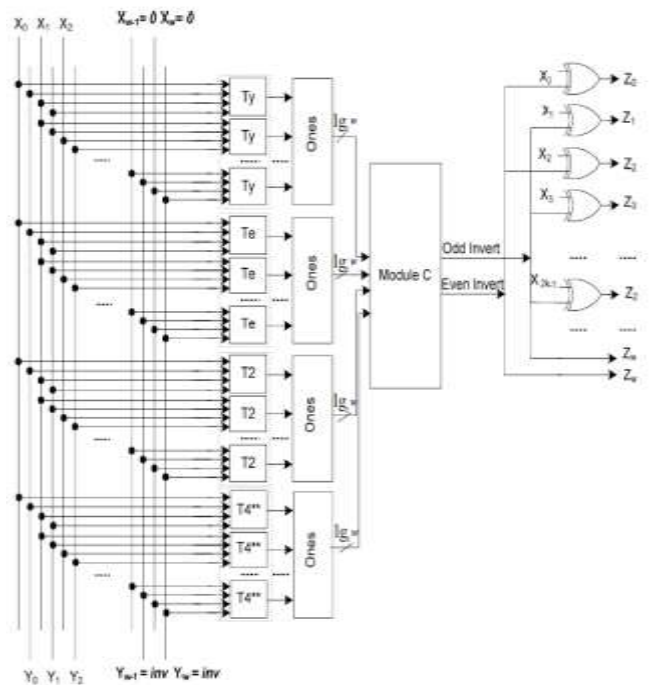When none of (28), (29), or (30) is satisfied, no inversion will be performed.

Fig 3. Encoder architecture scheme III

TABLE II

EFFECT OF EVEN INVERSION ON CHANGE OF TRANSITION TYPES

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t-1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			00, 11		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			01, 10		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			10, 01, 11, 00		

2) Proposed Encoding Architecture: The operating principles of this encoder are similar to those of the encoders implementing Schemes I and II. The proposed encoding architecture, which is based on the even invert condition of (28),the full invert condition of (29), and the odd invert condition of (30), is shown in Fig. 4. The wth bit of the previously encoded body flit is indicated by inv which shows if it was even, odd, or full inverted (inv = 1) or left as it was (inv = 0).The first stage of the encoder determines the transition types while the second stage is formed by a set of 1s blocks which count the number of ones in their inputs. In the first stage, we have added the Te blocks which determine if any of the transition types of T_2, T_1^{xx}, and T_1^{xxx} is detected for each pair bits of their inputs. For these transition types, the even invert action yields link power reduction. Again, we have four Ones blocks to determine the number of detected transitions for each Ty, Te, T_2, T_4^{xx}, blocks. The output of the Ones blocks are inputs for Module C. This module determines if odd, even, full, or no invert action corresponding to the outputs "10,""01," "11," or "00,"respectively, should be performed. The outputs "01," "11," and "10" show that whether (28), (29),and (30), respectively, are satisfied. In this paper, Module C was designed based on the conditions given in (28), (29),and (30). Similar to the procedure used to design the decoder for scheme II, the decoder for scheme III may be designed.

IV.RESULTS AND DISCUSSION:

Encoder is designed in verilog by using xilinxs 10.1 version and simulation results obtained by using modelsim 6.4b the below fig shows total power consumption value of scheme 1 encoder and decoder .here we are designing 8bit encoder and decoder consumption value shown for 28 number of combinations. the third encoder(scheme3) provides less power consumption when compared to the other two.

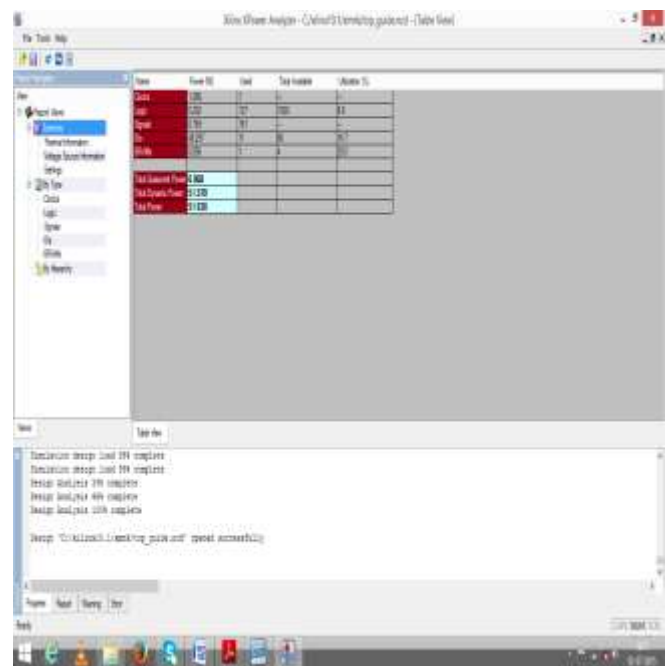Fig 1.power consumption value for scheme1 encoder

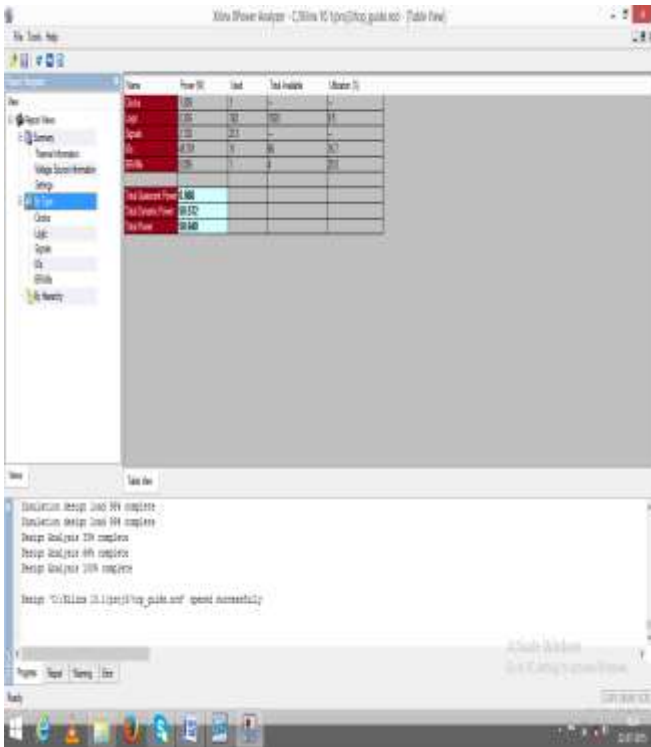Fig 2.power consumption value for scheme 2 encoder

Fig 3.power consumption value for scheme 3 encoder

V. CONCLUSION :

In this paper, we have presented a set of new data encoding schemes aimed at reducing the power dissipated by the links of an NoC. In fact, links are responsible for a significant fraction of the overall power dissipated by the communication system. In addition, their contribution is

expected to increase in future technology nodes. As compared to the previous encoding schemes proposed in the literature, the rationale behind the proposed schemes is to minimize not only the switching activity, but also (and in particular) the coupling switching activity which is mainly responsible for link power dissipation in the deep sub micron meter technology regime .The proposed encoding schemes are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the NI. The encoders implementing the proposed schemes have been assessed in terms of power dissipation and silicon area. The impacts on the performance, power, and energy metrics have been studied using a cycle- and bit accurate NoC simulator under both synthetic and real traffic scenarios. Overall, the application of the proposed encoding schemes allows saving of power dissipation and energy consumption without any significant performance degradation.

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Y.SUPRAJA is studying M. Tech with VLSI in P.B.R Visvodaya Institute of Technology and Science kavali, and obtained B.Tech from Audisankara college of Engineering and Technology JNTUA, Guduru in 2012

Mr R.S.PRATAP SINGH is the associate professor in ECE dept. At P.B.R Visvodaya Institute of Technology and Science kaval.,His research area is Communications. He completed his Mtech from P.B.R visvodaya institute of technology kavali affiliated to JNTUA. He completed his Btech from vijaya nagara engineering college, bellary affiliated to Gulbarga university. He has 15 years of experience guided 15 PG,100+UG Projects.