Utilization Of Renewable Energy Resource Pva With Parallel Current Sharing Dc-Dc Booster Converters

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In this paper, a new current sharing technique on general case of N paralleled DC–DC boost converters is presented. The proposed optimization is based on the knowledge of individual boost parameters. Every loss through the structure are modeled b equivalent resistors. Using an accurate online estimation of those resistors, the losses through each individual converter can be de termined. Then, a new current sharing scheme is defined aiming to maximize the global efficiency of the overall structure. To verify the proposed method, simulations and experiments have been realized on a three-parallel boost converters structure.

Index Terms—Boost converters, current-sharing, parallel con-verters, parameter estimation.

I. INTRODUCTION

PARALLELING dc–dc converters is widely used since it leads to many desirable features [1]. First, paralleling dc–dc converters allows a reduction of the size of components, especially inductive ones. It also reduces stress among individual converters by segmenting the total power, leading to a better global efficiency. Furthermore, this leads to an enhanced reliability, and allows possible reconfigurations when one or more of the paralleled modules present malfunctioning. In nonisolated applications, the boost converter is one of the most used since it is well known and allows good efficiency. In this paper, an N parallel boost converters structure with one output capacitor is considered, as shown in Fig. 1.

A good reliability of energy conversion is always needed. By diagnosing the fault in its early stages, the reliability of the power conversion system can be increased significantly [2]. To achieve this, it is very interesting to develop an efficient online parameter estimation. Many parameter estimation techniques have already been proposed for dc–dc boost converters. For example, in [3] and [4] a method to estimate inductance, capacitor, capacitor serial resistance, and load is presented. One of the main disadvantages of the proposed technique, as for those proposed in [5] and [6], is that it requires a sampling frequency much higher than switching frequency. For the present application, the sampling frequency is kept equal to the switching frequency. For
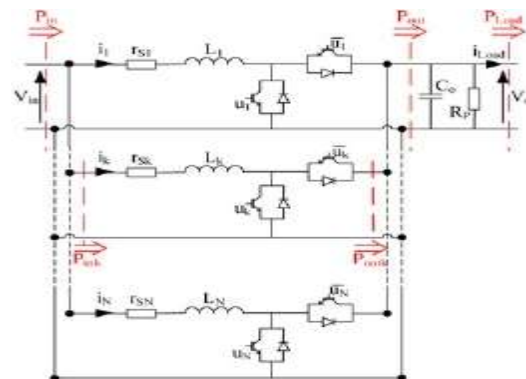

Fig. 1. N parallel boost converters structure with one output capacitor.

this reason, Shahin *et al.* work [7] is of great interest. In this paper, the authors proposed a method to model and estimate losses of the boost converter through two equivalent resistors. Note that even if loss modeling is only represented through resistors, those parameters include every loss of the converter such as capacitive or inductive ones.

Current sharing is an important functionality for parallel power converters to ensure reliable and efficient operation [8]. A good review of current-sharing techniques has been proposed by Chen *et al.* in [9] on different interconnection schemes. A first method for controlling parallel boost converters is to define one converter as the master which imposes output voltage while others are slave and only current regulated. Master–slave control have been used in [1] and [10]. Unfortunately, this control strategy is not suitable for a good reliability of the global system since it might suffer from fault tolerance against the failure of the master converter [1]. Another method found in the literature is to use current sharing to manage the output voltage error as done in [11] by using synergetic control. In [12], cur

sharing is directly integrated in a nonlinear controller design on the case of a double-input H-bridge-based buckboost–buckboost converter. A last method which can be underlined is presented in [13] where the sharing scheme is used to cancel circulating current between parallel inverters.

However, in most of the applications, current reference is equally divided between the parallel elements as done in [14]–[17]. Equal power repartition has for example been used in [18], where the control is realized with a classical PID. Many studies propose an equal repartition among many different structures, as for example in [19] on paralleled dual active bridge dc–dc converters. This is also the case for classical control techniques of paralleled inverters as done in [20] and [21]. Equal repartition is also used while thinking in voltage mode controlled structures with no current sensors as done in [22] and [23] on multiphase buck converter structures.

In this paper, a new current-sharing method based on the knowledge of estimated loss parameters is proposed. As previously mentioned, compared with the sharing techniques found in the literature, the proposed method presents real advantages. In most of the literature, the current repartition is only designed in order to allow the system to work. However, as it will be underline in this paper, the repartition can influence on the global structure efficiency. Classically, this is not taken into account. In this aim, the new sharing scheme proposed in this paper allows us to maximize the global efficiency of the overall structure.

II. Structure Modeling and Estimation

A. Model of the Structure

The system consists in N parallel boost converters with one output capacitor as shown in Fig. 1. The considered modeling equations (1a) and (1b) are a direct application of Shahin *et al.* work [7]. In this paper, it is proposed to model losses through a boost converter by adding N serial and one parallel resistors in the conventional ideal model. For the considered application, each individual boost converter model has a serial resistance r_{s_k}, while a unique parallel resistor R_p includes all the rest of the losses for the whole structure. This difference with the method proposed in [7] comes from the nature of the structure with only one output capacitor and one output current sensor. The next section details the method to obtain an accurate online estimation of the resistor values
where d_k represents the duty cycle corresponding to the PWM

$$\begin{cases} L_k \dfrac{di_k}{dt} = V_{\text{in}} - r_{s_k} i_k - (1 - d_k) V_o \ . \\ C_o \dfrac{dV_o}{dt} = \sum_{k=1}^{N} (1 - d_k) i_k - i_{\text{Load}} - \dfrac{V_o}{R_p} \end{cases} \quad (1a) \\ (1b)$$

output signal u_k.

Even if the adopted loss modeling is only represented through resistors, it is useful to underline that not only ohmic losses are taken into account. In fact, every loss through the converter is taken into account with those of equivalent resistors, such as core hysteresis and eddy current losses, conduction ohmic losses, and switching losses of semiconductors [7]. Particularly,

the parallel resistor R_p does not only represent the capacitor C_o losses through its ESR. Indeed, it is well known the even under zero power, boost converters still present losses, which will be taken into account through parameter R_p while serial resistor is not able to model this behavior. Finally, parameters r_{s_k} and R_p represent the overall losses through the structure. This will be verified in the experimental part by checking that calculated losses correspond to measurement. For a more detail description of this loss modeling technique, the reader is invited to read reference [7], where analytical study is presented, as well has load dependence behavior of such a modeling in the case of a single-boost converter.

It has to be noticed that the estimation of losses through the converters can also been used for others purpose. As an example, it can be used for verifying the ageing of the individual converters by checking on the variations of the estimated equivalent resistors. This aspect cannot be developed in this paper since it is not its goal, but reader is again invited to read [7] for more details on the estimation.

B. Parameters Online Estimation

Before designing control laws and current-sharing technique, the system parameters need to be estimated. This has to be realized by considering online sampled signals, namely, V_{in}, i_k, V_o and i_{Load}. As proposed in [7], it is possible to estimate the equivalent loss resistors following (2) and (4).

Considering that the input power follows its reference $P_{\text{in}} = P^{\text{iref}} \, _{\text{in}} t$, serial resistors will be estimated through (2). This condition will be ensured with the current regulation presented in Section III

$$\frac{d\hat{r}_{s_k}}{dt} = \lambda_{s_k} \cdot \left(\hat{P}_{\text{out}_k} - P_{\text{out}_k} \right) \cdot \left(\frac{V_{\text{in}}}{P_{\text{in}_k}} \right)^2 . \quad (2)$$

Wherepower P_{out_k} and estimated power P_{out_k} follow (3), and λ_{s_k} convergence coefficients corresponding to serial resistor r_{s_k}

$$\begin{cases} P_{\text{out}_k} = (1 - d_k) V_o i_k \\ \hat{P}_{\text{out}_k} = P_{\text{in}_k} - \hat{r}_{s_k} \left(\frac{P_{\text{in}_k}}{V_{\text{in}}} \right)^2 . \end{cases} \quad (3)$$

Then, considering the output voltage perfectly regulated ($V_o = V_o^{\text{ref}} \, t$), the parallel resistor will be estimated through (4). This condition will be ensured through the energy regulation

$$\frac{d\hat{R}_p}{dt} = \lambda_p \cdot \left(\hat{i}_d - i_d \right) \cdot \frac{\hat{R}_p^2}{V_o} . \quad (4)$$

presented in the following section

C. Stability of the Estimation

Exponential stability can be proved easily with the classical Lyapunov approach [7]. The stability and dynamics of the proposed estimations are determined by coefficients λ_{sk} and λ_p. In order to demonstrate their stability, the Lyapunov candidate
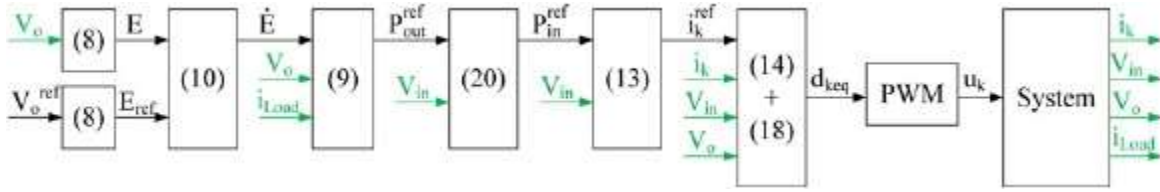
Fig. 2. Control strategy. Measurements are in green.

functions following (5) are defined as

$$\begin{cases} V\left(\hat{r}_{s_k}\right) = \frac{1}{2}\left(\hat{P}_{\text{out}_k} - P_{\text{out}_k}\right)^2 \\ V\left(\hat{R}_p\right) = \frac{1}{2}\left(\hat{i}_d - i_d\right)^2. \end{cases} \tag{5}$$

For a positive input power, their derivative can be expressed through (6)

$$\begin{cases} \dot{V}\left(\hat{r}_{s_k}\right) = \left(\hat{P}_{\text{out}_k} - P_{\text{out}_k}\right)\dfrac{\text{d}\left(\hat{P}_{\text{out}_k} - P_{\text{out}_k}\right)}{\text{d}\hat{r}_{s_k}}\dfrac{\text{d}\hat{r}_{s_k}}{\text{dt}} \\ \dot{V}\left(\hat{R}_p\right) = \left(\hat{i}_d - i_d\right)\dfrac{\text{d}\left(\hat{i}_d - i_d\right)}{\text{d}\hat{R}_p}\dfrac{\text{d}\hat{R}_p}{\text{dt}} \end{cases} \tag{6}$$

The derivatives of Lyapunov functions (6) can be simplified in view of (2) and (4), leading to (7)

$$\begin{cases} \dot{V}\left(\hat{r}_{s_k}\right) = -\lambda_{s_k}\left(\hat{P}_{\text{out}_k} - P_{\text{out}_k}\right)^2 \leq -2\lambda_{s_k}V\left(\hat{r}_{s_k}\right) \\ \qquad\qquad\qquad\qquad\qquad \forall \lambda_{s_k}, \lambda_p > 0 \quad (7) \\ \dot{V}\left(\hat{R}_p\right) = -\lambda_p\left(\hat{i}_d - i_d\right)^2 \leq -2\lambda_p V\left(\hat{R}_p\right). \end{cases}$$

Then, by choosing those two parameters positive, it is demonstrated that the estimation errors exponentially converge to 0.

III. CONTROL DESIGN

To ensure the control of the structure, it has been decided to design a two-loop control scheme. A first controller enables voltage regulation through energy control. It is based on flatness control method. A second-loop controller, based on sliding method, ensure the current regulation for each individual converter. The proposed control strategy ensures asymptotic stability, robustness against parameter variations, and high dynamics regulation. A block schematic of the entire control is given in Fig. 2.

A. Energy Control Loop Based on Flatness

Flatness was firstly defined by Fliess *et al.* [24] using the formalism of differential algebra. It has been decided to indirectly control the output voltage V_o by regulating the energy E (8) stored in the capacitor C_o. As detailed in [25] and [7], it is possible to demonstrate that E is a flat output for the considered system in view of (1a) and (1b)

$$E = \frac{1}{2}C_o V_o^2. \tag{8}$$

To obtain a relationship between the input current references i_k^{ref} and the flat output system E, the derivative $\dot{E}$ is considered

as

$$\dot{E} = P_{\text{out}} - P_{\text{Load}} - \frac{V_o^2}{R_p}. \tag{9}$$

To ensure reference tracking, a second-order control law as (10) is proposed to cancel the static error

$$\left(\dot{E}_{\text{ref}} - \dot{E}\right) + 2\xi_E \omega_{n_E}\left(E_{\text{ref}} - E\right) + \omega_{n_E}^2 \int \left(E_{\text{ref}} - E\right)\text{dt} = 0. \tag{10}$$

The power P_{out} is given as follows:

$$P_{\text{out}} = P_{\text{in}} - \sum_{k=1}^{N} r_{s_k}\left(\alpha_k \frac{P_{\text{in}}}{V_{\text{in}}}\right)^2. \tag{11}$$

The parameters α_k are power repartition coefficients. In the next section, a new current-sharing scheme aiming to maximize the overall efficiency will be detailed as a function of the parameters α_k. However, in order to transfer the needed power through the structure, repartition coefficients must follow:

$$\sum_{k=1}^{N} \alpha_k = 1 \quad \Rightarrow \quad \alpha_N = 1 - \sum_{k=1}^{N-1} \alpha_k. \tag{12}$$

Finally, current references are deduced from (13). Parameter $P_{\text{in}}^{\text{ref}}$ of this equation will be defined in Section IV

$$i_k^{\text{ref}} = \alpha_k \frac{P_{\text{in}}^{\text{ret}}}{V_{\text{in}}}. \tag{13}$$

B. Current Loops Design—a Sliding Approach

To ensure current regulation, it has been decided to design a sliding-based controller as used in [26]. Sliding based control allows robust regulation and has been detailed in [27]. It has already been applied on the case of paralleled boosts in [28] where robustness against inductor variations is underlined and guaranteed. For each individual boost converter, the sliding surface S_k is defined as follows:

$$S_k = \left(i_k - i_k^{\text{ref}}\right) + K_{i_k}\int\left(i_k - i_k^{\text{ref}}\right)\text{dt}. \tag{14}$$

The current i_k will follow its reference i_k^{ref} if the derivative of the surface S_k verify

$$\dot{S}_k = -\lambda_{i_k}S_k. \tag{15}$$

Equations (14) and (15) can be expressed as

$$\dot{\epsilon}_k + \left(K_{i_k} + \lambda_{i_k}\right)\epsilon_k + K_{i_k}\lambda_{i_k}\int \epsilon_k\,\text{dt} = 0 \tag{16}$$

where K_{i_k} and λ_{i_k} are the current regulation parameters and $\epsilon_k = \left(i_k - i_k^{\text{ref}}\right)$. Comparing (16) with a second-order law, it is

	Parameter	Value
Energy Control Loop	ξ_E	0.7
	$\omega_{n\,E}$	100 rad/s
Current Regulation	K_{i_k}	2000 rad/s
	λ_{i_k}	2000 rad/s
	ω_{i_k}	2000 rad/s

possible to express current regulation pulsation ω_I as

$$\omega_{I_k}^2 = K_{i_k}\lambda_{i_k}. \qquad (17)$$

By combning (1) and (15), it is possible to determine the equivalent duty cycle $d_{k\mathrm{eq}}$ allowing a good reference tracking

$$d_{k_{\mathrm{eq}}} = 1 + \frac{1}{V_o}\left[r_{s_k}i_k - V_{\mathrm{in}} \right.$$
$$\left. + L_k\left(-\lambda_{i_k}S_k + \frac{\mathrm{d}i_k^{\mathrm{ref}}}{\mathrm{dt}} - K_{i_k}\left(i_k - i_k^{\mathrm{ref}}\right) \right) \right]. \quad (18)$$

For simulations and experimental validation, the switching frequency is set to f_s = 20 kHz. Table I shows parameters of the controllers. Parameters ω_{i_k} are chosen in order to verify (19) which is necessary to ensure the validity of the used mean model. In a two-loop control scheme, dynamics of the regulation must be separated, then ω_{n_E} is chosen in order to satis

$$\begin{cases} \omega_s = 2\pi f_s \gg \omega_{i_k} & (19a) \\ \omega_{i_k} \gg \omega_{n\,E}. & (19b) \end{cases}$$

IV. REFERENCE POWER REPARTITION METHOD

By combining (9) and (11), the energy regulation gives the expression (20) of the total input power reference P^{ref} as a

$$P_{\mathrm{in}}^{\mathrm{ref}} = \frac{V_{\mathrm{in}}^2 - \sqrt{V_{\mathrm{in}}^4 - 4 * P_{\mathrm{out}}^{\mathrm{ref}}\left(\sum_{k=1}^N \alpha_k^2 r_{s_k}\right)}}{2\left(\sum_{k=1}^N \alpha_k^2 r_{s_k}\right)}. \quad (20)$$

Then, a new method to split the power between the parallel boost converters is presented. The proposed repartition aims to maximize the global efficiency of the structure. Indeed, it is possible to demonstrate that there is a unique point which minimizes the total input power reference P^{ref}. This can be seen in Fig. 3, where total input power is presented as a function of power repartition parameters on the case of three-parallel boost converters with the same parameters as used in Section V. Only two coefficients appear in this figure, while it is about a three-parallel boost converter structure; the third one is indeed directly imposed from (12).

As an example, in this case the minimum value differ from equal repartition possibility. Then, the interest of the proposed method appears easily compared to the most used current-sharing technique. Therefore, it is needed to determine the repar-
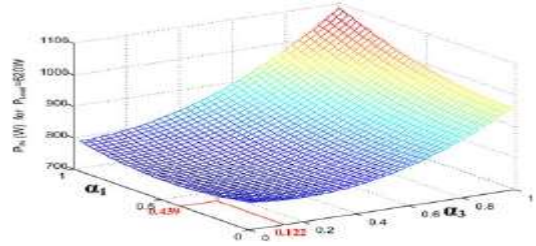the proposed repartition leads to a lower current reference for

Fig. 3. Input power function of power repartition coefficients for an imposed load of 620 W.

tition parameters α_k, so that the input power reference $P^{\mathrm{ref}}_{\mathrm{ref}}$ is is a function of $N - 1$ parameters. Minimizing this reference power leads to a given load reference P_{out}. In view of (12), $P_{\mathrm{in}}^{\mathrm{ref}}$

$$\begin{cases} \dfrac{\partial P_{\mathrm{in}}^{\mathrm{ref}}}{\partial \alpha_k} = 0, & k = \{1, N-1\} . \end{cases} \quad (21)$$

The optimal values of parameters α_k minimizing the input reference power can be expressed as (22), presenting the advantage to be quite simple and so easily implementable. Under low power, parameters r_{s_k} can not be precisely defined (they tend to infinite for zero current). In this case, it is chosen to stop $N - 1$ converters and uses only o

$$\alpha_k^{\mathrm{opt}} = \frac{\prod_{\substack{j=1\\j\neq k}}^N r_{s_j}}{\sum_{i=1}^N \prod_{\substack{j=1\\j\neq i}}^N r_{s_j}}. \quad (22)$$

Then, knowing parameters α_k, the input power reference is calculated from (20) so that it is possible to find current references for each individual converter as (13). If the parallel converters have strictly the same parameters, the propose repartition leads to equal current references $\alpha_k = \frac{1}{N}$. The main interest in the proposed method appears when one converter or more present a lower efficiency compared to the others (resulting in differences on the estimated parameters r_{s_k}). In this c the less efficient converter, leading to a benefit on the global efficiency.

Finally, before presenting simulation and experimental validation lets underline requirements for practical application of the proposed method. First, while measuring some precautions must be taken into account but such requirements are among the classical thematic of digital control, and the proposed technique does not require more accurate measurement than classically used for controlling similar power conversion structures. Second, in term of computational resources, it is obvious that this current-sharing strategy requires more than a simple equal sharing.

TABLE I
REGULATION PARAMETERS

	Parameter	Value
Energy Control Loop	ξ_E	0.7
	ω_{n_E}	100 rad/s
Current Regulation	K_{i_k}	2000 rad/s
	λ_{i_k}	2000 rad/s
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possible to express current regulation pulsation ω_I as

$$\omega_{I_k}^2 = K_{i_k}\lambda_{i_k}. \tag{17}$$

By combining (1) and (15), it is possible to determine the equivalent duty cycle $d_{k_{eq}}$ allowing a good reference tracking

$$d_{k_{eq}} = 1 + \frac{1}{V_o}\left[r_{s_k} i_k - V_{in} \right.$$
$$\left. + L_k \left(-\lambda_{i_k} S_k + \frac{di_k^{ref}}{dt} - K_{i_k}\left(i_k - i_k^{ref} \right) \right) \right]. \tag{18}$$

C. Regulation Parameters

For simulations and experimental validation, the switching frequency is set to $f_s = 20$ kHz. Table I shows parameters of the controllers. Parameters ω_{i_k} are chosen in order to verify (19) which is necessary to ensure the validity of the used mean model. In a two-loop control scheme, dynamics of the regulation must be separated, then ω_{n_E} is chosen in order to satisfy

$$\begin{cases} \omega_s = 2\pi f_s \gg \omega_{i_k} & \text{(19a)} \\ \omega_{i_k} \gg \omega_{n_E}. & \text{(19b)} \end{cases}$$

IV. REFERENCE POWER REPARTITION METHOD

By combining (9) and (11), the energy regulation gives the expression (20) of the total input power reference P_{in}^{ref} as a function of repartition parameters α_k, with P_{out}^{ref} calculated from (9) as shown in Fig. 2

$$P_{in}^{ref} = \frac{V_{in}^2 - \sqrt{V_{in}^4 - 4*P_{out}^{ref}\left(\sum_{k=1}^{N}\alpha_k^2 r_{s_k}\right)}}{2\left(\sum_{k=1}^{N}\alpha_k^2 r_{s_k}\right)}. \tag{20}$$

Then, a new method to split the power between the parallel boost converters is presented. The proposed repartition aims to maximize the global efficiency of the structure. Indeed, it is possible to demonstrate that there is a unique point which minimizes the total input power reference P_{in}^{ref}. This can be seen in Fig. 3, where total input power is presented as a function of power repartition parameters on the case of three-parallel boost converters with the same parameters as used in Section V. Only two coefficients appear in this figure, while it is about a three-parallel boost converter structure; the third one is indeed directly imposed from (12).

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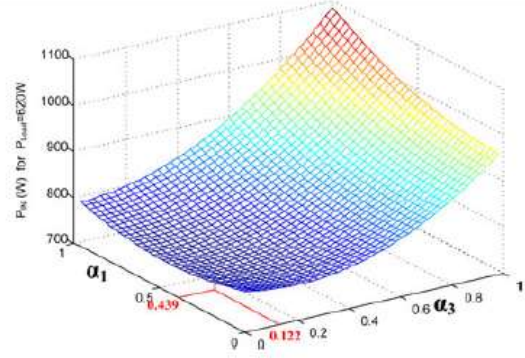

Fig. 3. Input power function of power repartition coefficients for an imposed load of 620 W.

tition parameters α_k, so that the input power reference P_{in}^{ref} is minimum for a given load reference P_{out}^{ref}. In view of (12), P_{in}^{ref} is a function of $N-1$ parameters. Minimizing this reference power leads to solve

$$\begin{cases} \dfrac{\partial P_{in}^{ref}}{\partial \alpha_k} = 0, & k = \{1, N-1\}. \end{cases} \tag{21}$$

The optimal values of parameters α_k minimizing the input reference power can be expressed as (22), presenting the advantage to be quite simple and so easily implementable. Under low power, parameters r_{s_k} can not be precisely defined (they tend to infinite for zero current). In this case, it is chosen to stop $N-1$ converters and uses only one

$$\alpha_k^{opt} = \frac{\prod_{\substack{j=1\\j\neq k}}^{N} r_{s_j}}{\sum_{i=1}^{N}\prod_{\substack{j=1\\j\neq i}}^{N} r_{s_j}}. \tag{22}$$

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Finally, before presenting simulation and experimental validation lets underline requirements for practical application of the proposed method. First, while measuring some precautions must be taken into account but such requirements are among the classical thematic of digital control, and the proposed technique does not require more accurate measurement than classically used for controlling similar power conversion structures. Second, in term of computational resources, it is obvious that this current-sharing strategy requires more than a simple equal sharing. However, additional calculations are quite simple and the additional required computation time is not important. Then, in most of the cases, implementing the proposed technique will
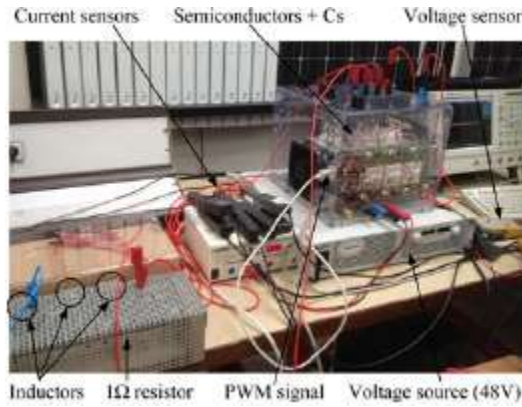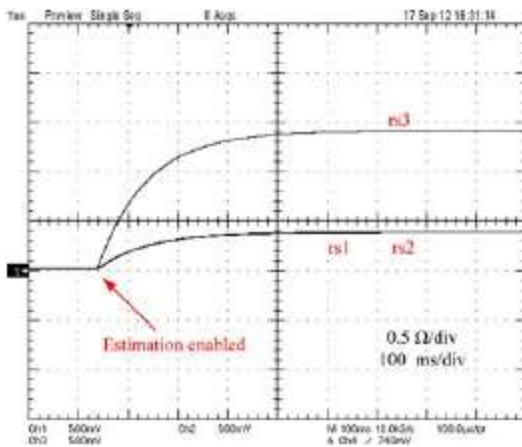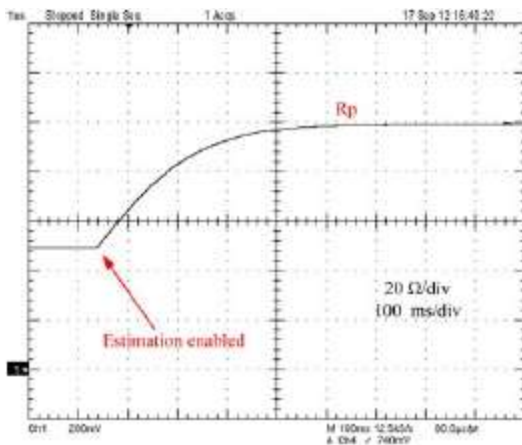
Fig. 6.   Experimental test bench.

Fig. 7.   Convergence of estimated parameters r_{sk} —Experimental result.

Fig. 8.   Convergence of estimated parameter R_p—Experimental result.

A. Control and Losses Estimation Validations

First, the validity of losses estimation is verified. Figs. 7 and

8 attest the convergence of estimated resistors. As expected, one of the serial resistor in about $1\,\Omega$ higher than other, allowing to verify the interest and validity of the proposed power repartition. The correctness of those estimated parameters is also verified as measured losses are equal to estimated ones.
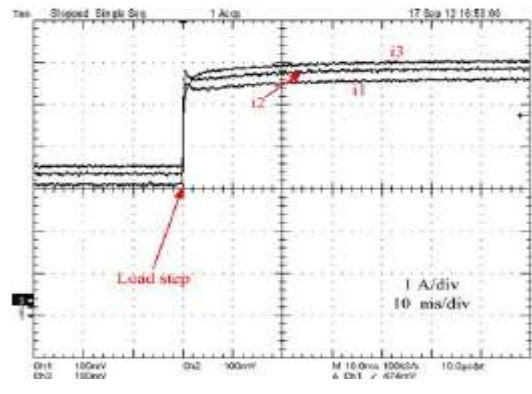

Fig. 9.   Verification of the energy regulation—Result on the output voltage V_o—Starting.

Fig. 10.   Verification of the currents regulation—Mean values of the currents for a load step.

Fig. 9 shows voltage response when the regulation starts. At this time, output voltage varies from $V_o = V_{in} = 48$ V to $V_o = 100$ V as expected. Fig. 10 shows the validity of current regulations for a step of load from $R_{Load} = 30\,\Omega$ to $R_{Load} = 15$ Ω with equal power sharing between the three converters. In this figure, only mean values of the currents are shown.

B. Current-Sharing Verification

In this section, the behavior of the proposed current-sharing scheme is verified and compared with equal repartition. Those results have been obtained with a constant resistive load $R_{Load} = 15.15$ Ω. As previously done by simulation, the next results have been obtained when power repartition passes from equal ($\alpha_k = \frac{1}{3}$) to the new optimal definition introduced in this paper. Fig. 11 shows the evolution of the structure efficiency, and Fig. 12 the corresponding sampled currents i_k. Repartition parameters obtained with our method converge to the following

values:

$$\begin{cases} \alpha_1^{opt} = 0.438 \\ \alpha_2^{opt} = 0.440 \\ \alpha_3 = 0.122. \end{cases} \qquad (24)$$
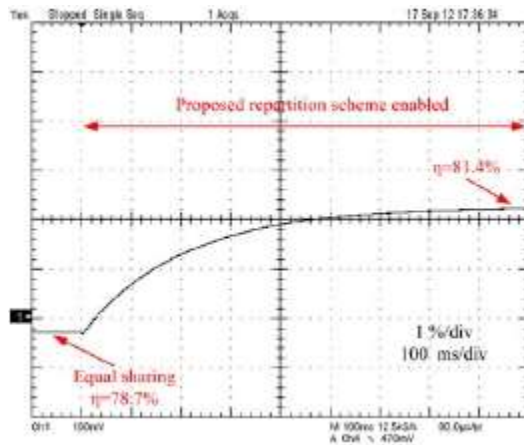
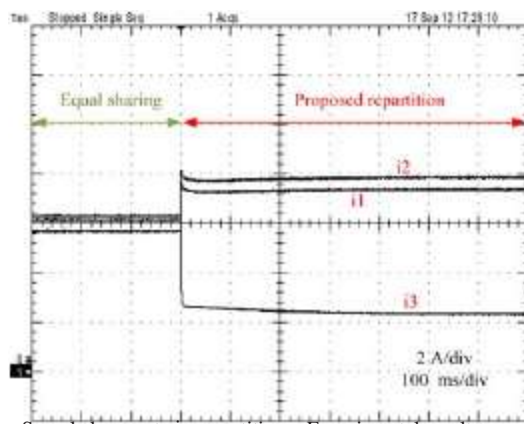Fig. 11.   Efficiency of the structure—Experimental result.

Fig. 12.   Sampled currents i_k repartition—Experimental result.

Fig. 11 shows the validity of the proposed current-sharing scheme in term of efficiency, compared with the classical equal sharing technique. In this figure, the system starts with equal sharing between the converters, and when the proposed technique is enabled, values are those of (24). After, the proposed repartition is enabled, the efficiency converges to a higher value. The transitory which can be seen in this figure comes to the fact that estimated resistor values change with the functioning point, then changing the repartition which itself changes the functioning point, and so forth, leading to a quite long transitory. This long transitory is only present in the tested case, where repartition passes from equal to the proposed one to underline its benefit. In real application, this transitory will not exist while only one of the two repartition scheme will be applied (the proposed one). This transitory is also visible in Fig. 12, where currents took time to definitely stabilize when the proposed approach is applied. In this case, when all values have converged with the proposed repartition, the new value of estimated resistors are $r_{s1} = 0.356\ \Omega$, $r_{s2} = 0.354\ \Omega$ and $r_{s1} = 1.459\ \Omega$, leading to repartition parameters following (25). This difference explains the transitory, and is also the cause of the difference with the results shown in simulation where equivalent loss resistors have been chosen constant with values equal to the one estimated

TABLE III
EXPERIMENTAL PARAMETERS

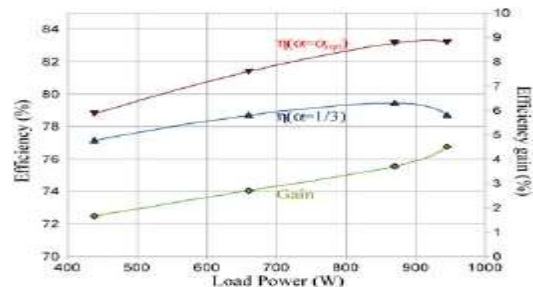| Load power	Efficiency $\alpha_k = \frac{1}{3}$	Efficiency $\alpha_k = \alpha_{opt}$	Gain
438W	77.15%	78.8%	1.65%
660W	78.7%	81.4%	2.7%
870W	79.45%	83.15%	3.7%
945W	78.7%	83.2%	4.5%

Fig. 13.   Efficiency load dependence—Advantage of the proposed method.

with equal sharing

$$\begin{cases} \alpha_1^{opt} = 0.447 \\ \alpha_2^{opt} = 0.443 \end{cases} \tag{25}$$

For the tested case, the global efficiency of the structure increases from $\eta = 78.7\%$ to $\eta = 81.4\%$ when the proposed strategy is applied. Then, compared to equal sharing, which is the most used power repartition scheme, the method detailed in this paper allows a global efficiency higher than 2.7%.

As mentioned viewing simulation results, the proposed technique should lead to make uniform ageing between parallel elements. This can be visible in Fig. 12, where the current in the converter presenting the more losses is the lower.

C. Load Dependence Experiment

In this part, the behavior of loss parameters and efficiency are experiment with respect to the load power. As explained previously, estimated loss resistors change with respect to the load. Then, advantage of the proposed method will depend on the load power. Four level of power have been tested and are listed in Table III.

The efficiency of the converter with equal sharing and with the proposed method are shown in Fig. 13. First, this result confirm the attractivity of the proposed repartition scheme since it leads to a gain in efficiency on the entire load range from 1.65% under low power to 4.5% gain under higher power. It is also possible to underline that the gain increases when power increases, and that the maximum of efficiency of the structure is higher with the proposed method. Then, compared with the classical equal sharing technique, the proposed method shows great advantage on the structure efficiency.

VII. Conclusion

A new current-sharing technique on parallel dc–dc boost converters has been presented in this paper. Through online estimation, individual converter losses are deduced and power repartition coefficients are redefined in order to maximize the efficiency of the overall structure. Output voltage and individual input currents are regulated through a two-loop control design based on flatness theory and sliding mode controllers.

Compared with the most used current-sharing technique consisting in equal repartition, the proposed method shows its interest when one or more converter in parallel present malfunctioning. In these conditions, the presented method allows a gain in efficiency up to 4.5% in the tested cases, depending on the load power. Another benefit of the proposed repartition is the fact that it leads to uniform ageing between the paralleled elements. This should have an effect on the structure health improving its long-term reliability and facilitating its maintenance. Long-term experimentations are required to attest this last assumption and will be part of future works.

The presented current sharing has been discussed, verified, and tested both by simulation and experiment. The validation has been realized on the case of a three-parallel boost converter structure, but the concept can easily be scaled to any number of phases. Indeed, theoretical study has been led on the general case of N converters in parallel. Practically, each phase will need its own current regulation, its own serial resistor estimation, and the repartition coefficients calculation will require only a few more time as the number of converter increase.

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