www.ijecs.in
International Journal Of Engineering And Computer Science ISSN: 2319-7242
Volume 4 Issue 10 Oct 2015, Page No. 14643-14648

A Study of Two Stage Operational Transconductance Amplifier using Floating gate MOSFET

Vijeta[1], Dr. Subodh Wairya[2]

[1] Electronics Engineering Department, Institute of Engineering & Technology,
Gautam Buddh Technical University,
Lucknow-226021, U.P, India
vvijeta203@gmail.com

[2]Associate Professor
Electronics Engineering Department, Institute of Engineering & Technology,
Gautam Buddh Technical University,
Lucknow-226021, U.P, India
swairya@ietlucknow.edu

Abstract: ***This paper presents a two stage operational transconductance amplifier realized using floating gate MOSFETs in differential inputs. A configuration of two stage operational transconductance amplifier using floating gate MOSFET for low power and low voltage applications is presented. Here we design a two stage operational transconductance amplifier using floating gate MOSFET in HSPICE 180nm CMOS technology with the entire transistor in the saturation region. The simulated output transient response and frequency response is shown for a supply voltage of 1V using Cosmos Scope in HSPICE. DC gain is 60dB, settling time 550ns and power consumption 3.06pW.***

Keywords: Keywords: OTA, Floating gate MOSFET

1. Introduction

Operational amplifier is an integral part of many analog and mixed mode signal systems. OPAMs with vastly different levels of complexity are used to comprehend functions ranging from dc bias generation to high-speed amplification or filtering [1].Using OPAMs greatly simplifies design analysis and implementation for analog applications. OPAMPs work well for low frequency applications, such as audio and video systems. For higher frequencies, however OPAMP design become difficult due to their frequency limit. For high frequencies, operational transconductance amplifier (OTA) is deemed to be promising to replace OPAMPs as the building blocks. Operational transconductance amplifier is one of the most important building blocks in analog IC design. OTA is an amplifier whose differential input voltage produces an output current. Thus, it is voltage controlled current source [9]. A wide variety of analog signal systems have performance that is limited by settling time behavior of CMOS OTA. The settling time behavior of CMOS OTAs determine the accuracy and speed that can be reduced [11]. However, the threshold voltage is not reduced proportionally with the supply voltage. Thus, the threshold voltage is becoming moderation for many analog circuits. Some unique technique are used to prevail over the size of the threshold voltage , e.g. floating gate transistors, bulk-driven transistors continuous time filter and low threshold transistors [12].

It is preferred to implement low voltage circuits using a floating gate transistor. Floating gate MOSFET are used in spite of of MOSFET in differential input of operational transconductance amplifier. The desire for portability of electronics equipment generated a need for low power system in battery-operated products, So the need of circuit that dissipate low power is arising significantly because low power consumption is essential in these applications to have reasonable battery life and weight. Average power, Pavg , consumed by these circuits consists of the sum of two components, static and dynamic power [4]:

$$P_{avg} = P_{static} + P_{dynamic} = V_{DD}\ I_{leakage} + CV_{DD}^2 f \quad (1)$$

Where

V_{DD} power supply voltage

$I_{leakage}$ sub- threshold leakage current of MOSFET transistor

C total capacitance of system

f frequency at which a circuit operates

Since $I_{leakage}$ is exponentially dependent upon the threshold voltage of transistor VT, the obvious way to achieve low power dissipation would be to operate them at low supply voltages, i.e to reduce power supply voltage, VDD. The simulation results have been obtained by 180nm CMOS technology. Simulation results are verified using Cosmos Scope.

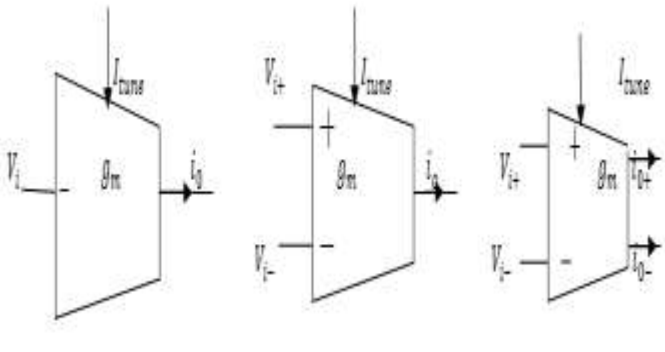
2. OTA Concept

Operational transconductance Amplifier (OTA) a monolithic direct coupled, differential voltage controlled current source (DVCCS). Feedback is added to control its overall performance, when operated into a suitable load with provision for feedback, these amplifiers are very well suited for a wide variety of applications. An ideal operational transconductance amplifier (OTA) is a voltage- controlled current source with a constant transconductance and infinite input/ output impedances. It can be characterized by the following expressions,

$$i_0 = g_m v_i \quad (2)$$

$$Z_i = \infty, \; Z_0 = \infty \quad (3)$$

Where v_i and i_0 in equation (2) denote the input voltage and the output current respectively, and g_m is the transconductance with a constant value ideally. Z_i and Z_0 in equation (3) represent the input and output impedance respectively.



(a) (b) (c)

Figure 1: Three types of OTAs (a) single input/output (b) differential-input single-output (c) differential input/output [15]

Depending on the input and output configurations, OTAs can be categorized into three types: single input/output, differential-input single-output and differential input/output (fully differential) as shown in fig.1.

$$i_0 = -g_m v_i \quad (4)$$

$$i_0 = g_m(v_{i+} - v_{i-}) \quad (5)$$

$$i_0 = i_{0+} - i_{0-} = g_m(v_{i+} - v_{i-}) \quad (6)$$

In these three types of OTAs, the transconductance g_m can be tuned via their DC current bias I_{tune} .The single input/output transconductance shown in figure 1(a) is simplicity of this type of OTA makes it motivating for high frequency performance, while most of the works preferred the differential configurations in figure 1(b) and figure 1(c) due to their common mode rejection and their flexibility to engage feedback configurations [13][14].In this paper differential-input single-output OTA is used. It contain a source – coupled differential- pair input stage, which can provide high input impedance, high gain and high common-mode rejection [16].

3. Block Diagram Of Two Stage CMOS OTA

The circuit presented here is a two stage conventional CMOS differential transconductance amplifier is often desired as the first stage in an OTA due to its differential input to single-ended output conversion and its high gain. The differential pair in input is formed by P- channel MOSFET M_1 and M_2 as shown in figure 2. The use of PMOS input devices also provides reduced power supply and low sensitivity to change in power supply voltage. This first stage of OTA had the current mirror circuit formed by an N- channel MOSFETs, M_3 and M_4.The transistor M_7 serves as an P-channel common source amplifier which is second stage of OTA [6][7].

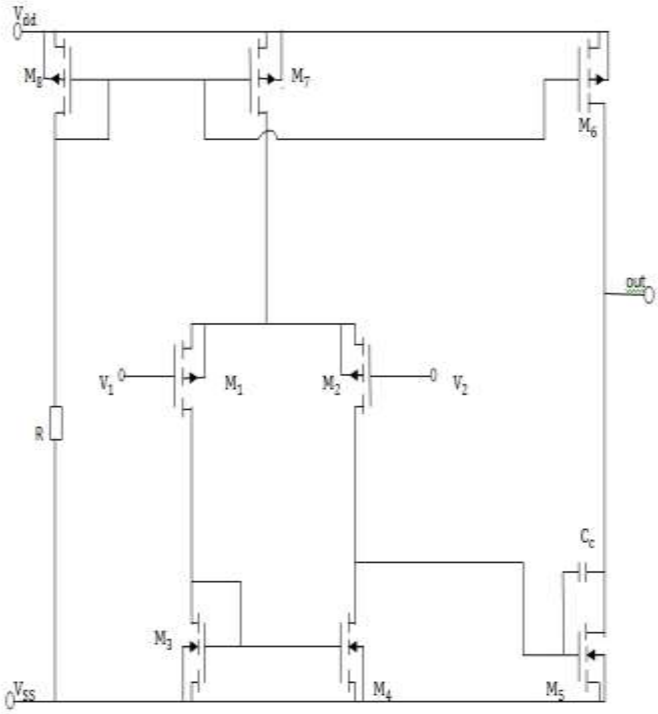


Figure 2: Two stage CMOS OTA [5]

Table1. Gate Dimensions of a Two Stage CMOS OTA

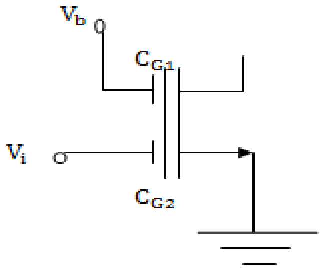
Device	Type	Gate length (µm)	Channel width (µm)
M1,M2	PMOS	0.18	10
M3,M4	NMOS	0.18	10
M5	NMOS	0.18	10
M6	PMOS	0.18	40
M7	PMOS	0.18	20
M8	PMOS	0.18	20

4.Floating Gate MOSFETS

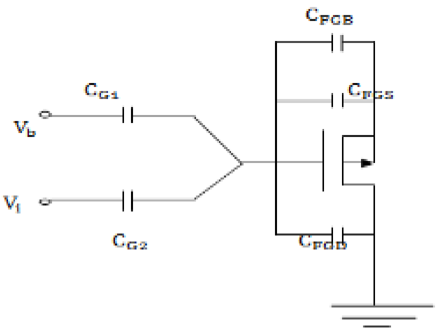
The floating-gate MOSFET (FGMOS) is field-effect transistor, whose construction is like to a conventional MOSFET. The gate of FGMOS is electrically inaccessible, generate a floating node in DC, and a number of secondary gates or inputs are deposited above the floating gate (FG) and are electrically inaccessible from it. These inputs are only capacitive connected to the FG. Since the FG is entirely bounded by high resistive material SiO_2. Because of the very good insulation properties of SiO_2, the charge on floating gate leaks away very slow, so that it always unchanged for long periods of time. As the SiO_2 layer is very thin, electrons travels through this SiO_2 layer to the floating gate, give the floating gate electrode an electrical charge. Hence the threshold voltage of the floating gate transistor is increased. When the floating gate transistor is bathed in UV light for some time, the charge on floating gate will disappear [17][18].

Two input floating gate MOSFET shown in figure 3, is a standard CMOS field effect transistor with only capacitive connections to the gate. Floating-gate MOSFET transistors are generally used in digital world as EPROMs (Erasable

Programmable Read Only Memories) and EEPROMs (Electrically Erasable Programmable Read Only Memories), that was the case for decades, but the trend these days is to use them as circuit elements, as it will be shown in this paper [4].



(a) Schematic symbol



(b) Equivalent circuit

Figure 3: Two-input floating-gate MOSFET

Two-input floating-gate MOSFET are used in operational transconductance amplifier in differential inputs as shown in fig.3. FG transistors had only been used in digital electronics EEPROM devices and despite the important role FG-MOSFET devices used in analog circuits. The main reason for this is the uncertain amount charge (Q_{FG}) that might stay trapped at the floating gate during the fabrication process causing variations of the threshold voltage. Floating gate MOSFET are useful because of their ability to store an electrical charge for extended periods of time without a connection to a power supply. Because of the very good insulation property of SiO_2 the charge on the floating gate leaks away very slowly. Reported solutions to remove Q_{FG} , floating gate transistor is bathed in ultraviolet (UV) light of correct wavelength for some time, hot electron injection, Fowler-Nordheim (FG) tunneling and forcing an initial condition with a switch [8].

The floating gate voltage is given by [4] :

$$V_{FG} = \frac{Q_{FG} + C_{FGD} V_D + C_{FGS} V_S + C_{FGB} V_B + \sum_{i=1}^{n} C_{Gi} V_{Gi}}{C_{TOTAL}} \quad (7)$$

Where V_{Gi} is voltage of the i_{th} control gate and C_{TOTAL} is the total capacitance which is given by [4]:

$$C_{TOTAL} = C_{FGD} + C_{FGS} + C_{FGB} + \sum_{i=1}^{n} C_{Gi} \quad (8)$$

Where

C_{FGD} , C_{FGS} , and C_{FGB} capacitances from gate to drain, source, and bulk respectively.

V_D, V_S, V_B drain, source, and bulk voltages

C_{Gi} capacitance coupling between each input gate and the floating gate

V_{Gi} voltage applied at input gates

5.Operational Transconductance Amplifier Based On FG-MOSFETS

Operational transconductance amplifier (OTA) is a basic block used in many analog and mixed- mode circuits. The OTA is similar to standard operational amplifier in that it has high output impedance. The circuit presented here is a two stage transconductance amplifier. The p-channel floating-gate transistors use at the differential input, M_1 and M_2 each with two input floating gate. In differential pair formed by floating gate MOSFET M_1 and M_2, one of the control inputs of each device is used for biasing and other input for signal processing purpose. It can be to use a complementary scheme with n-channel input transistors. The circuit is cascade of two stage: the first stage is a differential amplifier which consists of input devices M_1, M_2 and the current mirror M_3, M_4 which is acting as an active load, the second stage is a conventional inverter with M_5 as a driver and M_6 as an active load. The current of M_1 is mirrored by M_3, M_4 and subtracted from the current comes from the drain of M_2,then the signal contributions of the two currents multiplied by the output resistance of the first stage give the single-ended first stage output voltage. This consequential signal constitutes the input of the second gain stage. It is important that all transistors must still be working in the saturation region. Compensation capacitor Cc takes care of compensation requirements since it connects gain stage's output of the OTA with its input[9][10].

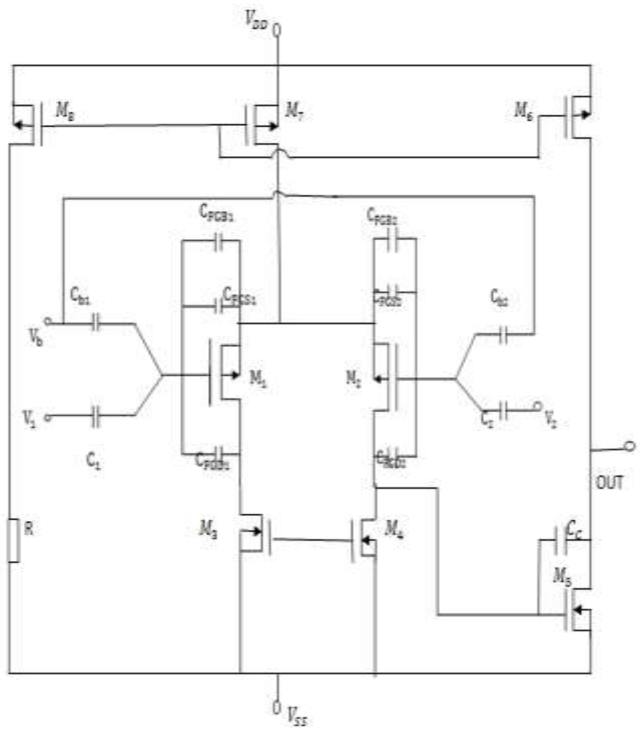


Figure 4: Circuit of two- stage OTA using FG-MOSFETs [4]

The performance of the circuit is summarized in Table 2. The values of the input capacitances for the circuit, compensation, bias voltages, and resistance used are collected in Table 3.

Table 2.Gate Dimensions of Floating Gate OTA

Device	Type	Gate length (µm)	Channel width (µm)
M1,M2	PMOS	0.18	10
M3,M4	NMOS	0.5	10
M5	NMOS	0.5	10
M6	PMOS	0.3	40
M7	PMOS	0.3	20
M8	PMOS	0.3	20

Table 3. Measurement Conditions of Two Stage FG OTA Circuit

Parameter	Value
C_{b1},C_{b2}	0.5pF
C_1,C_2	0.3pF
Cc	5 pF
V_b	0.5V

6. Simulation Results And Performance Analysis

Simulation results by HSPICE simulation in Cosmos Scope, where we summarize the results in table 4. Simulation results frequency response and transient response are shown in fig.5 and fig.6, the results shows that DC gain increase and settling time increase in OTA based on FG-MOSFETs.

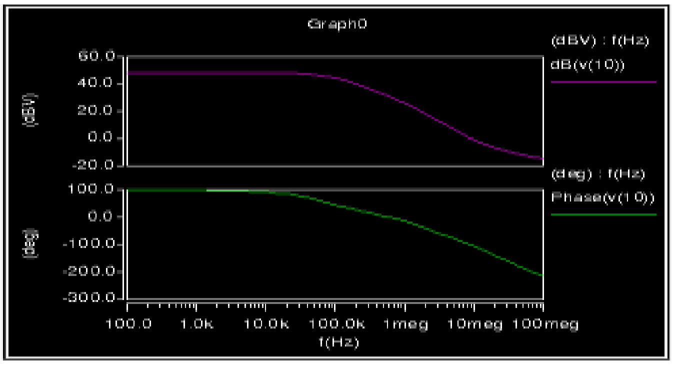


Fig.5(a). Frequency response for two stage OTA

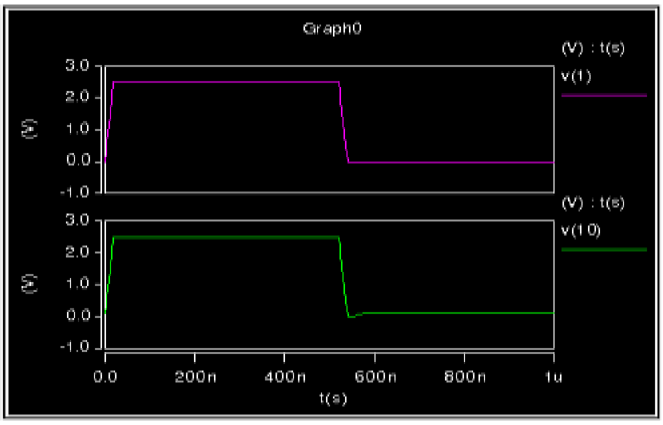


Fig.5(b). Transient response for two stage OTA

Fig. 5(a) and 5(b) shows the frequency response (magnitude and phase shift) and transient response of two stage CMOS OTA. The frequency response of two stage OTA shows the DC gain 48.2dB, gain margin is 11.19dB, phase margin is 78.48° and transient response shows the settling time is 540ns.

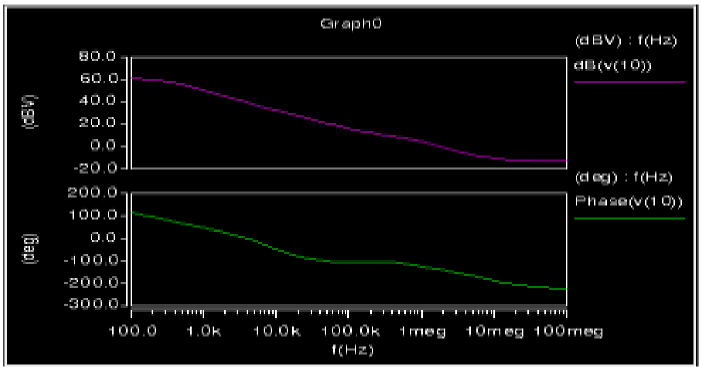


Fig.6(a). Frequency response for two stage FG OTA

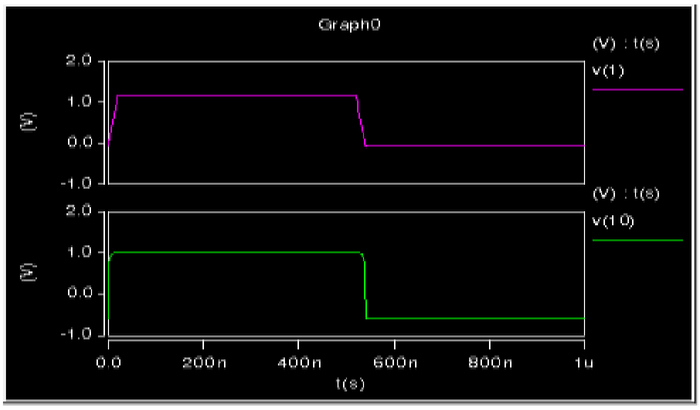


Fig.6(b). Transient response for two stage FG OTA

Fig. 6(a) and 6(b) shows the frequency response (magnitude and phase shift) and transient response of two stage CMOS FG OTA. The frequency response of two stage OTA shows the DC gain 60dB, gain margin is 9.39dB, phase margin is 39.38° and transient response shows the settling time is 550ns.

Table 4. Summarized Results of Two Stage OTA and FG-OTA

Parameters	Two stage OTA	Two stage FG-OTA
Voltage supply	1V	1V
Voltage gain	48.2dB	60dB
Gain margin	11.19dB	9.39dB
Phase margin	78.48°	39.98°
Power consumption	20nW	3.06nW
Settling time	540ns	550ns

7. Conclusion

In this paper, we have described floating gate MOSFET and used it to implement an operational transconductance amplifier. Floating gate transistors have proven to be extremely useful devices in the development of analog system. This work describes the development of this model and demonstrates its use in various applications. This work provides a solid foundation on which to build further enhancements. We can develop a model of hot- electron injection in FG transistor based on black body radiation. Also, it is likely that new dielectric materials will be used in future processes that will allow all transistors, including floating gate transistors to operate with low leakage currents while still using the thin oxide. The two stage OTA based on floating gate has compared with two stage CMOS OTA. In this paper two stage OTA and FG OTA is optimized and simulation results of the circuit are presented in 180 nm CMOS technology using HSPICE. The technique employed leads to a significant increase in DC gain and decrease in the settling time without extra power consumption.

References

[1] G. Laksmi Bhavani and A. Kalpana, "A Low Voltage CMOS Op-Amp", International Journal of Emerging Trends in Electrical and Electronics (IJETEE-ISN: 2320-9569) vol. 10, Issue 7, Aug 2014.

[2] Anjali, Vijay Khare, Dipak Dahigaonkar, "Effect of Scaling on Operation of Low Voltage OTA", International Journal of Engineering And Science (IJES) vol.2 Issue 01, 2013.

[3] S.S Rajput and S.S Jamuar, "Low Voltage Analog Circuit Design Techniques", Circuits and Systems Magazine, IEEE, vol. 2, Issue 1, pp. 24-42, August 2002.

[4] Ziad Alsibai, "Floating Gate Operational Tranconductance Amplifier", International Journal of Information and Electronics Engineering, vol.3, no.4, pp. 361-364, July 2013.

[5] Radwene Laajimi, Nawfil Gueddah, Mohamed Masmoudi, "A Novel Design Method of Two Stage CMOS OTA used for Wireless Sensor Receiver", International Journal of Computer Applications, vol.39 No. 11, February 2012.

[6] G. Palmisono, G.Palumbo and S. Pennisi, "Design Procedure for Two Stage CMOS Transconductance Operational Amplifiers", Analog Integrated Circuits and Design Processing, vol. 27, pp. 179-189, 2001.

[7] Soroush Moallemi and Abumoslem Jannesari, "A new architecture for two stage OTA with no- miller capacitor Compensation", Circuits and Systems (ICCAS), IEEE International Conference, pp. 180-183, October 2012.

[8] Steven Joseph Rapp, "A Comprehensive Simulation Model For Floating Gate Transistors", Master of Science in Electrical Engineering And Mineral Resources At West Virgima University, 2010.

[9] V. Suresh Babu, Ambika Sekhar, Salini Devi and M.R Baiju, "Floating gate MOSFET based OTA and study of mismatch", Industrial Electronics and Applications (ICIEA), IEEE Conference, pp.127-132, May 2009.

[10] David W. Graham, Ethan Farquhar, Brain Degnan, Christal Gordon, "Indirect programming of floating –gate transistor", IEEE Transactions on circuits and systems vol. 54. No.5, May 2007.

[11] Hassan Jassim Motlak and S.Nasaem Ahmad, "A Novel Design Technique of One Stage CMOS OTA for High Frequency Applications", Frequenz, vol.61, Issue 7-8, pp. 182-188, August 2007.

[12] Hitesh Modi, Nilesh D.Patel, "International Journal of Engineering and Advanced Technology (IJEAT), vol. 2, no. 3, pp. 2249-8958, February 2013.

[13] A.N. Mohieldin, E. Sanchez-Sinencio, and J.Silva-Martinez, "A fully balanced pseudo-differential OTA with common-mode feedforward and inherent common-mode feedback detector," IEEE Journal of Solid-State Circuits, vol.38, no.4, pp. 663-668, Apr.2003.

[14] G.Meyer-Brotz and A.Kley, "The Common-Mode Rejection of Transistor Differential Amplifiers," IEEE Trans. Circuit Theory, vol. 13, no. 2, pp.171-175, June 1966.

[15] Shireen T. Sheikh, D.J. Dahigoankar, Hemant Lohana, "Comparative Analysis of CMOS OTA," IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), vol.1, no.3, pp. 01-05, Dec.2012.

[16] Tahira Parveen, Operational Transconductance Amplifier And Analog Integrated Circuits, I.K. International Publishing House Pvt. Ltd, 2009.

[17] Adel S. Sedra, Kenneth Carless Smith, Microelectronics Circuits, Kenneth Carless Smith, Oxford University Press, 1998.

[18] J. Geralds, "Sega Ends Production of Dreamcast," vnunet.com, para. 2, Jan. 31, 2001. [Online]. Available: http://nl1.vnunet.com/news/1116995. [Accessed: Sept. 12, 2004]. (General Internet site)

Author Profile

Vijeta received the B. Tech degree in Electronics and Communication Engineering from FGIET, Raebareli, Uttar Pradesh Technical University, India and is currently working towards her M. Tech degree in Microelectronics with the research interest in Increasing gain and speed and decreasing power consumption of OTA, form Institute of Engineering and Technology, Uttar Pradesh Technology University, Lucknow, India.

Dr. Subodh Wairya received B. Tech (1993), M.Tech and Ph.D (2012) from HBTI, Kanpur, Jadavpur University, Kolkata and MNNIT Allahbad, India, respectively. His Ph.D research work was oriented towards PERFORMANCE EVALUATION OF HIGH SPEED LOW POWER CMOS FULL ADDER CIRCUITS FOR LOW VOLTAGE VLSI DESIGN. Currently, he is an Associate Professor at IET, lucknow(from 6 May 1996- Present).He has also served as Scientist "B" Adhoc (One Year) at DRDO, Lucknow during January, 1995-January, 1996 and Graduate Engineer under Consultancy Project at HAL, Lucknow during From January, 1994-January, 1995 (one year). Also he is one of the authors of a book entitled "A Simplified Approach to Telecommunication and Electronic Switching Systems" by C.B.L. Srivastav, Neelam Srivastava & Subodh Wairya Published by Dhanpat Rai and Company in the year 2006.