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Performance Studies of Three-Phase Cascaded H-Bridge and Diode-Clamped Multilevel inverters

T.Rakesh, Dr.V. Madhusudhan, Dr.M.Sushama
Research Scholar, JNTUH, Kukatpally, Hyderabad.
, Principal and Dean, KORMCE, Kadapa.
, Professor& Head,JNTUCEH, Kukatpally, Hyderabad.
Email: rakeshphd227@gmail.com

***Abstract*—This paper discusses a concept of two types multilevelinverters including of Cascaded H-Bridge and Diode-Clampedfor harmonic reduction on high power applications. Normally,multilevel inverters can be used to reduce the harmonic problemsin electrical distribution systems. These studies focused on theperformance and analysis of a three phase multilevel invertersincluding Cascaded H-Bridge and Diode Clamp based on SPWMapproaches. Based on the various simulations on nine levels ofmultilevel inverters, we found that the Total HarmonicsDistortion for voltage (THDv) output for both multilevelinverters is decreased. It also produces lower contents based onthe IEC standard.**

***Index Term* —Multilevel inverter, diode clamped (NPC), HBridgeinverter (CHB), SPWM.**

I. INTRODUCTION

Multilevel converters provide more than two voltage levels. And general topology of the multi-level inverter can achieve a balance between the level of effort in itself, regardless of thedrive control and load characteristics. The concept wasintroduced multi-level inverters since 1975. The applicationsare diverse and affect a wide field of electrical engineeringfrom a few watts to several hundred megawatts. They aredevoted to medium and high-voltage for current applications.The output quality of the current and voltage of multilevelinverter can be determined by high frequency switchingtechniques. The semiconductor power (e.g. GTO or IGBT highcaliber) usually operate at relatively low frequencies. [1]. Thestructure of the nine-level inverter is most suitable, ascompared to the conventional structure, since the voltages andcurrents output has a much lower harmonic distortion. Thevoltage of each switch is half and the chopping frequency islower [2]. Multilevel inverter topologies are the Neutral-PointClamped (NPC) inverters (or Diode-Clamped inverters), thecascaded H-bridge inverters (CHB), and the Flying Capacitor(FC) inverters (or Capacitor Clamped inverters), shown inFig. 1 [1].

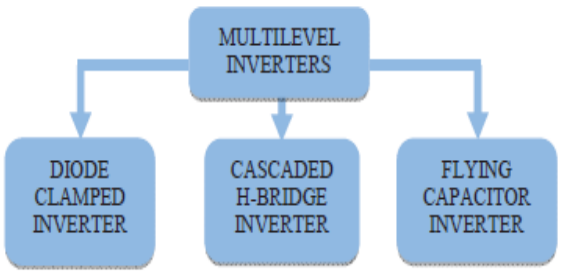

Fig.1. Multilevel Inverter Topologies.

Diode-clamped inverter has a drawback regarding the operating at complex PWM controller. However, cascaded H-bridge multilevel inverter does not this problem. Both modules have its supply the DC voltage level required, an inverter that converts DC-AC. The control structure and operation of this inverter is much more sophisticated compared to other inverters [2]. In this study, the use of GTO power will be put forward to allow higher switching frequency for harmonics reduction especially for industrial application. The (THD) for voltage and current can be calculated by using equations(1-3).

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^2}}{H_1} \qquad (1)$$

Where, $H_n$equals to the n-th harmonics at nw0 frequency, H_1= equals to the fundamental component.

$$h_n = \frac{4E}{n\pi}\sum_{k=1}^{s}\cos(n\alpha_k) \qquad (2)$$

$$let\ H_{(n)} = h_n and H_1 = h_1\ THD = \frac{\sqrt{\sum_{n=2}^{\infty} h_{(n)}^2}}{h_1}$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{1}{n}\sum_{k=1}^{s}\cos(n\alpha)\right)^2}}{\sum_{k=1}^{s}\cos(n\alpha_k)} \qquad (3)$$

The problem to be solved is to create a suitable modulator for controlling a voltage inverter using GTO Thyristor as switching elements for applications in high voltage and suitable at the same time to generate voltage waveforms with reduce harmonic content. Several PWM-procedures for multilevel inverters are available in [3]. Method of sinusoidal PWM (SPWM) can generate a wave with amplitude of which varies between a lower level and a higher level for a voltage by a multilevel inverter. "Phase Disposition "(PD), This method is applicable to both the NPC and the H-bridge For values of themodulation index, and the lowest total harmonic distortion In this study, we present the comparative analysis between multilevel circuits diode clamped inverter and cascaded H-Bridge inverter with (SPWM) strategies to mitigate THD nine (odd) levels. The aim of this study is to implement the carrier frequency parameter with modulation index for achieving the low harmonic distortion. The simulation was implemented by using MATLAB/SIMULINK toolbox environment.

II. MULTILEVEL INVERTER (MLI)

The multilevel inverter diagrams Fig. 2. Illustrates of the inverters have been 2-level inverter, 3-level inverter, and the N-level inverter. All the capacitors include to a voltage of V_{dc}.

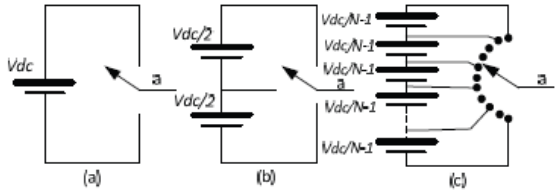

Fig. 2. The MLI diagrams of (a) 2-levels (b) 3-levels (c) N-llevels.

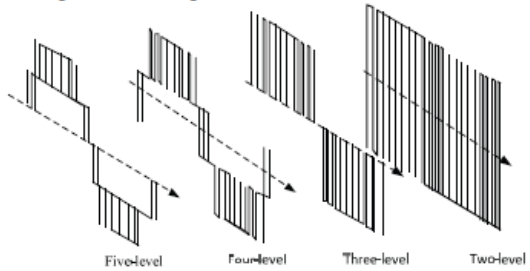

Fig. 3. Output Voltage of N-level inverter

III. MULTILEVEL INVERTERS WITH PWM METHODS

Must be a PWM signal frequency is much higher than thoseof the modulation signal, the fundamental frequency togenerate PWM signals addressed as follows:

1) Sinusoidal Pulse Width Modulation (SPWM).

2) Space vector PWM special switching sequence of three ofthe upper power of the three-phase power inverter. It can beused to expand the scope of control strategies at the twohigher levels

The method of pulse width modulation PWM is the mostcommon for comparing a modulating wave (generallysinusoidal). The PWM inverters are advancing to the previousmethod which is square-wave inverter in the following points[6]: (i) the ability of reducing total harmonic distortion, (ii)capable of controlling the output voltage, (iii) higher powerquality factor. The phenomenon of rapid and repeatedswitching at high speed causes the frequency of appearance oflowest order harmonic in the output voltage[4]. The techniquesof the carrier PWM approaches with several variant of phaserelationships for a (MLI)[5-6] are given as follows:

1) The carriers are in phase disposition (IPD).

2) Phase opposition disposition (POD). If the triangularcarriers are arranged in phase opposition, then the method isphase opposition disposition (POD) that is shifted by 180^0fromthose carriers if they are below the zero reference. This methodis more efficient than the PD of the harmonic point of view lowvalues of the modulation index.

3) The carrier arranged in triangular phase as PhaseDisposition (PD). Each of the carriers is shifted by $2\pi/(N-1)$radians.

A. Sinusoidal or "Sub harmonic" Natural Pulse Width Modulation (SPWM).

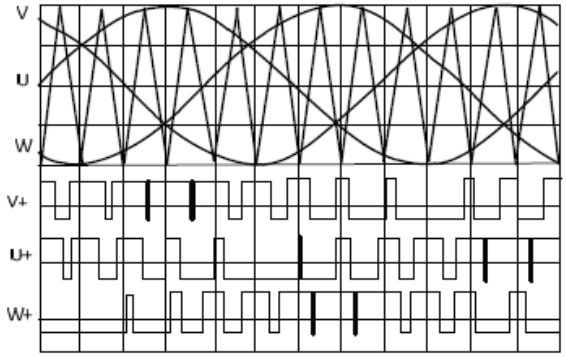

Fig 4: Modulation techniques SPWM.

In this control mode SPWM, the quality of the output voltage is being considered good if the modulation index (MI)within the range of 0 to 1.0. In case of MI is greater than 1.0,there is an anti-proportional relationship between the outputquality wave and the voltage magnitude if the quality of outputwave is decreased then the voltage magnitude increases.SPWM technology has its limitations regarding the maximumvoltage that can be achieved, and the transfer of power. Themaximum capacity of the base potential of the outputwaveform SPWM is the simplest of the rectangular waveform.In the case of a three-phase inverter, the proportion of the mainingredient to the line of maximum possible line voltage to a DCsupply voltage is 86.6% and this indicates the use of poor theDC power supply [7].

Sinusoidal PWM (SPWM) is an effective way to reduce the lower harmonics of the system while varied output voltage. However, the low frequency harmonics content is in minimum value. The modulation approach is shown in Fig. 4.

IV. TOPOLOGIES OF MULTI LEVEL INVERTERS.

A. Topology of Neutral Point Clamped Inverter(NPC)

There is another terminology that describes the diode clamped topology which is neutral point clamped topology. The main feature of the NPC topology is that it requires only one DC source similar to two-level in high power applications, the structure is most suitable, as compared to the conventional structure. The voltages and current outputs have a much lower harmonic distortion inverter. Moreover, it provides better performance [9]. In Fig. 5, we show three- phases of nine-level diode-clamped inverter. The nine-level can be achieved by using 16 switches; each phase is consisted of (8 switches for high leg and 8 switches for bottom leg). The three-phase shares common dc bus. The clamping diode can be used to restrict safe working level for the voltage across each capacitor. Fig. 6 depicts the 3 line-line output voltage wave for 9-level multilevel inverters. The output voltage is a 9-level staircase wave. Therefore, the *m*level diode-clamped inverter has a (2m-1)-level output voltage and an *m*-level output phase voltage [10].

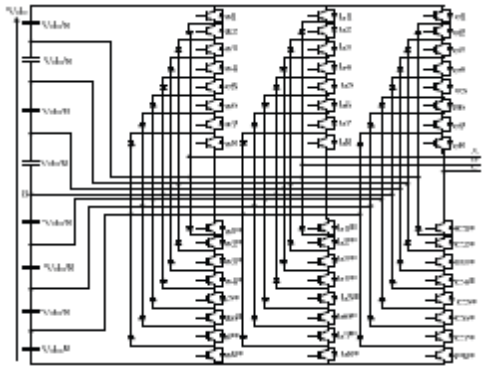

Fig. 5.Diode clamped of multilevel inverter 3-phase nine-level.

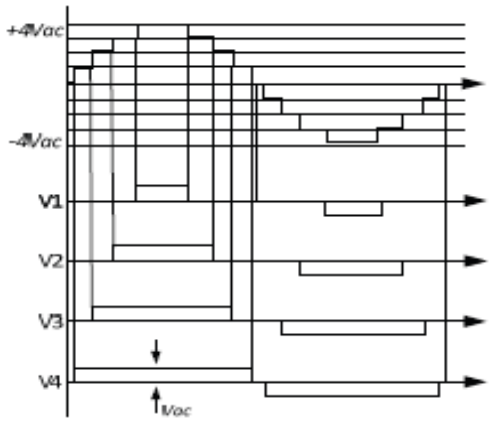

Fig.6. 9-level output voltage of multilevel inverter.

B.Topology of Cascaded H-bright Inverter (CHB)

The structure of a multilevel converter based on the series of inverters three phase H-bridge; sinusoidal wave voltage is produced by a series of connected H-bridge inverters. Each cell of the inverter is supplied by a source DC. The structure of a nine-level inverter arm cascade-type H-bridge is associated with cascade three leg three-phase inverter. The output has *2n+1* number. Total harmonic reduction can be optimized by adjusting the switching angles [11]. In comparison to diode clamped or flying capacitor, the development of inverter is cheaper. This is because the multilevel inverters very little number of components. Fig. 7 exposes out to us the three-phase nine-level cascade H-bridge inverter. In cascaded H-bridge, each low voltage H-bridge portion has its own DC-link voltage source. Its control structure is performing much better than previous ones [7]. This inverter is common with other inverters in having ninelevel. This inverter includes 4 H-bridge inverters that are connected in one lag cascaded form. The 9-level cascaded H-bridge has been built using 16 switching devices [9].

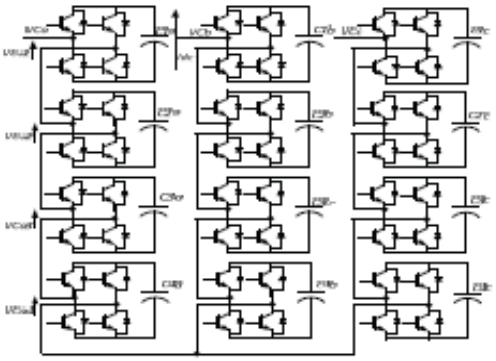

Fig. 7. Cascaded H-Bridge of multilevel inverter 3-phase nine-level .

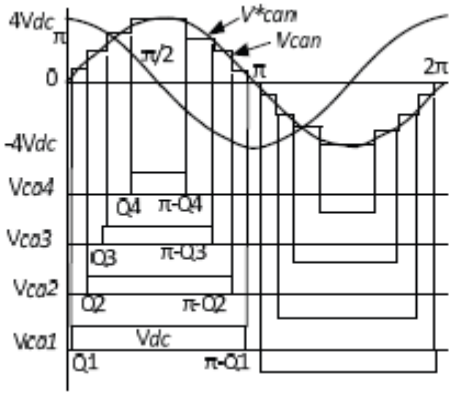

Fig.8. 9-level Cascaded H-Bridge inverter waveforms that is shown in Fig. 7.

V. SIMULATION RESULTS.

The simulation study has performed and carried out three-phase Multilevel inverters behavior based on comparativeregarding two different of a three-phase diode clamped andCascaded H-Bridge Multilevel inverters were developed andits parameters as shown in Table 1. Fig. 9-10 show thebuilding an Multilevel inverters model of MATLAB/SIMULINK simulation diagrams. In this simulation theconstant SPWM was used. We used 8 switches GTO in diodeclamped (NPC); thruster was used 48 switches GTO inCascaded H-Bridge (CHB). The carrier frequency used in thisdesigned is about 2500.

TABLE I. PARAMETERS OF CASCADED (CHB) AND DIODE (NPC).

Parameter	Value
Modulation Index	M=1, 0.8
DC Voltage	Vdc =100V
Output Frequency	50 Hz
Carrier Frequency	2500
GTO Thyristor	8 and 48 switches,

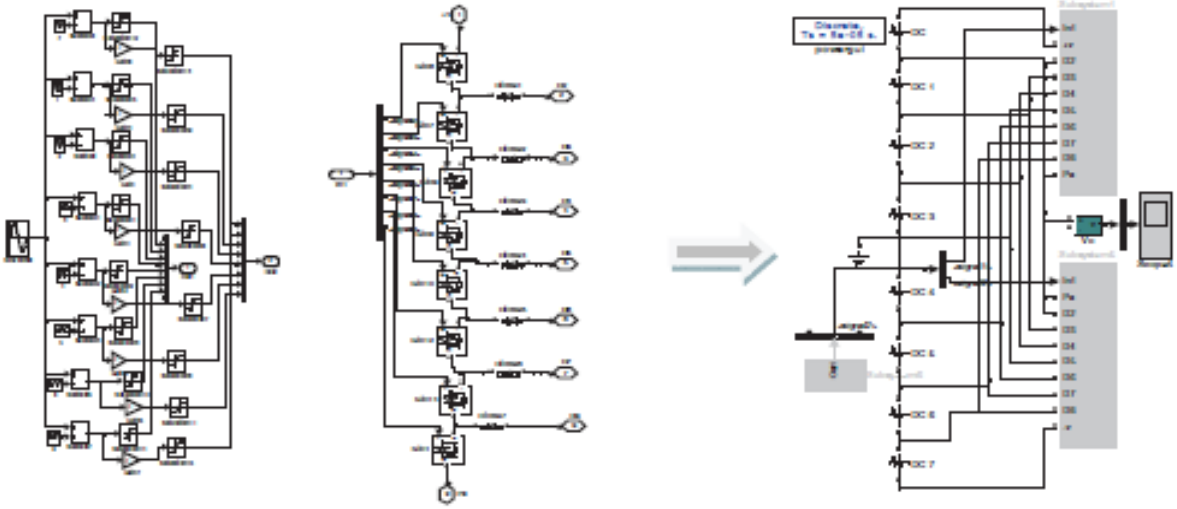

Fig.9. Block diagram for Diode Clamped: (a) left: control signal SPWM (b) middle: switching GTO Thyristor (c) right: one lag phase block diagram Diode Clamped Inverter.

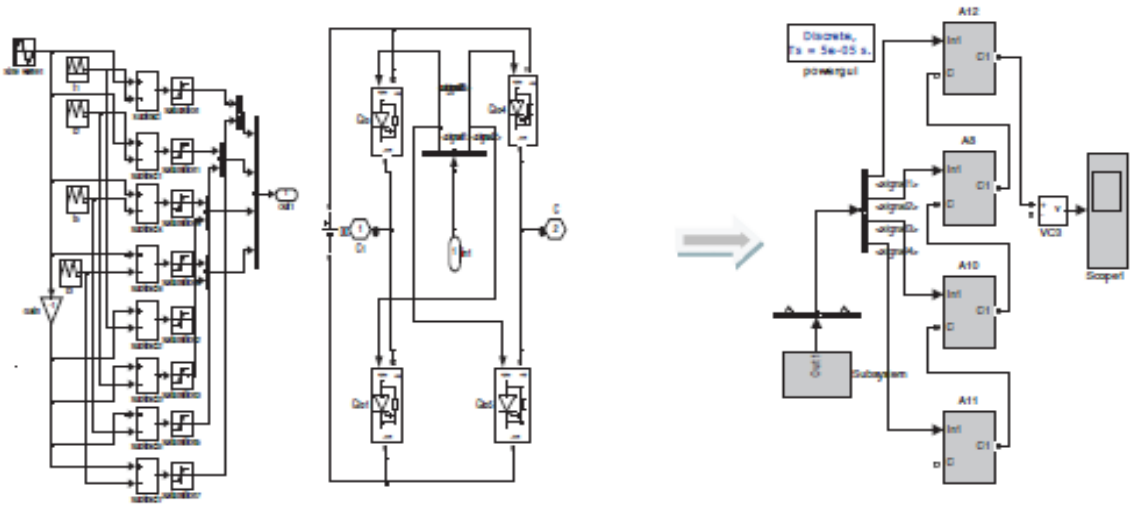

Fig.10. Block diagram for Cascade H-Bridge: (a) left: control signal SPWM (b) middle: switching GTO Thyristor (c) right: one lag phase block diagram Diode Clamped Inverter.

A.Diodeclampedmultilevelinverter results(NPCMLI):

The nine-level inverter waveform voltage line to neutral(NPC MLI) results is shown in Fig. 11. The modulation indexis equal to 1 and output RMS voltage was equal to 315.5 V. Ifthe modulation index decreased to 0.8 as shown in Fig. 12, theoutput RMS voltage was equal to 285.4 V. The quarter waveare 9 (n=9) for both of figures steps of number and the fullwave are 18 ($2n$=18, n=9) of the number of steps.

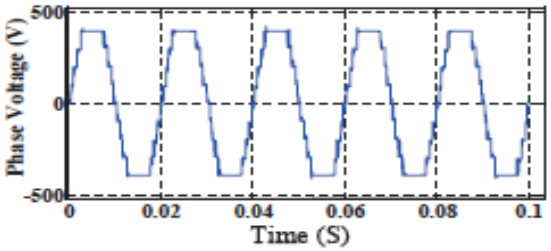

Fig.11. Phase Voltage MI=1.

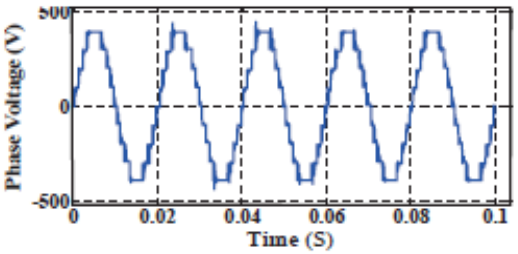

Fig.12. Phase Voltage MI=0.8.

The nine-level inverter waveform voltage line to line (NPCMLI) shows the result in Fig. 13. If modulation index is equal to 1 and output RMS voltage was equal to 542.7 V. The steps of number level quarter equal to 18 and the full wave steps level equal to 36. The modulation index decreased to 0.8 as shown in Fig. 14, output RMS voltage was equal to 492.9V.

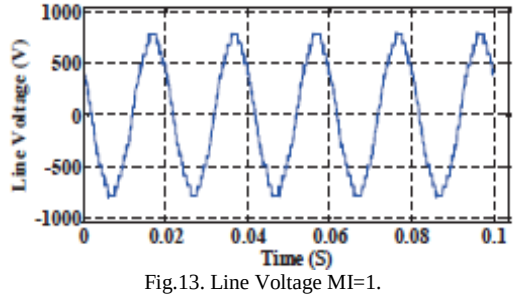

Fig.13. Line Voltage MI=1.

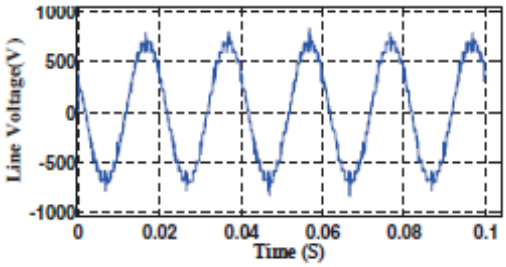

Fig.14. Line Voltage MI=0.8.

The measured MI=1 for voltage of the output diode clamped multilevel inverter the value of THD$_v$for voltage is around 3.9% as shown in Fig.15.

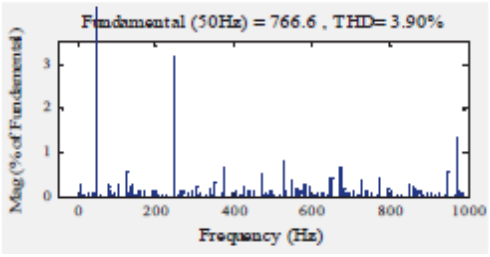

Fig.15. Harmonic Voltage M=1.

FFT analysis is the Diode clamped multilevel inverter output. The value of THD$_v$in Fig.16: for voltage obtained other output MI=0.8 lower than MI=1 and its value is 3.07%.

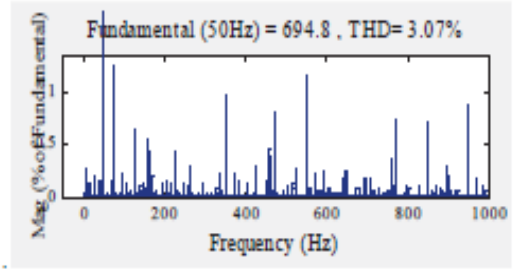

Fig.16 Harmonic Voltage M=0.8.

B.Cascaded H-Bridge multilevel inverter results (CHB):
The nine-level inverter waveform voltage lines to neutral (CHBMLI) shows the result in Fig. 17. If modulation index is equal to 1, output RMS voltage was equal to 262.2 V. When the modulation index decreased to 0.8 as shown in Fig. 18, the output RMS voltage was equal to 202.8 V. The quarter wave are 9 (n=9) for both of figures steps of number and the full wave are 18 (2n=18, n=9) of the number of steps.

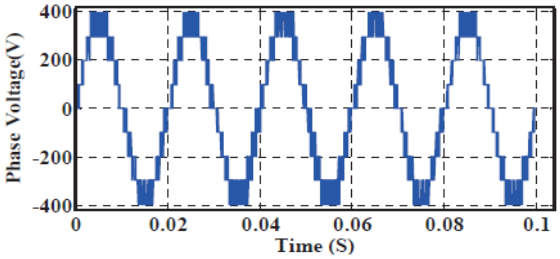

Fig.17. Phase Voltage MI=1.

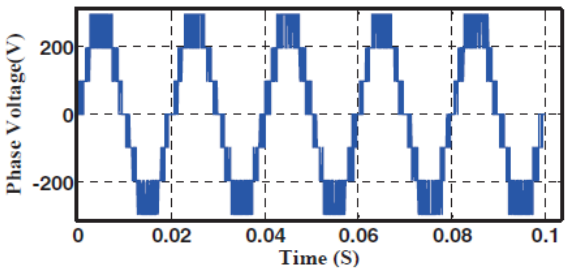

Fig.18. Phase Voltage MI=0.8.

The nine-level inverter waveform voltage line to line (CHBMLI) shows the result in Fig. 19.With modulation index is equal to 1 and output RMS voltage was equal to 452.8 V. The steps of number level quarter equal to 18 and the full wave steps level equal to 36. The modulation index decreased to 0.8 as shown in Fig. 20, the output of RMS voltage was equal to 349.7 V.

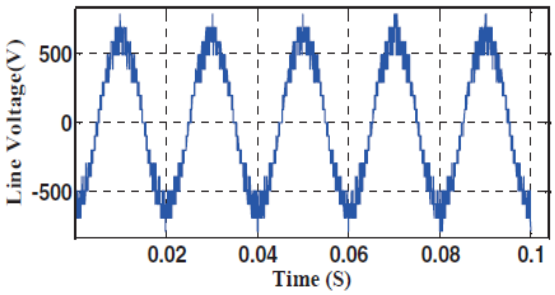

Fig 19.Line Voltage MI=1.

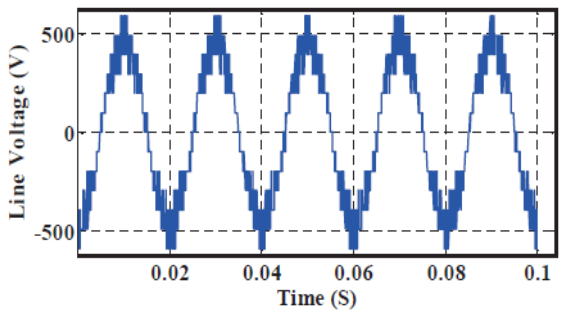

Fig 20.Line Voltage MI=0.8.

The measured MI=1 for voltage of the output Cascaded H-Bridge multilevel inverter the value of THD$_v$for voltage is around 2.92 % as shown in Fig. 21.

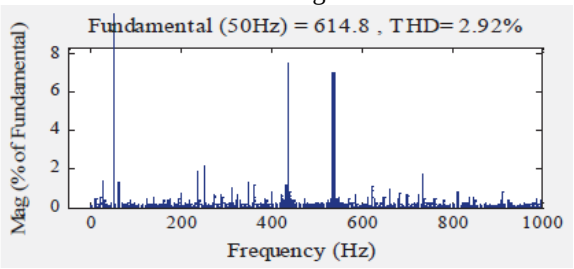

Fig 21.Harmonic Voltage M=1.

FFT analysis is the Cascaded H-Bridge multilevel inverter output. The value of THD_vshow in Fig. 22: for voltage obtained other output MI=0.8 lower than MI=1 and its value is 3.58%.

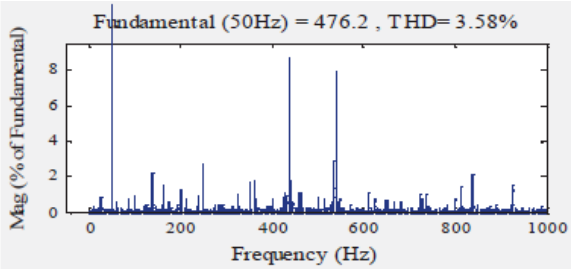

Fig.22 Harmonic Voltage M=0.8

TABLE II. COMPARISON NINE-LEVEL OF DIODE-CLAMP AND CASCADEDHBRIDGE INVERTERS WITH DIFFERENT MODULATION INDEX (M=1, M=0.8).

M		1	0.8
Phase Voltage	Diode Clamped	315.5	285.4
	Cascaded H-Bridge	262.2	202.8
Line Voltage	Diode Clamped	542.7	492.9
	Cascaded H-Bridge	452.8	349.7
THD	Diode Clamped	3.90%.	3.07%.
	Cascaded H-Bridge	2.92%	3.58%

VII. CONCLUSION

The comparative studies between two types of multilevel inverters have been investigated. The output line voltage of the diode clamped (NPC) is slightly higher than the output line voltage of H-Bridge cascaded (CHB) multilevel inverters due to more losses available in diode clamp. However the THD_v ofboth multilevel inverters are reduced and its values are following IEC standard.

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