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Pulsed Latches Methodology to Attain Reduced Power and Area Based On Shift Register

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Abstract

The power consumption and area reduction are the key challenges in the Very Large Scale Integration (VLSI) circuit design. Power consumption and Area reduction plays a major role in sequential circuit design. Shift register is the main building block in the VLSI circuits. The shift register is composed of clock inter connection network and timing elements such as flip-Flops and latches. The shift registers are design using edge triggered flip flops but the use of latches for shift register design also optimizes the area. This project introduces a low power and area efficient shift register using pulsed latch and pulse generation circuit. If the Flip-Flop is replaced with the pulsed latch the area and power consumption can be reduced to 50% in the shift register. For this design a non overlap clock pulses are used. This solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. To minimize power consumption various non overlap delayed pulsed clock signal design is proposed for data synchronization in an exceedingly multi bit shift register. The proposed system is designed by using a popular Schematic and layout capture tool with 90nm technology.

Keywords: Flip-flop, Pulse latch, Shift Register, Area-efficient, Pulsed clock

1. INTRODUCTION

The rapid growth in semiconductor devices and VLSI designs has led to the development of high performance designs with enhanced reliability, customized size and low power, and because of the power dissipation is critical issue for battery operated systems. Therefore the designs are needed to be consuming less power while maintaining comparable performance. So everyone in VLSI design must think about area utilization and power dissipation In digital design flip-flops and latches are basic storage elements. Flip flops are precarious timing elements in digital circuits which have a great impact on speed and power consumption. In VLSI chip design reducing power has become a important consideration of an performance and area. The Shift register is a type of sequential circuit it is mainly used for storage or transfer digital data.

Low power consumption and area reduction is one of the main objectives in the designing of VLSI design. The Shift register is the basic building block in VLSI circuits. It is commonly used in many applications. The architecture of shift register is quite simple. The M bit shift register can be is composed of M data flip-flops. The smallest flip-flops are suitable for designing of shift register to reduce the area and power consumption.

Latches and flip-flops are the basic elements for storing information. The flip-flops and latches could be grouped under the static and dynamic design styles. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their

content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes.

The shift registers are commonly used for memory designs. The shift registers are design using edge triggered flip flops. All the flip flops are synchronized through clock signals. The increase in word length of shift register will increase the number of flip flops. The edge triggered flip flops are design with two or more than two latches. The general structure of flip flop is design using master slave latches. The internal structure of shift register composed of N number of series connected D flip flops. The latches are design using combination multiplexer logic cell using transmission gates. The structure of N bit shift register is composed of series connected synchronized N number of flip flops. The shift register is design with cascaded flip flops hence there is no interconnected circuits between the flip flops hence speed is not the major constraints of shift register design as compare to area and power. The latches are mostly not used in design of shift register due to its timing problems. The non overlap pulse latches are the better option of design of shift registers. It reduces the number of transistors for design which in turn also reduces the area and power consumption.

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

2. OBJECTIVE

The designing of a shift register is quite simple. An n bit shift register is composed of series connected N data flip-flops. The speed of the flip flops is of no major constraint here as there are no connections between the shift registers and flip flops. The smallest flip flop is enough to drive the requirement of the shift register and for this same reason the pulsed latches have replaced the flip flops as they are much smaller in size Vis a Vis the flip flops there by reducing power consumption. Although there are some drawbacks like that of the timing problem, which is easy to overcome by the use of multiple clocked pulses instead of a simple single pulsed clock. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

3. PROBLEM STATEMENT

The main challenges for designing low power area efficient shift registers using latches is to optimize power & reduce the area without affecting the response or timing problem.

- Solving Timing Problem: Timing problem remains silent issue which stops the usage of pulse latch in shift register. The output signal of first latch changes correctly because input signal of first latch is constant during the clock pulse width T-Pulse. But the second latch Q2 has uncertain output signal because input from Q1 changes during clock pulse width. So to avoid this timing problem a delay circuit is introduced. As a result, all latches have constant input signals during the clock pulse width and no timing problem occurs between the latches.
- Reduced Area: Area required for Shift register using flip-flops is twice than that of shift registers using latches because a flip-flop consists of two latches. Thus area is reduced by 50% by replacing flip-flops with latches.
- Reduced Power: Flip-flop consumes near about 50% of total power because in sequential circuit. By replacing flip-flops with latches in proposed shift register, the power is saved by using clock pulsed instead of clock signal. Because of all these reasons, static differential sense amplifier shared pulsed latch is an attractive choice for efficient design of shift register.

4. PROPOSED METHOD

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A master slave flip-flop using two latches can be replaced by a pulsed latch consist of latch and a pulsed clock signal. In this, all the pulse latches share pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption

The shift register is designed by consisting of several latches and pulsed clock signal there will be a timing problem occur. The schematic diagram shows in Fig 1 consist of several latches and a pulsed clock signal. The operation wave form shows the timing problem in the shift register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width .But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock

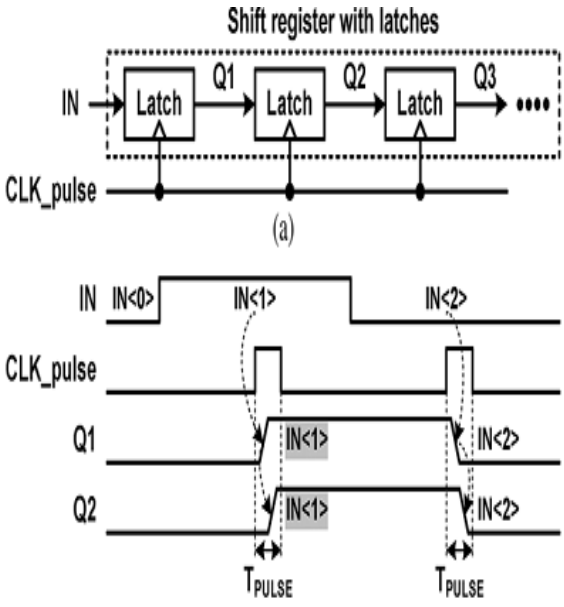
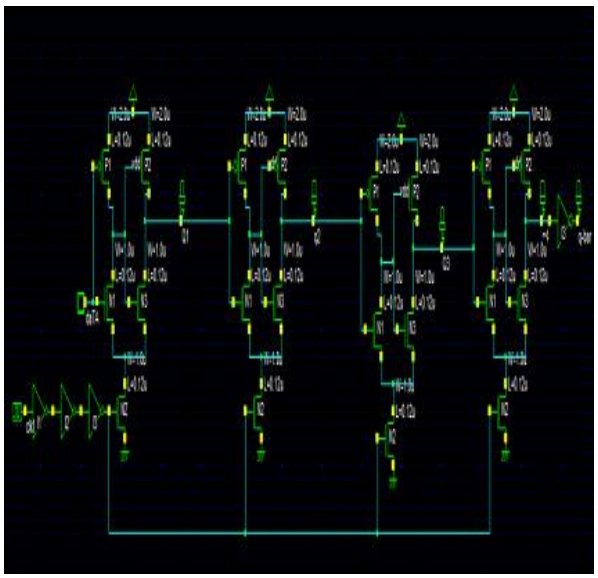
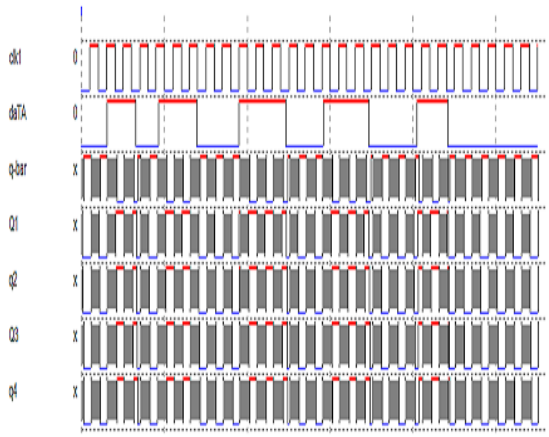


Fig. 1: Shift register with latches and pulsed clock signal (a) Schematic. (b) Wave form

The shift register with latches and pulsed clock signal designed by using DSCH2 tool is shown in Fig 2(a) and its timing response is shown in Fig .2(b). From this we can analyze the timing problem of the shift register.



(a)



(b)

Fig 2.simulation of shift register with latches (a) and its timing diagram (b)

One solution for the timing problem is to add delay circuits between latches. The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig.3 the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width, but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem will occur, however the delay of the circuit cause large area and power consumption.

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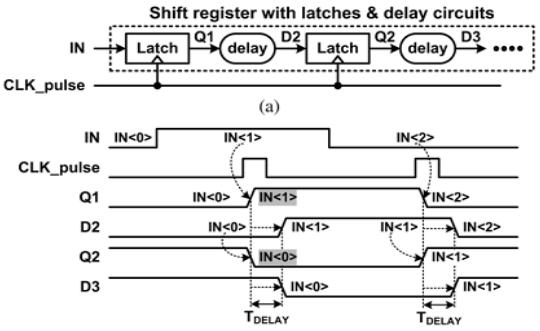

Fig3. Shift register with latches, delay circuits and a pulse clock signal (a) schematic and (b) waveform.

The proposed shift register is splits into many sub shifter register M as shown in fig. 4(a). it is to narrow the delays of pulsed clock signals. The operation of proposed shift register in this first four bit sub shifter exist of five latches and it executes shift operations with five non overlap delayed pulsed clock signals as clock_ pulse <1> up to clock _pulse <T>.In the whole sub shifter register is taken as the four bit shift register #1.The four latches stores four bit of data Q1, Q2, Q3, Q4 and finally last latch stores one bit usual data as T1 as shown in fig. 4(b). This T1 gives as the input next four bit shift register #2 and in this the latches stores the data as Q5 to Q8 and final last latch has the data of T2. In this the data shifts up to shift register #M. In shift register every latch exist clock pulses in this the clock pulses are generated from the delayed pulsed clock generator as shown in fig 3. In this shift register the delayed pulsed clock generator consists of delays, AND gates. In this delay circuits has the rising and falling times in all inverters so that the AND gate generated with inverters produce sharp pulsed clock signals.

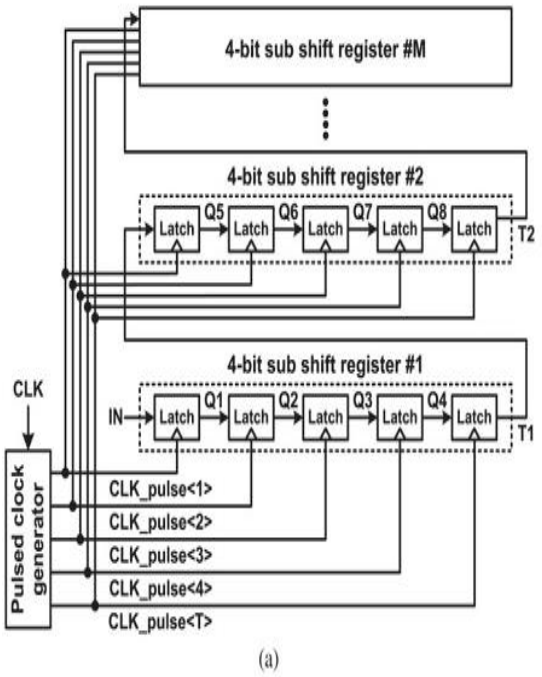

Fig. 4(a): proposed shift register using pulsed latches

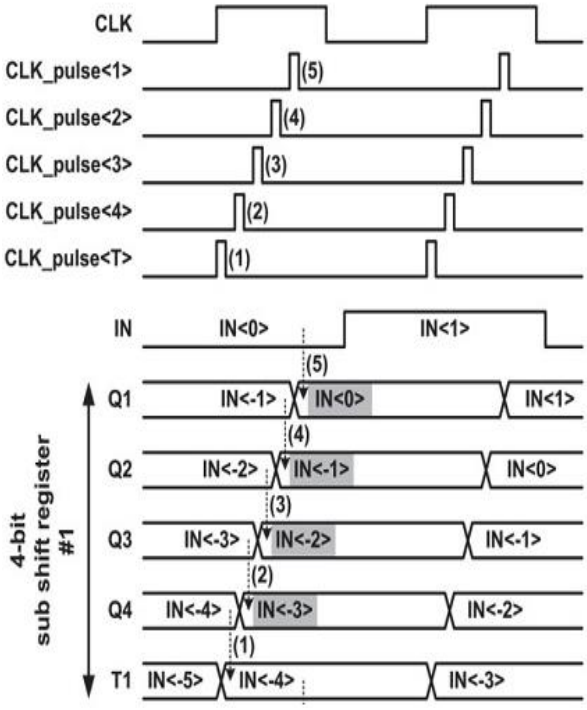

Fig. 4(b): proposed shift registers wave forms

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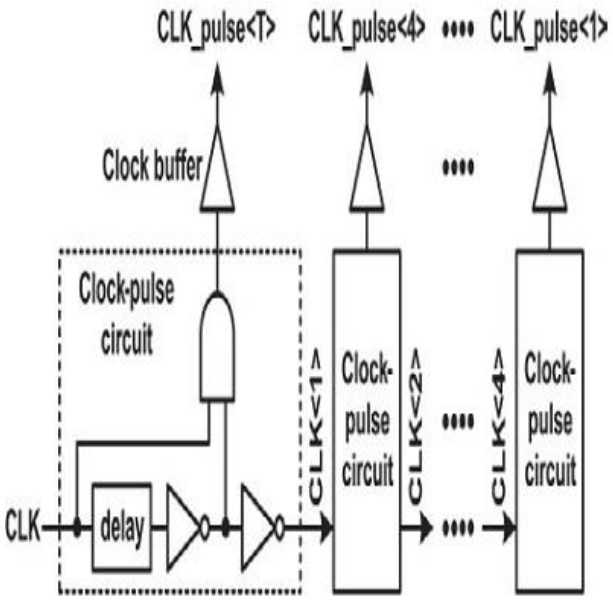

Fig.3: delayed pulsed clock generator

This design implementation the proposed shift register uses the pulsed latch is SSASPL (static differential sense amp shared pulsed latch) it is smallest pulsed latch. By using this SSASPL the design of pulsed latch used in proposed shift register. The below fig .4 shows the circuit diagram of SSASPL with transistors.

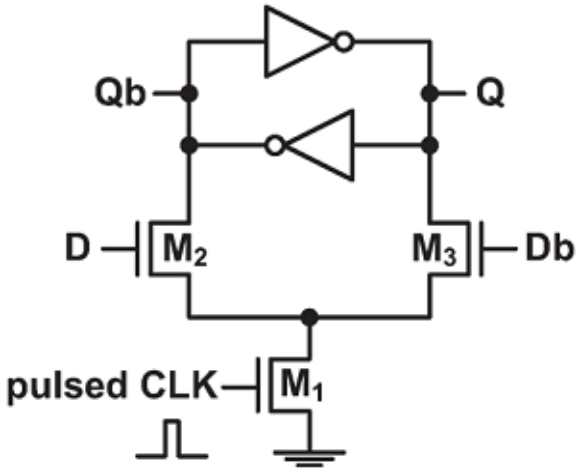

Fig.4: Circuit diagram of SSASPL

4. RESULTS

EXISTING

Area

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	9	4656	0%
Number of Slice Flip Flops	16	9312	0%
Number of bonded IOBs	19	232	8%
Number of GCLKs	1	24	4%

Delay

```
Data Path: d15/Q to Q<15>
                                   Gate     Net
  Cell:in->out       fanout      Delay    Delay  Logical Name (Net Name)
  ----------------------------------------------  ------------
   FDR:C->Q               2      0.514    0.380  d15/Q (d15/Q)
   OBUF:I->O                     3.169           Q_15_OBUF (Q<15>)
  ----------------------------------------------
  Total                          4.063ns (3.683ns logic, 0.380ns route)
                                         (90.6% logic, 9.4% route)
```

PROPOSED

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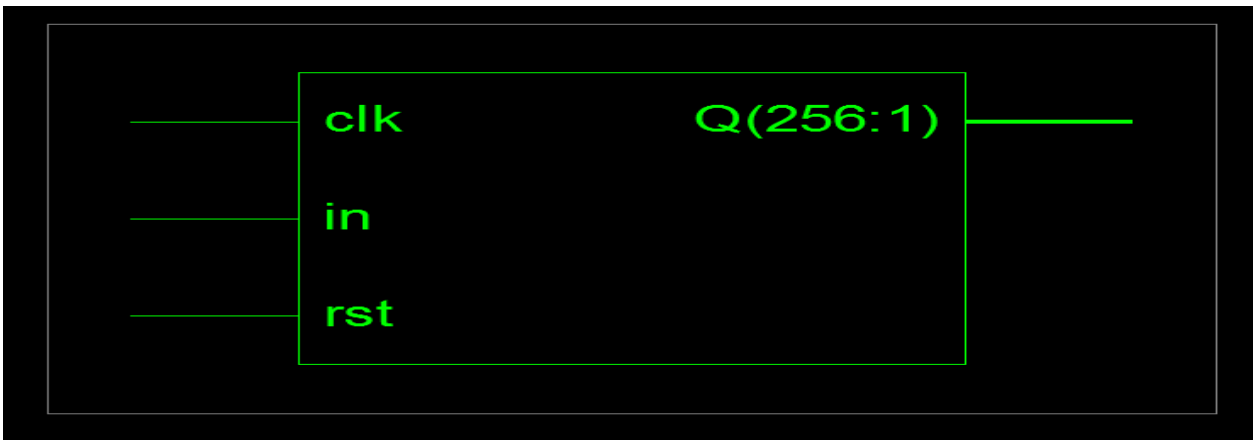
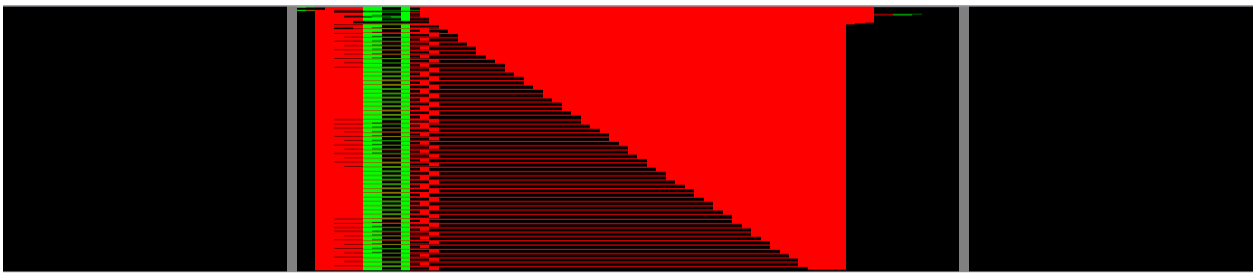
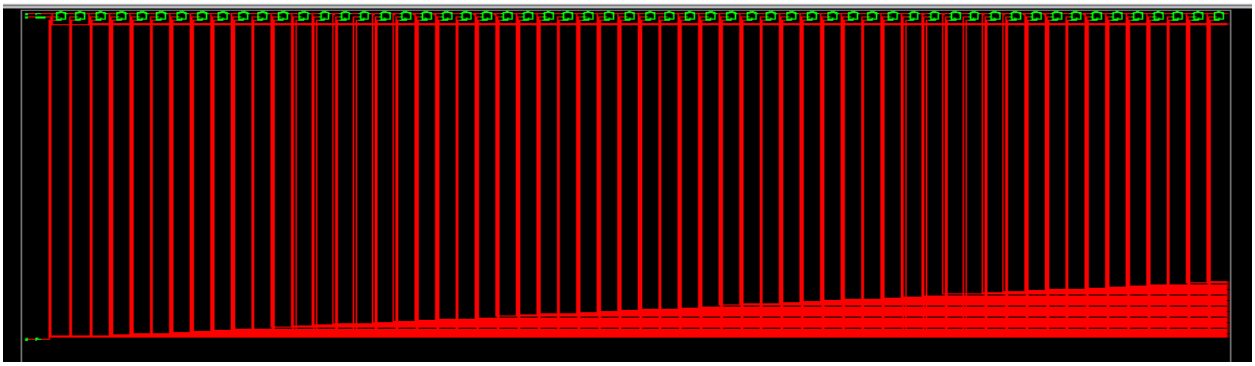


RTL schematic



Technology schematic:



Area

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	179	4656	3%
Number of Slice Flip Flops	319	9312	3%
Number of bonded IOBs	259	232	111%
Number of GCLKs	1	24	4%

Delay

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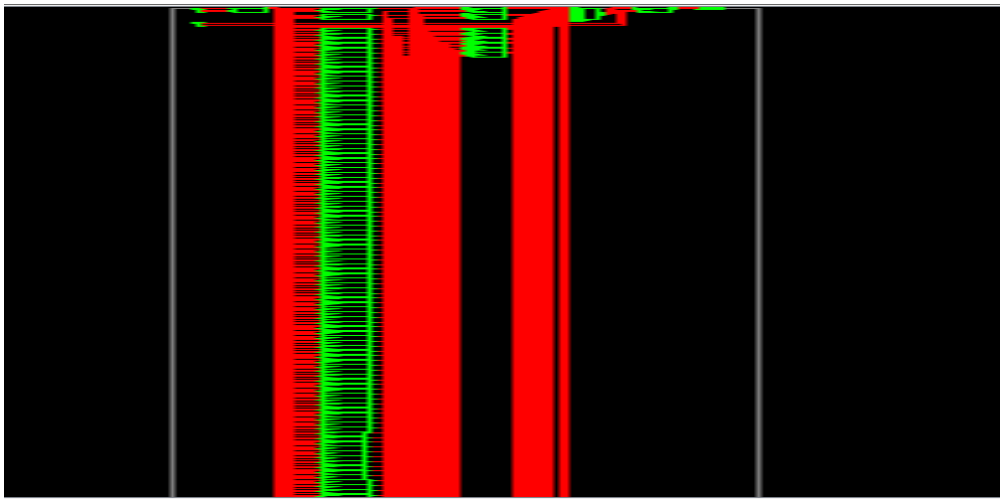
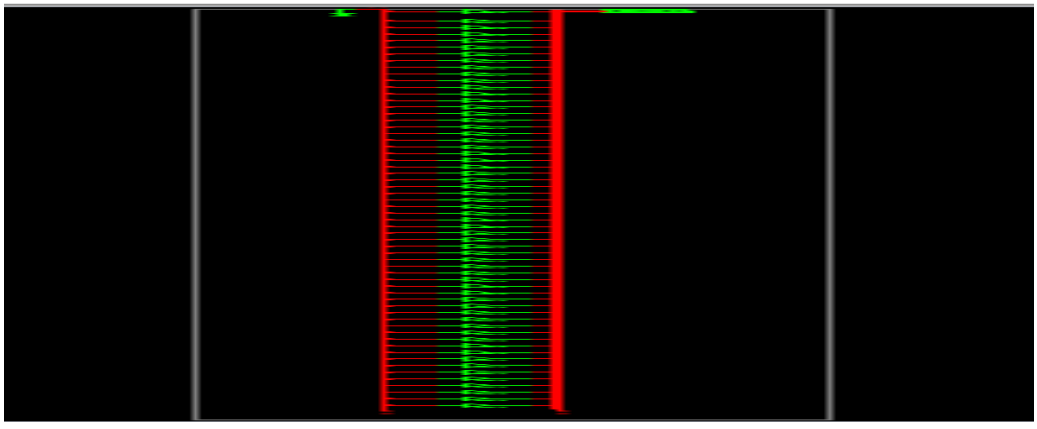
```
Data Path: m65/m3/Q to Q<255>
                                   Gate     Net
  Cell:in->out       fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FDR:C->Q                2   0.514   0.380  m65/m3/Q (m65/m3/Q)
   OBUF:I->O                   3.169          Q_255_OBUF (Q<255>)
  ----------------------------------------
  Total                        4.063ns (3.683ns logic, 0.380ns route)
                                       (90.6% logic, 9.4% route)
```

EXTENSION

RTL



Technology



Area

Device Utilization Summary (estimated values)				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	
Number of Slices	0	4656		0%
Number of bonded IOBs	256	232	110%	

Delay

```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
```

6. CONCLUSION

This paper proposes a low power and area efficient shift register using pulsed latch. The shift register reduces area and power consumption by replacing flip-flops with pulsed latch. The design and analysis of a shift register using pulsed latches with reduced power and area is proposed. In order to reduce the area the traditional data flip-flops are substituted placed with pulsed latches. The use of various non overlap delay pulsed clock signals substituted by the traditional single pulsed clock signals by this design solves the timing problem in pulsed latches. In the standard system, shift register uses single pulsed clock signal for data transition, which consumes additional power. The shift register uses a small number of the pulsed clock signals and combine the latches to many sub shifter registers and exploitation further temporary storage latches. To minimize power consumption multiple non overlap delayed pulsed clock signal design is proposed for data synchronization in an exceedingly multi bit shift register.

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