

Simulation and Analysis of 4 bit applications using 9T full adder

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Abstract—the most timing critical part of logic design usually contains one or more arithmetic operations, in which addition is commonly involved. Addition is a fundamental arithmetic operation and it is the base for arithmetic operations such as multiplication and the basic adder cell can be modified to function as subtractor by adding another XOR gate. Therefore, 1-bit Full Adder cell is the most important and basic block of an arithmetic unit of a system. Hence in order to improve the performance of the digital computer system one must improve the basic 1-bit full adder cell based application. In this paper simulate the performance of 4 bit adder- subtractor, 4 bit Carry skip adder and 4-bit multipliers are designed using 9T full adder. All the simulation results are using TSMC-0.18µM CMOS Technology.

Keywords: full adder, Power consumption, Adder, Subtractor, Multiplication.

and B with Cin yields a SUM and a Cout bit. The general equations for SUM and Cout are given below:

$$SUM = A \oplus B \oplus Cin \quad (1)$$

$$Cout = (A \oplus B)Cin + AB \quad (2)$$

I- INTRODUCTION

With the increasing level of device integration and the growth in complexity of microelectronic circuits, power dissipation, delay and area has come the primary design goal. The failure mode of high-power circuits relates to the increasing popularity of portable electronic devices. Laptop computers, pagers, portable video players and cellular phones all use batteries as a power source, which by their nature provide a limited time of operation before they require recharging. To extend battery life, low power operation is desirable in integrated circuits. Furthermore, successive generations of applications often require more computing power, placing greater demands on energy storage elements within the system. Power dissipation limitations come in two flavors. The first is related to cooling considerations when implementing high performance systems. High speed circuits dissipate large amounts of energy in a short amount of time, generating a great deal of heat as a by-product. This heat needs to be removed by the package on which integrated circuits are mounted. Heat removal may become a limiting factor if the package (PC board, system enclosure, heat sink) cannot adequately dissipate this heat, or if the required thermal components are too expensive for the application [1]. Addition is the most basic arithmetic operation and adder is the most fundamental component of any digital processor.

Outline paper

The rest of the paper is organized as follows: In section II, we present the mathematical equations which lead to construction of full adder. In section III, discussed full adder based applications. In section IV, Simulation Result table and waveform.

II-FULL ADDER [4]

We now present the mathematical equations which lead to the design of the new full adder cells. The addition of two bits A

and B with Cin yields a SUM and a Cout bit. The general equations for SUM and Cout are given below:

$$SUM = A \oplus B \oplus Cin \quad (1)$$

$$Cout = (A \oplus B)Cin + AB \quad (2)$$

These two equations can be rearranged as follows:

$$SUM = (A \oplus B)Cin' + (A \odot B)Cin \quad (3)$$

$$Cout = (A \odot B)Cin' + (A \oplus B)Cin \quad (4)$$

From the above equation it is clear that the adder cells can be designed by using XOR and XNOR gates. The above given expression can be rearranged to obtain different circuits for the adder cell.

Rajeev Kumar et al.[4], In this paper designed an 1 bit full adder cell using XOR-XNOR gate and also calculate the power dissipation, propagation delay and power-delay product of the designed adders have been compared with the existing adders and are found to be efficient.

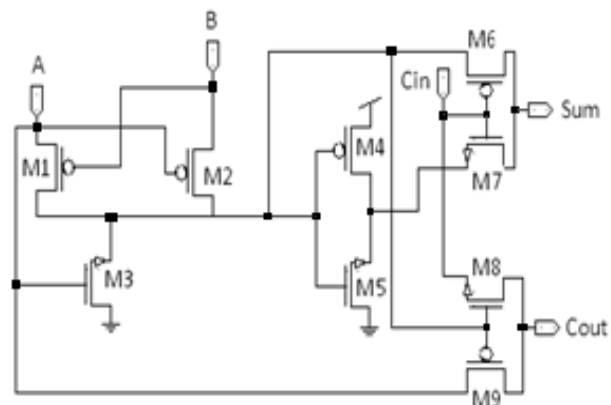


Fig.1. 9T Full Adder based on XOR-XNOR gate [4]

III-9 T full adder based applications

(A) ARCHITECTURE OF CARRY SKIP ADDER

The carry skip adder provides a compromise between a ripple carry adder and a CLA adder. The carry skip adder divides the words to be added into blocks. Within each block, ripple carry is used to produce the sum bit and the carry. The Carry Skip Adder reduces the delay due to the carry computation i.e. by skipping over groups of consecutive adder stages [6].

- If each $A_i \neq B_i$ in a group, then we do not need to compute the new value of C_{i+1} for that block; the carry-in of the block can be propagated directly to the next block.
- If $A_i = B_i = 1$ for some i in the group, a carry is generated which may be propagated up to the output of that group.
- If $A_i = B_i = 0$, a carry, will not be propagated by that bit location. The basic idea of a carry-skip adder is to detect if in each group all $A_i \neq B_i$ and enable the block's carry-in to skip the block when this happens as shown in figure1. In general a block-skip delay can be different from the delay due to the propagation of a carry to the next bit position [7] [8].

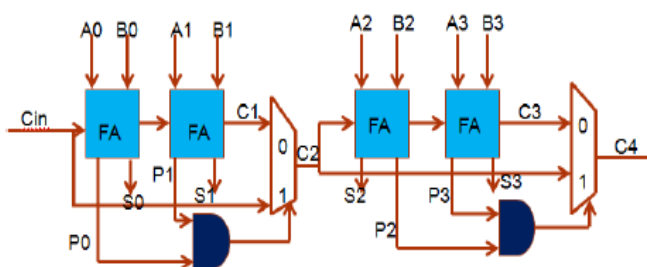


Fig.2 Architectural block of 4-bit Carry Skip Adder (CSKA)

(B) 4-Bit Adder-Subtractor

When the addition of 2 two's complement binary numbers produces a final carries, it can be ignored. However, it is necessary to detect the overflow that can occur when the result of the addition is out of range. It was concluded that an arithmetic overflow could be detected if the carry in and carry out of the most significant bit position are different. Thus, the overflow can be detected with one additional Exclusive-OR gate. The two's complement adder is not much different from the binary adder for unsigned numbers.

What about subtraction? We already suggested that subtraction should be carried out by complementing the subtrahend and adding. So the task is to design a circuit whose output is the two's complement of the input, and use its output as one input to an adder. Such a circuit can be designed easily, but why should a system contain some hardware dedicated to addition and other hardware dedicated to subtraction? If the only difference between these two circuits is a circuit that computes the two's complement, then why not design a circuit where either addition or subtraction can be selected with one additional input? When this additional input is, say, 0 the circuit performs addition, and when the input is 1 the circuit performs subtraction.

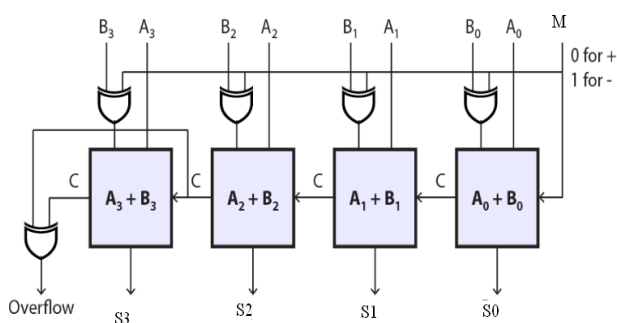


Fig.3 block diagram of 4- Bit Adder-subtractor

(C). MULTIPLIER ARCHITECTURES

The wide-bit addition is vital in many applications such as ALUs, multiply-and accumulates (MAC) units in DSPs, and , versatile microprocessor. It is also important for the performance of direct digital frequency synthesizers (DDFSs) where it is used as a phase accumulator. Numerous multiplier implementations exist whereas some are good for low power dissipation and some takes least propagation delay. In multiplication, multiplicand is added to itself a number of times as specified by the multiplier to generate product. In this section, two different 4-bit multiplier architectures are designed.

4 bit Tree Multiplier

C. S. Wallace suggested a fast technique to perform multiplication in 1964 [9]. The amount of hardware required to perform this style of multiplication is large but the delay is near optimal. The delay is proportional to $\log(N)$ for column compression multipliers where N is the word length. This architecture is used where speed is the main concern not the layout regularity. This class of multipliers is based on reduction tree in which different schemes of compression of partial product bits can be implemented. In tree multiplier partial-sum adders are arranged in a treelike fashion, reducing both the critical path and the number of adders needed as shown in the figure 5, shown below:

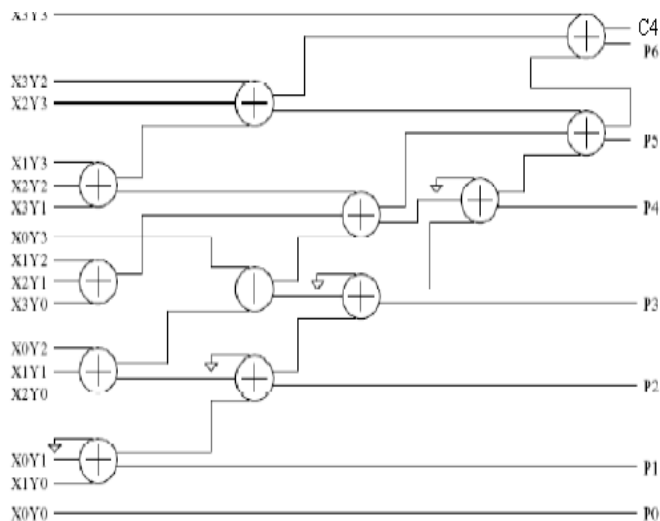


Fig 4: 4-bit Tree Multiplier (TM)

The partial products or multiples are generated simultaneously by using a collection of AND Gates. The multiples are added in combinational partial products reduction tree using carry save adders, which reduces them to two operands for the final addition. The results from CSA are in redundant form. Finally, the redundant result is converted into standard binary output at the bottom by the use of CPA [10].

IV-Simulation result

All schematic simulations are performed on Tanner EDA tool version 13.0 at 180nm technology with input and supply voltage 5V.

The performance of the power consumption 4-bit adder-subtractor, 4 bit carry skip adder and 4*4 bit tree multiplier as shown in table 1:

| Full adder based applications | Power consumption (pW) |
|-------------------------------|------------------------|
| 4 bit adder- subtractor | 4.39 |
| 4 bit Carry Skip Adder | 0.0019 |
| 4*4 tree multiplier | 104.99 |

In 4-bit Carry Skip Adder (CSKA) the input combination of [A0 A1 A2 A3 all bits are 1] + [B0 B1 B2 B3 all bits are 0] & Cin=0 and output as shown the waveform figure 5.

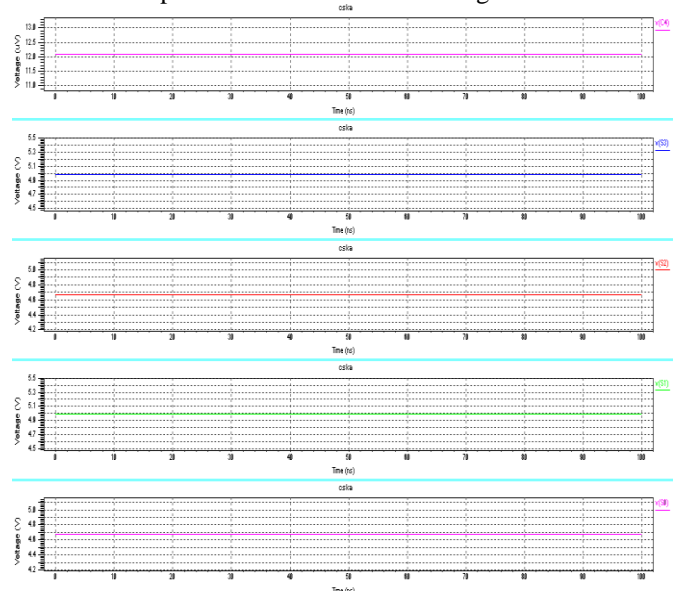


Figure 5– Waveform of 4-bit Carry Skip Adder (CSKA)

In 4-bit adder –subtractor the input combination of [A0 A1 A2 A3 all bits are 1] + [B0 B1 B2 B3 all bits are 1] & M0=0 for adder & M0=1 for subtractor, output as shown the waveform figure 6 & 7.

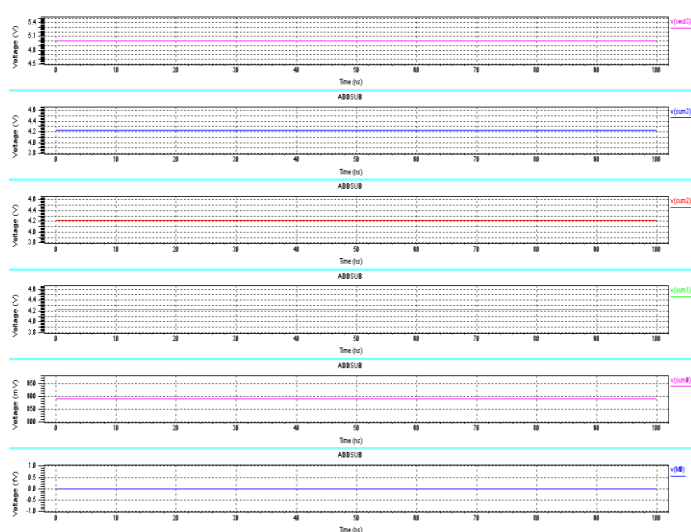


Figure 6: Waveform of 4- Bit Adder

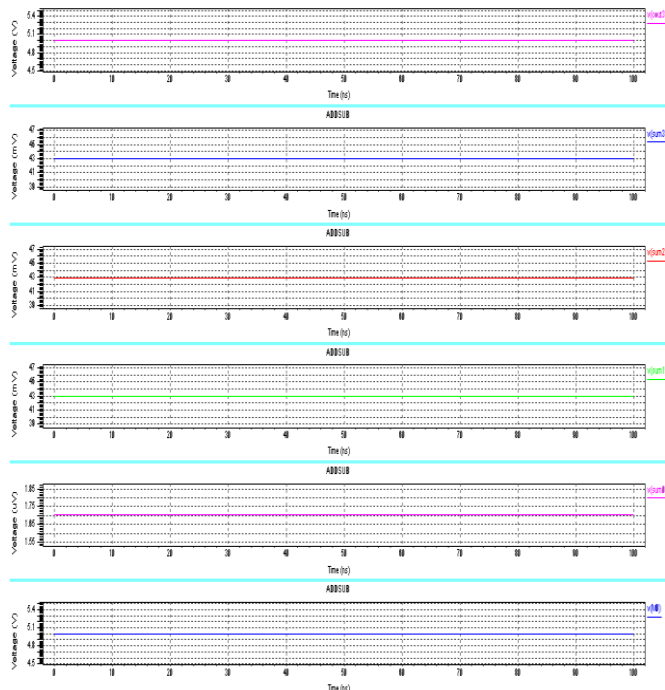


Figure.7: Waveform of 4- Bit subtractor

In 4*4-bit tree multiplier the input combination of [A0 A1 A2 A3 all bits are 0] + [B0 B1 B2 B3 all bits are 0] & Cin=0 .the output as shown the waveform figure 8.

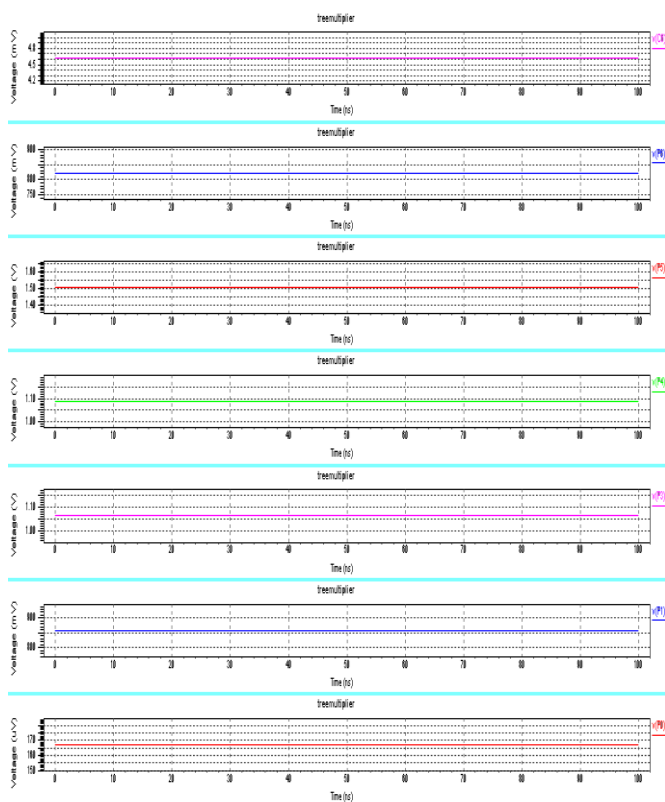


Figure.8 4 bit tree multiplier

CONCLUSION

In microprocessors, arithmetic's operation is performed in a variety of forms in hardware and Software using addition,

subtractor and multipliers and other reductions of power in arithmetic's operation are great importance in digital signal processors. Hence addition, subtractor and multiplier are designed by using full adder circuit. Then the performance parameters of arithmetic operation are determined. In this paper simulate the performance of 4 bit adder- subtractor, 4 bit Carry skip adder and 4-bit multipliers using TSMC-0.18 μ m CMOS Technology.

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REFERENCES

1. Chandrakasan, A., and Brodersen, Low Power Digital Design, Kluwer Academic Publishers, 1995
2. Weste, N., and Eshragian, K., Principles of CMOS VLSI Design: A Systems Perspective, Pearson Addison-Wesley Publishers, 2005.
3. Bellaouar, A., and Elmasry, M., Low-Power Digital VLSI Design: Circuits and Systems Boston, Massachusetts: Kluwer Academic Publishers, 1995.
4. Rajeev Kumar, Sandeep Gautam, Izhar Ahmed, Vishal Ramola, "A New design of 1-bit full adder based on XOR-XNOR gate" International Journal of Enhanced Research in Science Technology & Engineering, ISSN: 2319-7463 Vol. 3 Issue 6, June-2014, pp: (81-85), Available online at: www.erpublications.com.
5. Gupta, A., Design Explorations of VLSI Arithmetic Circuits, Ph.D. Thesis, BITS, Pilani, India, 2003.
6. L. Bisdounis, D.Gouvetas, and O.Koufopavlou., —A Comparative study of CMOS circuit design styles for low power high-speed VLSI circuits, Int. J. of Electronics, vol.84, no. 6, 1998, pp. 599-613.
7. A.Gupta. —Design Explorations of VLSI Arithmetic Circuits, Ph.D. Thesis, BITS, Pilani, India, 2003.
8. Guyot Alain, Hochet Bertrand, and Muller Jean-Michel. "A Way to Build Efficient Carry-Skip Adders", IEEE Transactions on Computers C, vol.30, October, 2010, pp.1144-1151.
9. Wallace, C.S., "A Suggestion for a Fast Multiplier", IEEE Transactions on Electronic Computers, EC-13, pp. 14-17, 1964.
10. Parhami, B., "Computer Arithmetic – Algorithms and Hardware Designs", Oxford University Press, 2000.
11. Bellaouar, A., and Elmasry, M. I., Low-Power Digital VLSI Design: Circuits and Systems, Kluwer, Norwell, MA, 1995.
12. Rabaey, J.M., Chandrakasan, A., and Nikolic, B., "Digital Integrated Circuits", Second Edition, PHI Publishers, 2003.
13. John P. Uyemura, "Introduction to VLSI Circuits and Systems," Wiley, John & Sons, Inc., 2002.
14. R. Kumar. V.K. Pandey, "A New 5-Transistor XOR-XNOR Circuit Based on The Pass Transistor Logic", University of Mumbai, IEEE International Conference, Dec-2011
15. J. Wang, S. Fang and W. Feng, "New Efficient Designs for the XOR and XNOR Functions on the Transistor Level", IEEE Journal of Solid-State Circuits, Vol. 29, No. 7, July 1994.
16. E. Abu-Shama, and M. Bayoumi, "A New Cell for Low Power Adders," Proc. Int. Symp. on Circuits and Systems, vol. 4, pp. 49-52, 1996.
17. H. Lee and G. E. Sobelman, "A New Low-Voltage Full Adder Circuit," Proc. IEEE Great Lakes Symp. on VLSI 97, pp. 88-92, 1997.
18. Santanu Maity, Bishnu Prasad De, Aditya Kr. Singh, "Design and Implementation of Low-Power High-Performance Carry Skip Adder" International Journal of