

Modelling & Simulation of Three-phase Induction Motor Fed by an asymmetrically Configured Hybrid Multilevel Inverter

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Abstract

Multilevel inverters (MLIs) have become viable solution for high power DC-AC conversion. They are especially advantageous for induction motors because of low dv/dt stress and low common mode voltages. Quality of a multilevel waveform is enhanced by increasing the number of levels. However, for increased number of levels, component count becomes very high. In this paper an asymmetrically configured hybrid inverter is employed for a three-phase induction motor, resulting in low device count as compared to the classical topologies. MATLAB/Simulink based models are used to simulate and validate the proposed concepts. .

Keywords

Multilevel inverters, hybrid topologies, asymmetric source configuration

1. Introduction

In last few decades, multilevel voltage source inverters have emerged as cost-effective and efficient solution for high power DC to AC conversion [1]. A multilevel inverter (MLI) comprises multiple input DC levels and power semiconductor devices to synthesize a stepped waveform. The voltage stresses borne by the power switches are lower as compared to the overall operating voltage level [2]. In addition, the output waveform has better harmonic profile as compared to the two level waveform obtained from the conventional inverters. Other advantages are higher efficiency and reduced dv/dt stresses on the load [3]. Attempts are also being made to employ MLIs for low power applications [4-6].

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Quality of the multilevel waveform is enhanced as number of levels increases, but it leads to necessity of a large number of power semiconductor devices and accompanying gate driver circuits, making the overall system complex and expensive [7]. Increasing number of levels also reduces the dv/dt stresses on the load and this is especially advantageous for induction motors fed with an inverter.

Multilevel topologies which are commercially available are: neutral point clamped (NPC) converters, cascaded H-bridge (CHB) converters and flying capacitors (FC) converters. Amongst these, the CHB topology offers higher reliability due to its modularity [7]. The CHB structure in series consists of several single-phase full bridge inverters also called 'cells'. However, for increased number of output levels, number of power switches number of switches conducting simultaneously and overall cost of the system increase significantly. Many modifications are being sought in the classical topologies to overcome these challenges. One of the simplest ways to increase number of levels using the same topology is to implement asymmetrical sources (i.e. two or more input DC sources are unequal) [7]. Decrease in component count, however, comes in this case at the cost of increased voltage rating of power switches.

In this paper, a newly proposed multilevel structure [8] is extended for asymmetric source configuration for a three-phase induction motor. The aforesaid topology leads to reduction in the count of power switches for a large number of levels in the output. Rest of the paper is organized as follows. In section 2, the three-phase multilevel topology is introduced. In section 3, the overall system with the multilevel inverter and three-phase induction motor is described. In section 4, simulation results are presented and in section 5, conclusions are drawn.

2. Three - phase multilevel inverter with Asymmetrically Configured Sources

A new topology is proposed in [8] with floating sources connected in cross fashion as shown in Fig.1. The topology utilizes only bidirectional-conducting-unidirectional-blocking power switches and electrically isolated input DC sources.

For n number of input DC sources, the topology would require '2n+2' number of power switches whereas a classical cascaded H-bridge topology would require '4n' number of power switches.

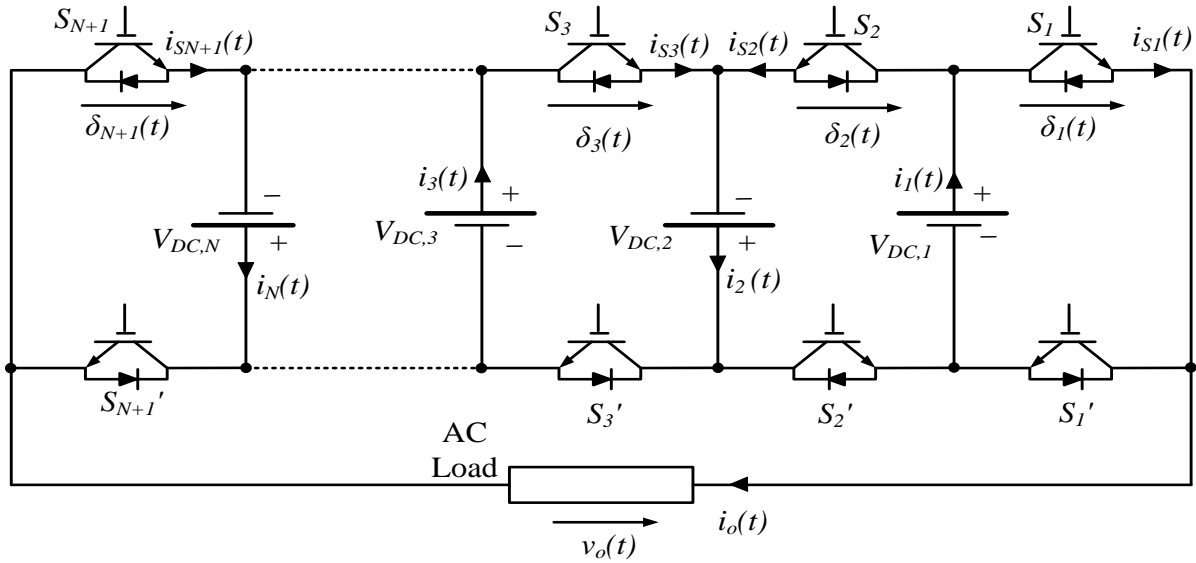


Fig.1. General Structure of topology proposed in [8]

Input DC sources in a multilevel inverter can be configured in symmetric and asymmetric fashions. Considering four input sources viz. V_1, V_2, V_3 and V_4 , the source configuration is designated as 'symmetric' when:

$$V_1 = V_2 = V_3 = V_4 = V_{DC} \quad (1)$$

When the values of input DC sources are different, the configuration is known as an 'asymmetric' source configuration. Two conventional asymmetric source configurations are:

(1) Binary Configuration :

Binary configuration is based on geometric progression (GP), i.e. the succeeding source has value equal to twice the preceding source. This means:

$$V_1 = V_{DC}, V_2 = 2V_{DC}, V_3 = 3V_{DC} \text{ and } V_4 = 4V_{DC} \quad (2)$$

(2) Trinary Configuration :

Trinary configuration is also based on geometric progression (GP), i.e. the succeeding source has value equal to thrice the preceding source. This means:

$$V_1 = V_{DC}, V_2 = 3V_{DC}, V_3 = 9V_{DC} \text{ and } V_4 = 27V_{DC} \quad (3)$$

Asymmetric source configurations lead to a significant decrease in number of power switches in the cascaded H-bridge topology. For example, a CHB structure with two binary sources can synthesize seven levels with eight switches while a classical CHB would require twelve switches to synthesize seven levels. Similarly, a CHB structure with trinary configuration would synthesize twenty seven levels with eight switches whereas a classical CHB would require fifty power switches for the same.

Thus, by employing asymmetric source configuration, number of power switches can be further

reduced for the topology shown in Fig.1. But while a CHB structure can synthesize all possibilities of additive and subtractive combinations of the input levels, the topology shown in fig.1 cannot do the same because of the limitations posed by the structure itself.

Because of the configurationally limitations posed by the topology, GP based asymmetric source configurations cannot be employed in the topology. Arithmetic progression (AP) based asymmetric source configuration is can be used in the so-called cross-connected source based multilevel inverter (CCS-MLI). That is to say, for four input sources, the source values are $V_{DC}, 2V_{DC}, 3V_{DC}$ and $4V_{DC}$. These sources need to be properly placed so that the output waveform has equal sized steps. For achieving this, the algorithm should be:

$V_1 = V_{DC}$
$V_2 = 3V_{DC}$
$V_3 = 4V_{DC}$
$V_4 = 2V_{DC}$

The asymmetric source configuration leads to further decrease in number of power switches. For example, the topology with symmetric source configuration would require 22 switches while it would require only 10 switches with the proposed source configuration. Moreover, a classical CHB structure would need 40 switches for the same.

The aforesaid configuration can synthesize 21 levels in the output waveform, from $-10V_{DC}$ to $+10V_{DC}$ in steps of V_{DC} . Thus the waveform will have a peak value of $10V_{DC}$. The three-phase structure with two DC sources in each phase is shown in fig.2 which has a star connection. A delta connected structure is shown in fig.3.

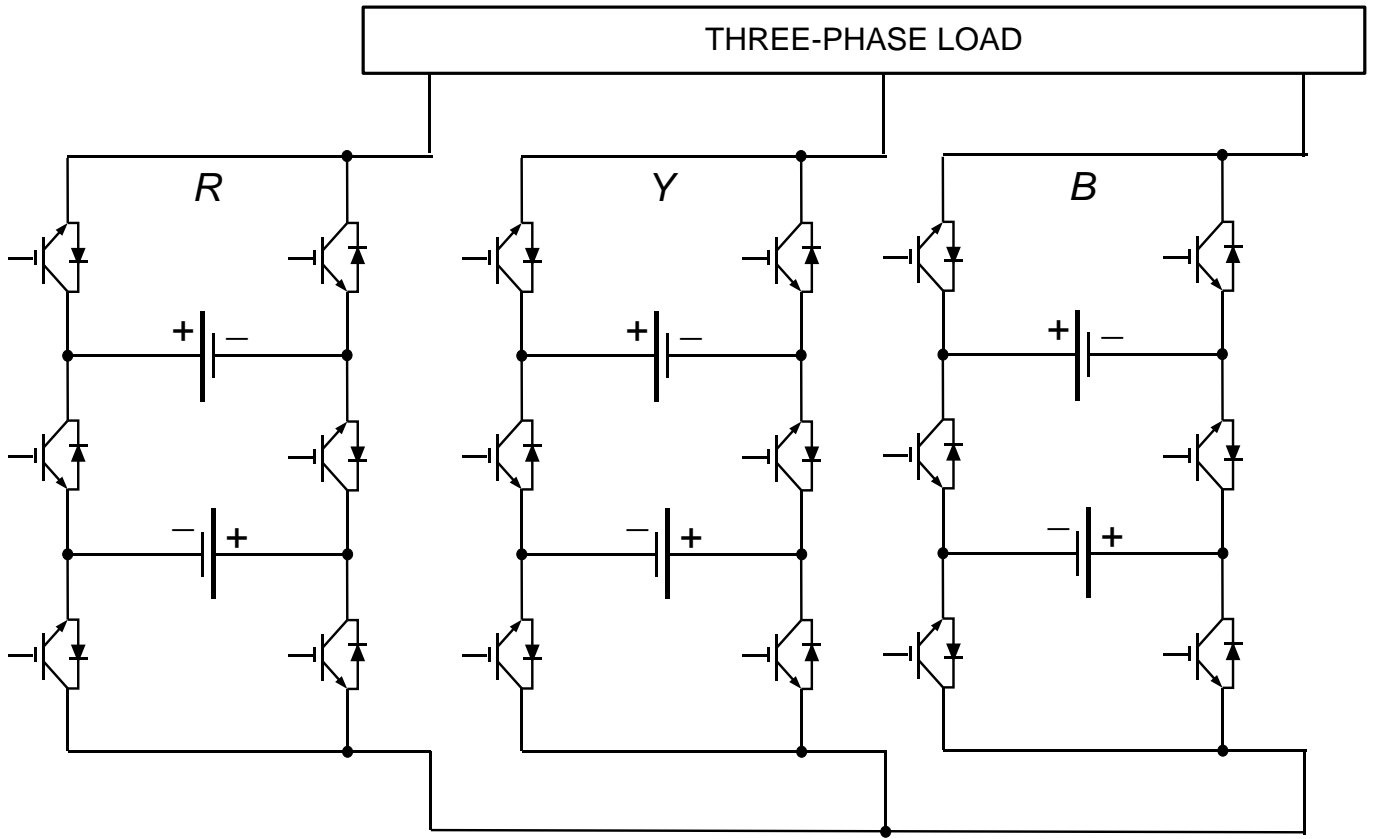


Fig.2. A three-phase star connected configuration of CCS-MLI with asymmetric sources

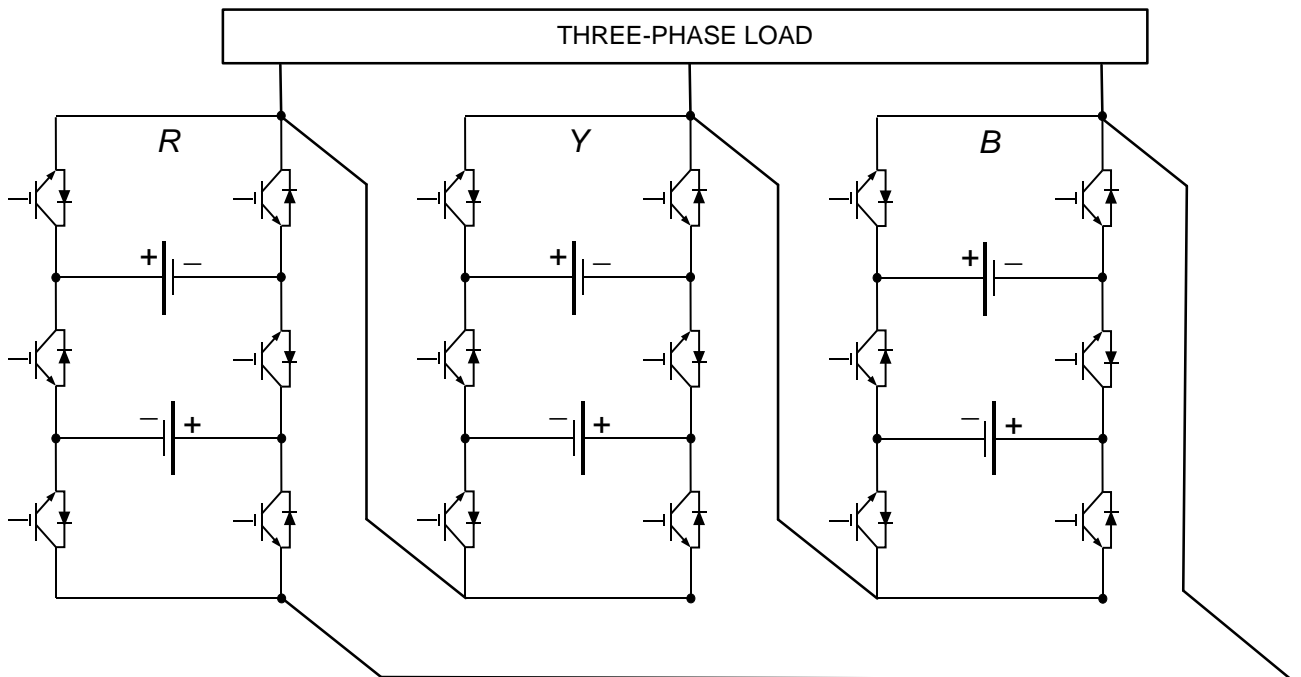


Fig.3. A three-phase delta connected configuration of CCS-MLI with asymmetric sources

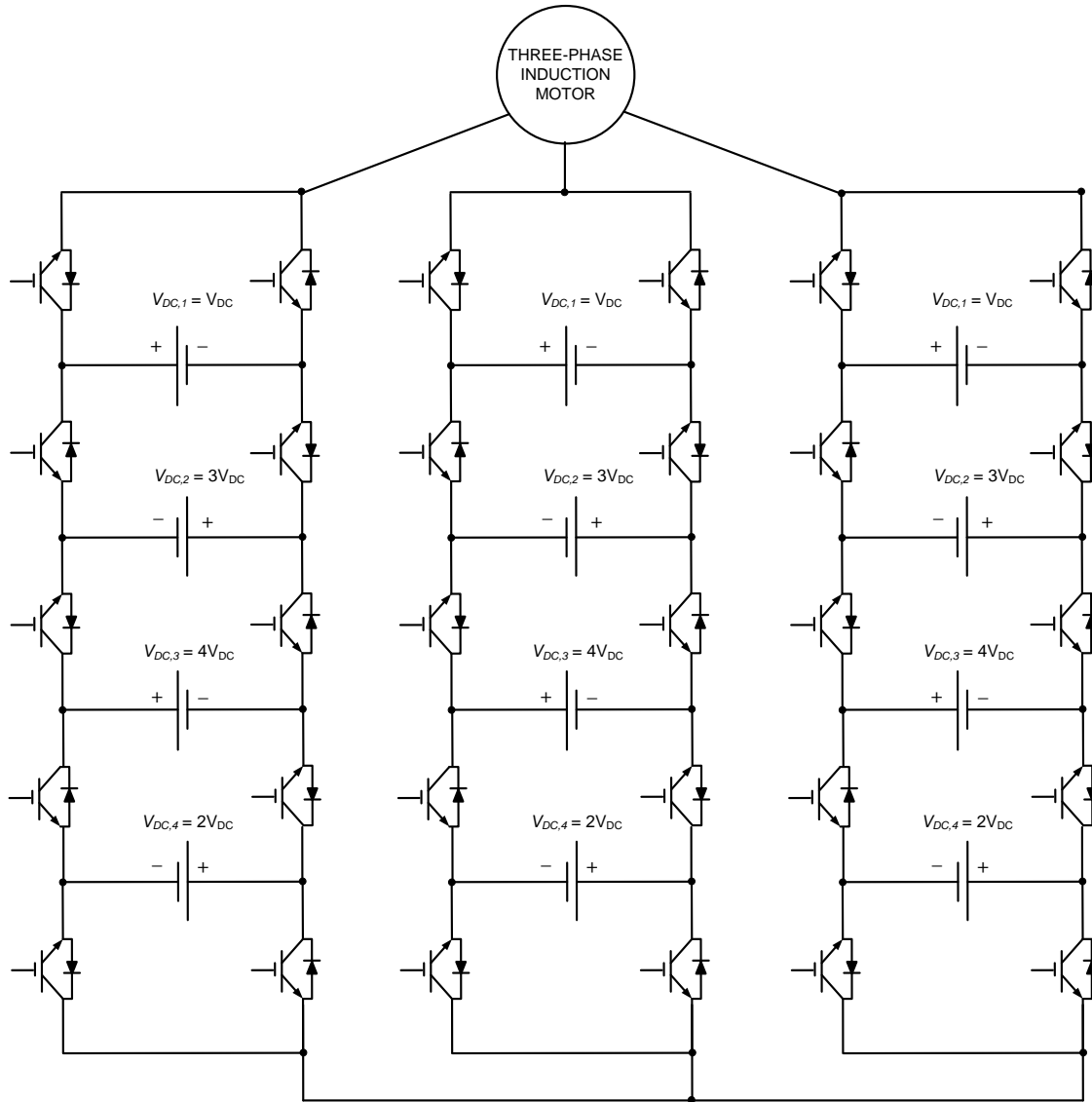


Fig.4. A three-phase system based on CCS-MLI with four input sources in each leg

3. System Description

In order to verify the performance of CCS-MLI with asymmetric source configuration for a three-phase induction motor, MATLAB/Simulink based modelling is used to obtain simulated results. Each leg has four input DC sources which are asymmetrically configured in a natural number sequence. A power circuit based on fig. 4 is utilized to model the system using MATLAB/Simulink. The three legs are connected in star. Sine-triangle based PWM technique is implemented. A sinusoidal waveform with 50 Hz frequency is used as the reference and twenty phase opposition-disposed triangular waveforms with frequency 100 Hz are used as carrier signals. Value of V_{DC} used is 32V. A three-phase induction motor rated at 50 HP, 400V, 50 Hz, 1480 RPM is used as a load. The aforesaid configuration is expected to synthesize twenty-one levels in

the phase voltage in steps of 32 V. The peak voltage would be 320 V. As far as the line voltage is concerned, it would have forty one levels. A load torque of 17Nm is applied. Ratings of the motor are summarized in table1.

Table 1 Motor Parameters

Power	50 HP
Voltage	400 V
Frequency	50 Hz
Speed	1480 RPM

4. Simulation Results

The MATLAB/Simulink based simulation model is shown in fig.5.

Parameter	Description
Number of phases	3

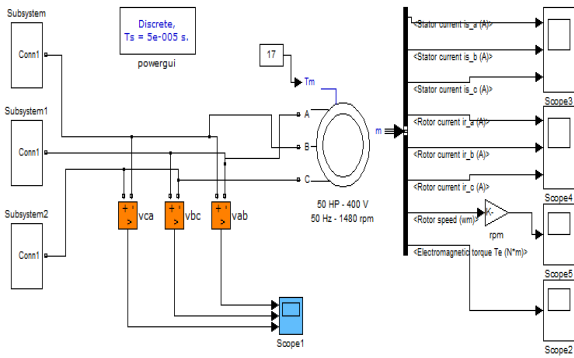


Fig.5. Simulation model for the proposed system

Phase voltage and line voltage are shown in fig. 6 and fig.7. respectively. Stator current is shown in fig.8.

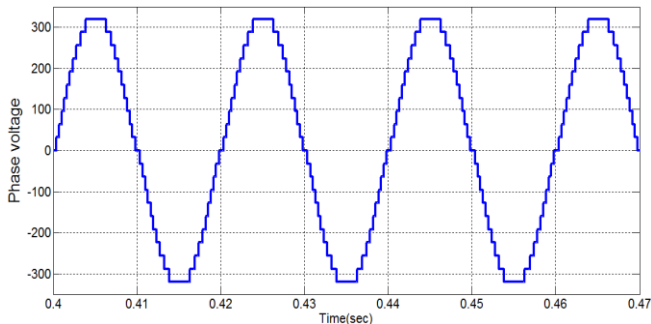


Fig.6. Phase voltage waveform for the proposed system

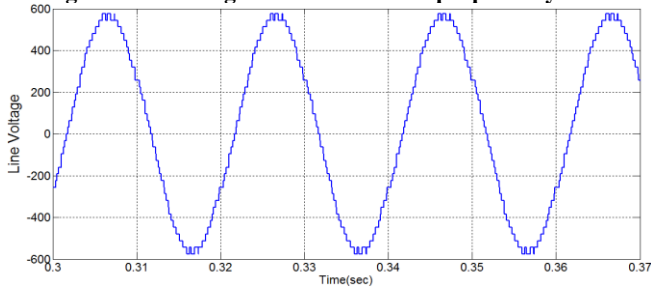


Fig.7. Line voltage waveform for the proposed system

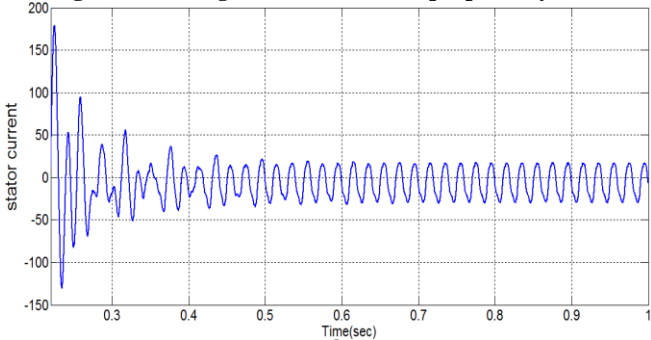


Fig.8. Stator current waveform of the induction motor for the proposed system

It can be seen that the phase voltage has twenty one levels while the line voltage has forty two levels. As a result, the line current for the stator winding of the motor is sinusoidal in nature.

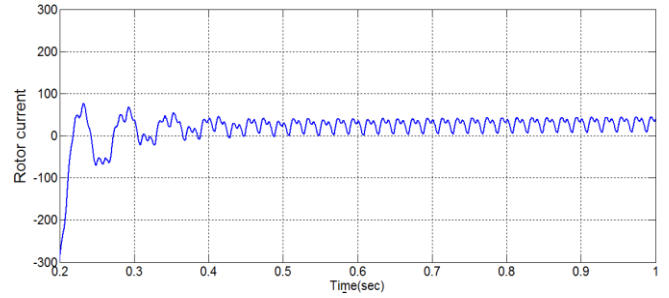


Fig.9. Rotor current waveform of the induction motor for the proposed system

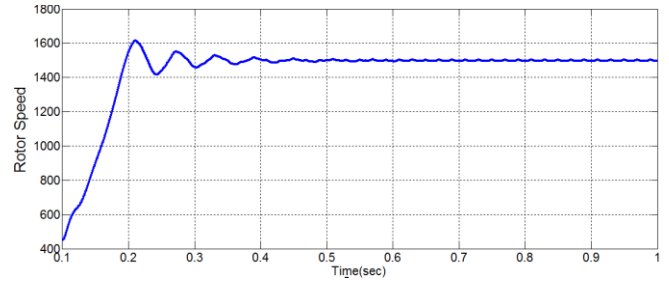


Fig.10. Rotor speed waveform of the induction motor

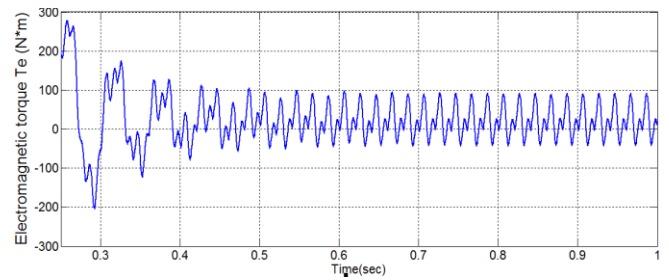


Fig.11. Waveform for electromagnetic torque

Rotor current waveform, speed waveform and waveform for electromagnetic waveform are respectively shown in figures 9, 10 and 11 respectively. It can be seen that satisfactory results are obtained.

5. Conclusion

A multilevel inverter based three-phase system is proposed in this paper. Cross-connected sources based multilevel inverter (CCS-MLI) topology is implemented with asymmetric source configuration. Four sources with natural number sequence of sources with proper placement are used in each phase. Satisfactory results are obtained with the simulations carried out using MATLAB/Simulink.

References

- [1] Franquelo L. G., Rodriguez J. L., Leon J., S. Kouro, Portillo R., Prats M.A.: 'The age of multilevel converters arrives'. IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [2] Rodriguez J., Franquelo L.G., Kouro S., Leon, J.I., Portillo R.C., Prats M.A.M., and Perez M.A.: 'Multilevel Converters: An Enabling Technology for High-Power Applications'. Proceedings of the IEEE, vol.97, no.11, pp.1786-1817, Nov. 2009
- [3] Rodriguez J., Lai J.S., Peng F.Z.: 'Multilevel inverters: A survey of topologies, controls, and applications'. IEEE Trans. Ind. Electron., vol.49, no. 4, pp. 724–738, Aug. 2002.

- [4] Liu, Y.; Luo, F.L.; "Multilevel inverter with the ability of self-voltage balancing," Electric Power Applications, IEE Proceedings - , vol.153, no.1, pp. 105- 115, 1 Jan. 2006.
- [5] De, S.; Banerjee, D.; Siva Kumar, K.; Gopakumar, K.; Ramchand, R.; Patel, C.; , "Multilevel inverters for low-power application," Power Electronics, IET , vol.4, no.4, pp.384-392, April 2011.
- [6] Hua, C.-C.; Wu, C.-W.; Chuang, C.-W.;; "A novel dc voltage charge balance control for cascaded inverters," Power Electronics, IET , vol.2,no.2, pp.147-155, March 2009
- [7] Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Pérez, M.A.; , "A Survey on Cascaded Multilevel Inverters," Industrial Electronics, IEEE Transactions on , vol.57, no.7, pp.2197-2206, July 2010.
- [8] Gupta, K.K. and Jain, S.: "Theoretical analysis and experimental validation of a novel multilevel inverter topology for renewable energy interfacing applications," AIP Journal of Renewable and Sustainable Energy (JRSE), vol.4, issue 1, 2012.



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