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Reconfigurable Fir Filter Architecture for EEG Application

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Abstract:
Filters play an important role in noise removal. There are many different types of filter architecture that have been proposed. Reconfigurable architectures of FIR filter are used in application like software defined radio (SDR) which support multistand communication and also in medical application. In this designed work Reconfigurable Finite Impulse Response (FIR) filter is designed for Electro Encephalo-Gram (EEG) application. The filter is in transpose form which support pipelining and multiple constant multiplications (MCM). Area and delay is calculated on FPGA using XILINX 14.2 software and filtering of EEG signal using MATLAB 2013a. The design is less complex utilizing less area and delay. The overall delay for block size 8 was 12.17ns and frequency 167.57 MHz
Keywords: FPGA, FIR Filter, XILINX 14.2, MCM, Area-Delay, EEG.

1. Introduction

Filters play a role in applications such as speech processing, image processing, echo cancellation, noise cancellation, software defined radio etc. filters are basically classified into analog and digital. In this paper digital filter is used. These are further classified into IIR and FIR filters. Many applications require FIR Filter in order to meet frequency specifications. FIR filters have advantage over infinite impulse response (IIR) as they are easy to design and support high sampling rate. The number of multiplication and addition operations increases as the filter order increases. FIR filters can be made linear phase by making filter coefficients symmetrical where quantized values of impulse response of frequency transfer H(f) is h(n) in FIR filter . These remain constant and are known priori in signal processing applications.

EEG contains four different types of signals alpha, beta, delta and theta ranging from 8-14Hz, 14-50Hz, 0.5-14Hz and 14-50Hz respectively. Signals ranging out of these are treated as noises or artifacts. These can be from eye blinks, motion artifacts, impedance of wires etc. Therefore, to remove the noise content of signal, in [7] Lab-View platform is used for epileptic seizure detection using statistical analysis.

Many researchers have suggested different design styles for filters by making use of Distributed Arithmetic (DA) and MCM methods. DA based designs utilize look up tables to store values, thereby reducing design complexity. The MCM technique reduces number of addition steps in multiplication operations. This method is more suitable for FIR filter designing and implementation. These can be implemented in transpose form but not in direct form configuration of FIR filter.

Another way that is popular is block processing which gives higher throughput. The area-delay efficiency is also improved in this. Block processing is straight forward. When direct form configuration of FIR filter is derived. In transpose form block processing is not supported directly. In order to make FIR filters more efficient advantages of both MCM and Block processing is combined. It is realized in transpose form as they have pipelining nature and provide high operating frequency in order to support higher sampling rate and block processing for higher throughput.

2. References

Chen and Chiueh [1] have proposed a reconfigurable FIR filter (RFIR) where a non-zero canonic sign digit values are modified to reduce precision of filter coefficients without significant

impact on filter behaviour. This design is not area delay efficient. The architecture suits only lower order filter. Constant shift method and programmable shift method has been proposed in [2] for RFIR for SDR channelizer. The SDR channelizer need reconfigurable FIR filter in order to support multistand wireless communication. Sang Yoon Park et al. [3] proposed an efficient distributed arithmetic (DA) based approach for high throughput reconfigurable implementation of finite impulse response (FIR) filters. The filter coefficients change during runtime. J. Park, et al. presented [5] a programmable digital finite impulse response (FIR) filter for high-performance and low-power applications. The architecture can be used in low complexity programmable FIR filter design. It is based on a computation sharing multiplier (CSHM) which targets computation re-use in vector-scalar products.

In some multiplier based structure either transpose or direct form is used. DA based architecture used direct form and multiplier less based architecture used transpose form. Block based filters are inefficient for large filter length and variable coefficients. They are suitable only for 2D filters and block least mean square (BLMS). In this work MCM technique and pipelining is used for area delay efficiency to realise large order FIR filter for both fixed and reconfigurable application.

EEG signals contain artifacts (noise) along with required data signals of the brain. These noises can be filtered using different filters like high pass, low pass, band-pass, etc depending on the requirement of actual data. Different diseases like sleep disorders, epilepsy, seizures etc can be detected through EEG signals. Various artifacts such as PLI (Power line interference), MA (Muscle artifact), and EBA (Eye blink artifact) are present during recording the EEG. Overview of various artifacts which occur in EEG signal is mentioned in [6]..

The work presents reconfigurable architecture that can be used for EEG filtering as it occupies less area and is also efficient. Paper is organized into sections as section I introduction, section II references, section III proposed system, section IV results and section V conclusion.

3. Proposed System

In enhanced design, the block FIR filter is presented for fixed filter which uses MCM scheme. Coefficients of filter play a main role. In applications like SDR FIR filters must be of different specifications. Hence they require RFIR to support multistand communication. The proposed structure is in transpose form for reconfigurable application.

Coefficient storage unit (CSU), register unit (RU), inner product unit (IPU) and pipelined adder unit (PAU) are present in the architecture. Coefficients of filters used are stored in CSU which is implemented using ROM LUTs. The RU receives input values x_k and produces S_k^0 values in parallel. The IPU receives M vectors from CSU such that produces (m+1)th IPU gets c_{M-m-1} from CSU and L rows of S_k^0 form RU. The IPU contains inner product cells (IPC) which receives rows of S_k^0 and coefficient vector c_m to calculate inner product r(kL-1). Here the block size is L=8. PAU finally adds generated partial products.

The output of filter of length N can be computed using

$$y(n) = \sum_{i=0}^{N-1} h(i) \cdot x(n-i). \quad \ldots. 1$$

With L new input samples for transpose form of block filter which produce L output samples the output y_k of kth block is

$$y_k = X_k \cdot h \quad \ldots.2$$

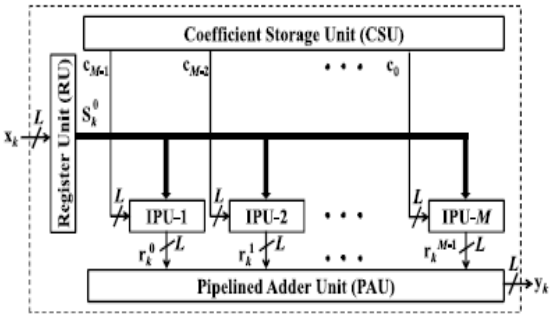


Figure. 1 Block Diagram

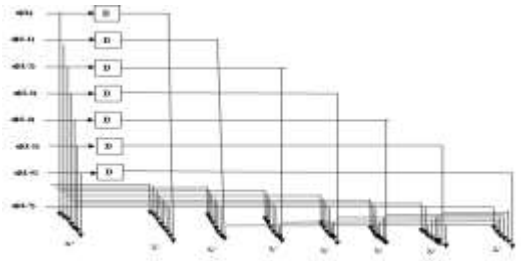


Figure. 2 Register Unit

Where $X_k = [\ x_k^0\ x_k^1\ x_k^2\ \ldots\ldots x_k^{N-1}]$

$$h = [\ h(0)\ ,\ h(1)\ ,\ h(2)\ \ldots\ldots\ h(N-1)\ ]^T \quad \ldots3$$

The coefficient vector h is decomposed into smaller weights

c_m = [h(mL), h(mL+1) **,…..,** h(mL+L-1)] ….4

$S_k^m = S_{k-m}^0$ ….5

S_k^m is symmetric. S_k^m is m clock cycle delayed with respect to S_k^0. Therefore

$y_k = \Sigma_{m=0}^{M-1} r_k^m$ ...6

where $r_k^m = S_{k-m}^0 \cdot c_m$.

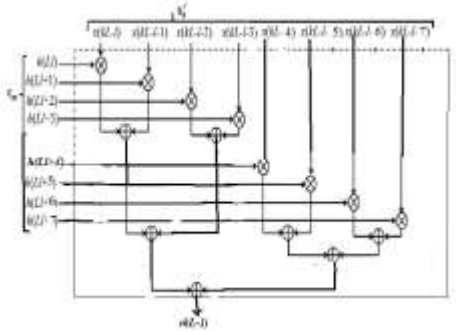


Figure. 3. Inner Product Cell

For fixed coefficient, CSU and IPU are not required. Symmetric input matrix S_k^0 is used for MCM implementation. It performs horizontal as well as vertical addition using common sub-expression elimination.

The MCM structure for FIR filter is implemented for L=8. Shift and add multiplication algorithm is implemented in MCM blocks to produce inner products. These values are finally added in Pipelined Adder Unit to obtain final output of filter.

For EEG application the filter used is Low pass FIR filter with hamming window technique. The coefficients are calculated using MATLAB Filter Design Tool (FDA). The dataset is obtained from [10] whose spectral bandwidth is 0.5-85Hz. Hamming window is used [7] with cutoff frequency 32 Hz and frequency sampling rate of signal is 173.6 Hz.

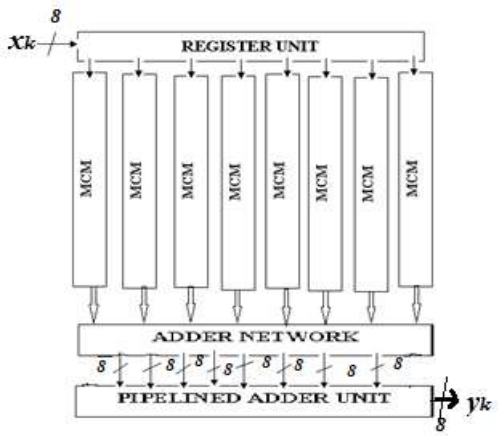


Figure. 4 Proposed block diagram

4. Simulation result

Simulation result obtained is shown in fig 5. Xilinx ISE simulator is used for simulation. The proposed system has better frequency rate and delay when compared to existing system. It even consumes lesser area. The simulation is done for EEG values [10].

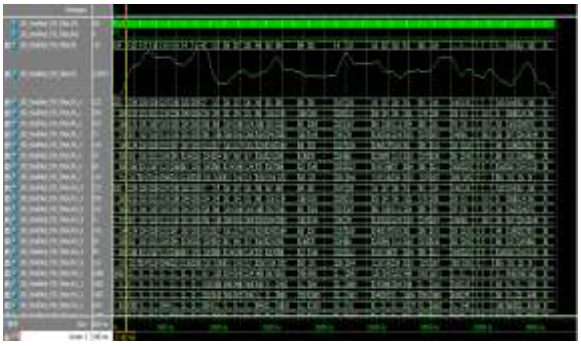
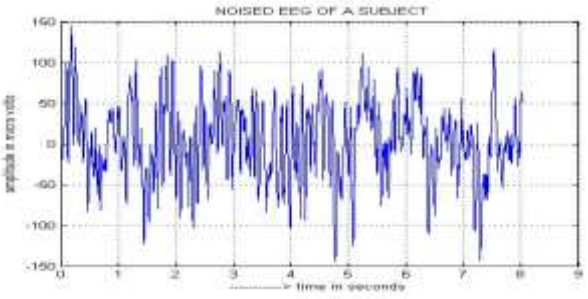


Figure 5 Simulation of proposed system

EEG signal from dataset collected is filtered using FIR filter designed in MATLAB. In the acquired dataset only one segment is filtered and shown in fig. 6 where the fig a is a segment of EEG data signal, fib b the filtered signal. The signal is open eye condition of a person which is the artifact in the data.



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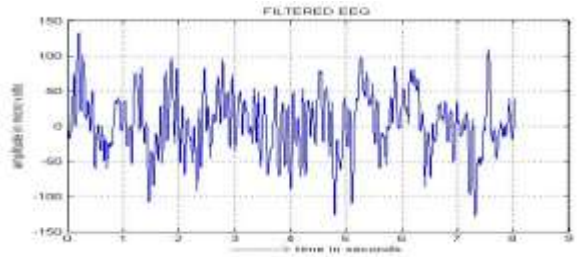

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Figure**. 6 a) EEG signal b) filtered signal**

Table-1 shows the area and delay comparison between the existing and proposed architecture.

Table 1. Comparison between existing and proposed

Sl no.	Resources	Existing system	Proposed system
1.	Slice Registers	961	811
2.	Slice LUTs	4092	1839
3.	LUT Flip Flop pairs	814	1980
4.	IO utilisation (bonded)	101	39
5.	BUF/BUFGCntrls	1	1
6.	Frequency	94.969Mhz	167.574Mhz
7.	Overall Delay	25.702ns	12.171ns

5. Conclusion

Thus the architecture with L=8 block size consumes less area, delay and higher frequency than with that of other block size. The signals can be easily filtered using MATLAB for further seizure detection and analysis. It can be further improvised and can be implemented for IIR filters using other multiplication techniques.

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