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Voltage Differencing Buffered Amplifier Based on Floating-Gate MOSFET and its Filter Applications

Aakansha Suchitta [1,2], Richa Srivastava[1,3], Himani Kanwar[1], Devesh Singh[3]*

[1]Netaji Subhas Institute of Technology,
New Delhi 110078, India
[2]Indian Institute of Technology Delhi,
New Delhi 110016, India,
[3]A.K.G. Engineering College,
Ghaziabad – 201009, India
iitd.akanksha@gmail.com, richa_ec@yahoo.co.in, himani.himani2@gmail.com, dsinghece@gmail.com

Abstract:
In this work, floating-gate MOSFET (FGMOS) based low-voltage, low-power (LV/LP) variant of voltage differencing buffered amplifier (VDBA). The linearity of the Operational Transconductance Amplifier (OTA) stage of the proposed active element is observed to increase compared to the conventional CMOS VDBA. This has been demonstrated for several supply voltages. The proposed circuit operates at low supply voltage of ±1.35V with total power consumption of 0.745mW. The application of the proposed circuit is verified through robust resistorless voltage mode universal biquad filters which are observed to implement standard filter functions. The simulations are performed through SPICE in TSMC 0.18µm technology. The work is intended to find applications in low-voltage, low-power battery-operated medical devices and other analog signal processing circuits**.**

Keywords: FGMOS, Voltage Differencing Buffered Amplifier (VDBA), Operational Transconductance Amplifier (OTA), Universal Filter, Analog Signal Processing**.**

1. Introduction

Voltage mode (VM) analog signal processing techniques offer several advantages: convenience in measuring nodal voltages, easily achievable high voltage gain, infinite input impedance of MOS transistors and low voltage circuit design [4]. Among several VM active elements, VDBA (Voltage Differencing Buffered Amplifier) has attractive properties of current mode technology such as reduced power consumption, larger bandwidth, wider linearity and higher slew rate compared to OP-AMP [6]. Furthermore, lower output impedance of VDBA compared to OTA eliminates loading effect which is suitable for VM circuit synthesis. These evidences demand analog signal processing circuits with VDBA as a building block. Several modifications of VDBA and their practical applications in various signal generation circuits have been suggested by Sotner et al. [7].

LV/LP electronics are highly desired in modern portable consumer electronics and battery-operated wearable and implantable biomedical devices. FGMOS techniques have advantages of flexibility, controllability and tunability. In addition, narrower bandwidth and relatively lower transconductance value in comparison to the conventional MOS transistor are attractive features for biomedical devices since biological signals have extremely low amplitude and frequency. Applications of FGMOS in voltage buffer, analog inverter, WTA, neural networks, electronic programming, squarers, current mirrors, multipliers, digital-to-analog and analog-to-digital converters, etc. have been reported [16]. Several research publications have dealt with CMOS implementations of VDBA [5-7]. Few VM active elements have been designed using the floating gate technique, such as Op Amp [18], OTA [19-22] and class AB output stage for CMOS Op-Amps [23]. As per authors' knowledge, suitable literature related to FGMOS based VDBA circuits was not found.

This paper introduces a new floating gate MOS based VDBA suitable for applications in voltage mode analog signal processing circuits. Implementation of second order active filters is possible with the utilization of the proposed VDBA.

Two VM biquad filters containing the newly proposed active element have been simulated. The proposed circuits are simulated using PSPICE. The previously reported CMOS based VDBA has been compared with the proposed FGMOS based VDBA. The use of proposed VDBA is confirmed with its applications to first and second form biquad filters and their capability in generating all standard filter functions.

2. Proposed FGMOS Realization of VDBA: Circuit Description

Conception of the conventional VDBA has been formulated in [5, 6, 17]. The behavioral model is given in Fig. 1. Using standard notation, the relationship between port currents and voltages of CMOS VDBA can be described by the following matrix equation (1):

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_W \end{bmatrix} \quad (1)$$

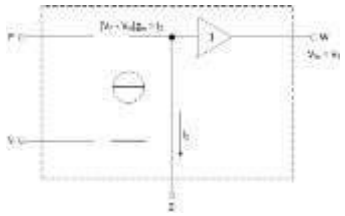


Figure 1: Behavioral model of VDBA

Here, g_m is the transconductance of VDBA, α is the corresponding voltage ratio (α = 1-εv), with εv being the voltage tracking error. The schematic implementation and circuit symbol of the proposed circuit are shown in Figs. 2 and 3 respectively. It consists of two fundamental building blocks: OTA (M_1-M_9) and voltage buffer (M_{10}-M_{16}), both are realized by FGMOS based differential pairs. FGMOS differential pair has been employed in OTA implementation which ensures low voltage operation because of low threshold voltage of FGMOS. In the differential pair formed by two floating gate transistors M1 and M2, one control input of each transistor is used for signal processing purpose, the other control input is used for biasing, and hence an adjustable threshold voltage is achieved. The differential input voltage $V_{in} = V_{FG1} - V_{FG2}$, produces an output current that is voltage controlled current source (VCCS) [6]. V_{FG1} is the floating gate voltage at M1 given by $V_{FG1} = \frac{C_1}{C_T}V_N + \frac{C_2}{C_T}V_{bias}$ and the floating gate voltage at M2 is given by $V_{FG1} = \frac{C_1}{C_T}V_P + \frac{C_2}{C_T}V_{bias}$, where C_T is the total floating gate capacitance, i.e., $C_T = C_1+C_2+C_{GS}+C_{GD}$. The current mirror load for the OTA is formed by MOSFETs M5 and M6. A voltage buffer is used in the output stage of the proposed implementation. It consists of a differential amplifier (M10 - M13) and a feedback transistor M14. The first control input of floating gate MOSFET M10 is V_Z terminal voltage. The input range of the OTA increases by the use of FGMOS transistors. The assumption here is that MOS and FGMOS transistors are of identical parameters and all transistors operate in saturation region.

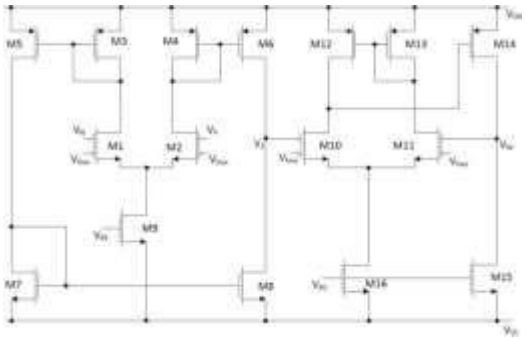


Figure 2: FGMOS implementation of the VDBA

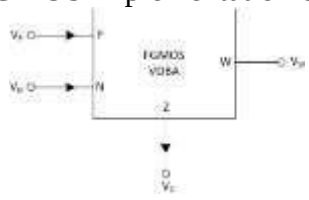


Figure 3: Circuit symbol of FGMOS VDBA

Calculation of input range of the proposed OTA:

Condition for M2 to be in saturation is given by

$$V_{D2} \geq V_{FG2} - V_{T2} \quad (2)$$

$$\text{and } V_{D2} = V_{G4} \quad (3)$$

$$V_{GS4} = V_{ov4} + V_{T4} \quad (4)$$

Equation (9) can be expressed as

$$V_{G4} - V_{S4} = V_{ov4} + V_{T4} \quad (5)$$

Substituting $V_{S4}=V_{DD}$ in Equation (10) gives

$$V_{G4} = V_{ov4} + V_{T4} + V_{DD} \quad (6)$$

Using (2), (3) and (6) gives

$$V_{ov4} + V_{T4} + V_{DD} \geq V_{FG2} - V_{T2} \quad (7)$$

From Fig. 3 the floating gate voltage of M2 is given as

$$V_{FG2} = \frac{C_1}{C_T}V_P + \frac{C_2}{C_T}V_{bias} \quad (8)$$

where C_1 and C_2 are the capacitances of FGMOS transistor and $C_T=C_1+C_2+C_{GS}+C_{GD}$, is the total capacitance.

Substituting V_{FG2} from (8) in (7) gives

$$V_{ov4} + V_{T4} + V_{DD} \geq \frac{C_1}{C_T}V_P + \frac{C_2}{C_T}V_{bias} - V_{T2} \quad (9)$$

$$V_P \leq \frac{C_T}{C_1}V_{ov4} + \frac{C_T}{C_1}V_{T4} + \frac{C_T}{C_1}V_{DD} - \frac{C_2}{C_1}V_{bias} + \frac{C_T}{C_1}V_{T2} \quad (10)$$

If $C_1=C_2$, then Equation (9) can be reduced to

$$V_P \leq 2V_{DD} + 2V_{ov6} + 2V_{T6} - V_{bias} + 2V_{T4} \quad (11)$$

The maximum input range of conventional VDBA is given as

$$V_P \leq V_{DD} + V_{ov4} + V_{T4} + V_{T2} \quad (12)$$

On comparing (11) and (12), it is seen that maximum input range for proposed circuit is higher as compared to the conventional. The same has been proved through simulations in Section IV. Circuits proposed in the work are based on the simulation model of a 2 – input FGMOS transistor depicted in Fig. 4 where transconductance, $g_{mF} = \left(\frac{C_{F1}}{C_T} g_m + \frac{C_{F2}}{C_T} g_m\right)$, with g_m being the gate transconductance of an identical MOS transistor having identical physical parameters as that of the FGMOS transistor. C_T is the total floating gate capacitance seen by the floating gate. It is assumed that the bulk transconductance of the FGMOS transistor is negligibly small.

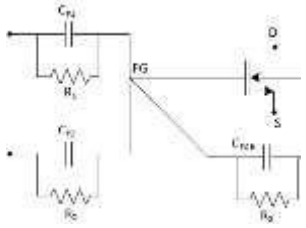
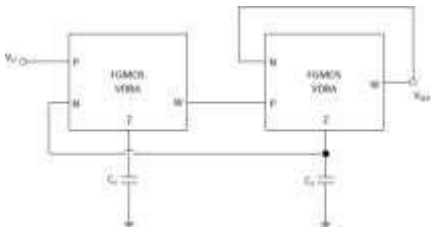


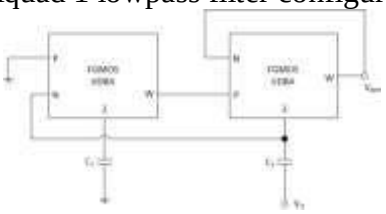
Figure 4: Simulation model of FGMOS

3. Filter Applications

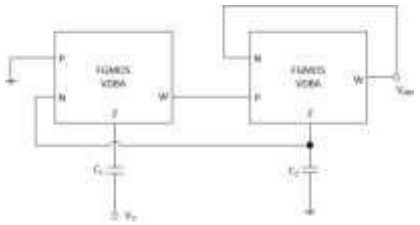
The proposed FGMOS based VDBA is found to be practical for biquad filter applications as will be discussed in this Section. The filters proposed consist of two cascaded FGMOS VDBA active elements together with two capacitors as passive components. Robust biquad filter configurations employing CMOS based VDBA have been proposed in [6]. The proposed biquad 1 and biquad 2 configurations showing several filter functions are shown in Figs. 5-6. These circuits are obtained on similar lines with the objective of low voltage operation.



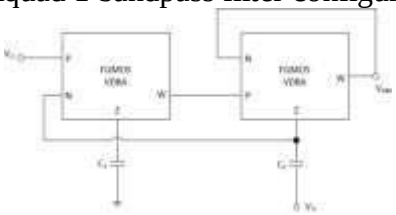
(a) Biquad 1 lowpass filter configuration



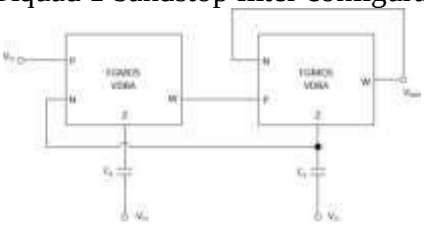
(b) Biquad 1 highpass filter configuration



(c) Biquad 1 bandpass filter configuration



(d) Biquad 1 bandstop filter configuration



(e) Biquad 1 allpass filter configuration

Figure 5 (a-e): Proposed biquad 1 configurations showing several filter functions

The nodal analysis of the proposed filters yield voltage transfer functions expressed by equations (13-17) and equations (18-22) respectively. The relations for natural frequency, quality factor and bandwidth of FGMOS based Biquad 1 and Biquad 2 circuits are given by equations (23) and (24) respectively.

$$\frac{V_{OLF}}{V_{in}} = \frac{\frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}}{s^2 + s\frac{g_{mF2}C_1\alpha_2}{C_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1}{C_1C_2}} \quad (13)$$

$$\frac{V_{OHF}}{V_{in}} = \frac{s^2\alpha_2}{s^2 + s\frac{g_{mF2}C_1\alpha_2}{C_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1}{C_1C_2}} \quad (14)$$

$$\frac{V_{OBF}}{V_{in}} = \frac{s\frac{g_{mF2}\alpha_1\alpha_2}{C_2}}{s^2 + s\frac{g_{mF2}C_1\alpha_2}{C_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1}{C_1C_2}} \quad (15)$$

$$\frac{V_{OBR}}{V_{in}} = \frac{s^2\alpha_2 + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}}{s^2 + s\frac{g_{mF2}C_1\alpha_2}{C_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1}{C_1C_2}} \quad (16)$$

$$\frac{V_{OAF}}{V_{in}} = \frac{s^2\alpha_2 - s\frac{g_{mF2}\alpha_1\alpha_2}{C_2} + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}}{s^2 + s\frac{g_{mF2}C_1\alpha_2}{C_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1}{C_1C_2}} \quad (17)$$

$$\frac{V_{OLP}}{V_{in}} = \frac{\frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}}{s^2 + s\frac{1}{R_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}} \quad (18)$$

$$\frac{V_{OHP}}{V_{in}} = \frac{s^2\alpha_2}{s^2 + s\frac{1}{R_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}} \quad (19)$$

$$\frac{V_{OBP}}{V_{in}} = \frac{-s\frac{g_{mF2}\alpha_2}{C_1C_2}}{s^2 + s\frac{1}{R_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}} \quad (20)$$

$$\frac{V_{OBR}}{V_{in}} = \frac{s^2\alpha_2 + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}}{s^2 + s\frac{1}{R_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}} \quad (21)$$

$$\frac{V_{OAP}}{V_{in}} = \frac{s^2\alpha_2 - s\frac{g_{mF2}\alpha_2}{C_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}}{s^2 + s\frac{1}{R_1C_2} + \frac{g_{mF1}g_{mF2}\alpha_1\alpha_2}{C_1C_2}} \quad (22)$$

$$f_0(\text{Biquad 1}) = \frac{1}{2\pi}\sqrt{\frac{g_{mF1}g_{mF2}\alpha_1}{C_1C_2}} \quad (23a)$$

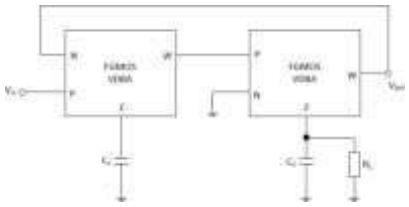
$$Q(\text{Biquad 1}) = \frac{1}{\alpha_2}\sqrt{\frac{g_{mF1}C_2\alpha_2}{g_{mF2}C_1}} \quad (23b)$$

$$B = \frac{\omega_0}{Q} = \sqrt{\alpha_1 \alpha_2}\frac{g_{mF2}}{C_2} \quad (23c)$$

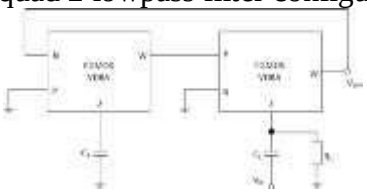
$$f_0(\text{Biquad 2}) = \frac{1}{2\pi}\sqrt{\frac{g_{mF1} g_{mF2} \alpha_1 \alpha_2}{C_1 C_2}} \quad (24a)$$

$$Q(\text{Biquad 2}) = R_1\sqrt{\frac{g_{mF1} g_{mF2} C_2 \alpha_1 \alpha_2}{C_1}} \quad (24b)$$

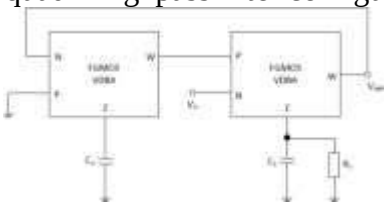
$$B = \frac{\omega_0}{Q} = \frac{1}{R_1 C_2} \quad (24c)$$



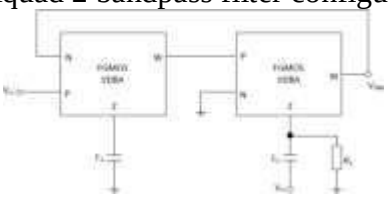
(a) Biquad 2 lowpass filter configuration



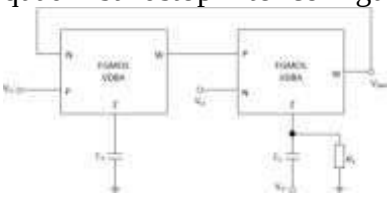
(b) Biquad 2 highpass filter configuration



(c) Biquad 2 bandpass filter configuration



(d) Biquad 2 bandstop filter configuration



(e) Biquad 2 allpass filter configuration

Figure 6 (a-e): Proposed biquad 2 configurations showing several filter functions

4. Simulation Results

The simulations for the proposed active element, FGMOS based VDBA and its biquad filter application circuits are performed with TMSC CMOS 0.18 µm technology. Supply voltage used was ±1.35V. DC convergence error is avoided by the use of model used suggested by [1] because of the floating gate of FGMOS transistor. Large value resistors are connected in parallel with input capacitances in the model. FGMOS capacitances are $C_{F1} = C_{F2} = 200$ fF. Aspect ratio values of MOS and FGMOS transistors are shown in Table 1. Comparison with previous topologies with the proposed circuit is done in Table 2.

Table 1: Aspect ratios of the transistors of proposed VDBA

Transistors	W(µm)	L(µm)
M_1, M_2, M_3, M_4, M_{10}, M_{11}, M_{15}, M_{16}	7	0.35
M_5, M_6	21	0.7
M_7, M_8	7	0.7
M_9	3.5	0.7
M_{12}, M_{13}, M_{14}	14	0.35

Table 2: Comparative Analysis of Conventional and Proposed VDBA

Comparison Parameters	*DO-VDBA [7]*	*FB-VDBA [7]*	*Conventional VDBA [6]*	*Proposed VDBA*
Technology (µm)	0.18	0.18	0.35	0.18
Supply Voltage (V)	± 1.2	± 1.2	± 1.5	± 1.35
No. of transistors	8 MOS	16 MOS	16 MOS	12 MOS + 4 FGMOS
Input range of OTA section (mV)	± 200	± 200	±200	±400
Power consumption	Not reported	Not reported	0.97 mW	0.745 mW
Output impedance at V_w (kΩ)	0.053	130	Not reported	1.132
Transconductance (g_m) (µS)	865 at I_B = 100 µA	1740 at I_B = 100 µA	748 at V_{B1} = 0.44V, V_{B2} = 0.9V	512 at V_{B1} = 0.41V, V_{B2} = 0.643V
Port z impedance (kΩ)	170	130	Not reported	101.9
Bandwidth of OTA stage (MHz)	217 at I_B = 100 µA	70 at I_B = 100 µA	Not reported	385 at V_b = -0.41V
Gain of	0.962	0.962	Not	0.97

buffer stage (V_w/V_z)			reported	

DC transfer characteristic of the output stage of the proposed VDBA at bias voltages V_{B1} = 1V and V_{B2} = 0.45V is shown in Fig. 7. It is seen that the linearity range extends from -1V to +1.5V. The I_Z versus V_P and V_N plot is shown in Fig. 8. The linearity extends in the range ±0.4V and a non-linear behavior is observed elsewhere. The operation of the OTA stage of the proposed VDBA, depicting I_Z against V_P for several values of power supply voltages can be seen in Fig. 9. It can be seen from the plot that though the swing for which the OTA justifies its operation decreases by reducing the power supply voltage; approximately ±350 µA at supply voltage of ±1.45V, ±300 µA at supply voltage of ±1.35V, ±250 µA at supply voltage of ±1.25V and ±200 µA at supply voltage of ±1.15V, the current swing provided for conventional CMOS based VDBA reported in [6], is around ±140 µA, and that too for a supply voltage of ±1.5V which is high compared to the ones simulated for the proposed FGMOS based VDBA. As a comparative analysis, it may be stated that whereas, the linearity observed is in the range ±0.4V for the proposed FGMOS based VDBA performed at different supply voltages (Fig. 9), the linearity extends only upto a threshold of ±0.2V for the conventional CMOS based VDBA [6]. This increase in the range of operation of the proposed VDBA can be accounted for the fact that the equivalent capacitance ratio (C_i/C_T) scales down the effective input signal at the floating gate, resulting in a wider range. However, it may also be mentioned that degradation in frequency response upto 3.50 GHz in the voltage buffer stage of the proposed VDBA is observed due to the additional capacitances in FGMOS. This is depicted in Fig. 10. The frequency response depicting the transconductance of OTA stage, voltage buffer and complete proposed VDBA is shown in the following Figs. 11-13. One out of the two inputs of FGMOS transistors in the OTA stage is grounded. The transconductance of OTA stage of the proposed VDBA at bias voltage of 0.41V is 512µA/V. The bandwidth of input stage of the OTA is found to be 385 MHz at V_b = -0.41V. The simulation results of the biquad 1 filter implemented using FGMOS based VDBA depicting standard filter functions is shown in Fig. 14. Passive component values chosen for simulation are C_1 = C_2 = 100pF and transconductances g_{mF1} = g_{mF2} = 512µA/V. VM biquad filters in Fig. 6(a-e) were designed for f_0 = 0.815 MHz and Q-factor of 1. Various responses of the proposed universal filter (Fig. 6(a-e)) of biquad 2 are shown in Fig. 15. For simulations, equal passive capacitance values C_1 = C_2 = 100pF and R_1 = 5kΩ are chosen for natural frequency of 0.815 MHz and Q-factor of 1.024. It is clear that both ideal and simulated results are in close agreement with each other. The simulation results emphasize high linearity and high performance of the proposed FGMOS based VDBA circuit in terms of reduced power consumption.

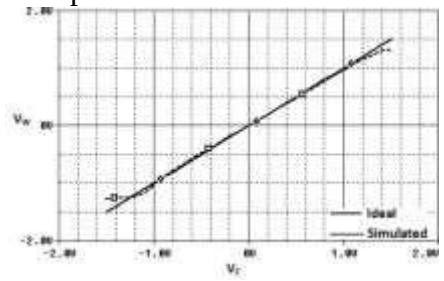


Figure 7: DC transfer characteristic V_W versus V_Z

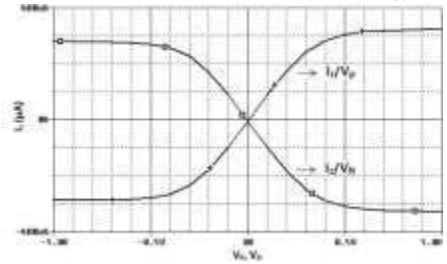


Figure 8: DC transfer characteristic I_Z versus V_P and V_N

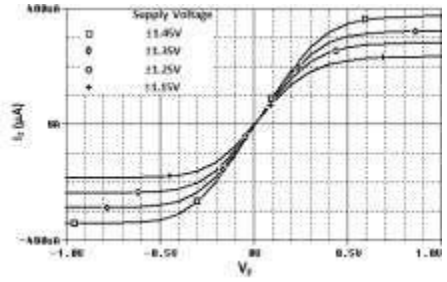


Figure 9: I_z versus V_P at different supply voltages

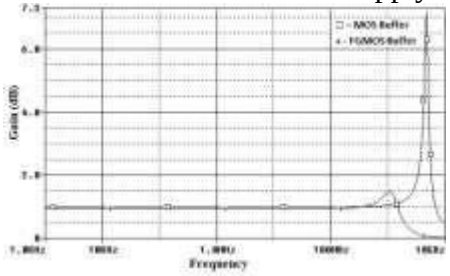


Figure 10: Comparative analysis of frequency response of MOS and FGMOS buffer stages

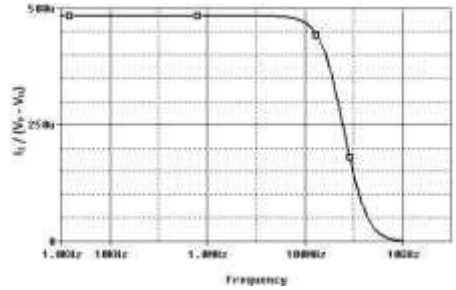


Figure 11: Frequency response of OTA stage

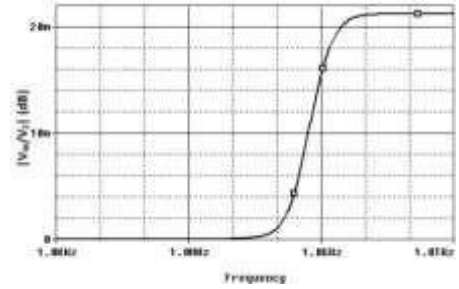


Figure 12: Frequency response of voltage buffer

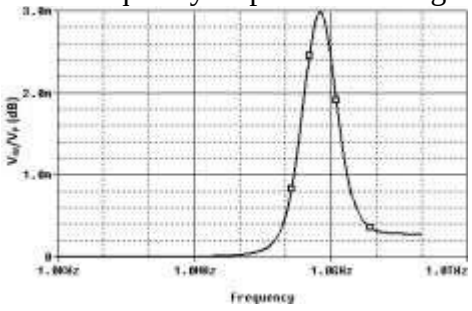


Figure 13: Frequency response of complete proposed VDBA

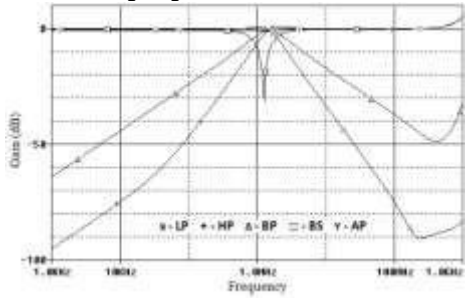


Figure 14: Various responses of proposed universal filter (Biquad 1)

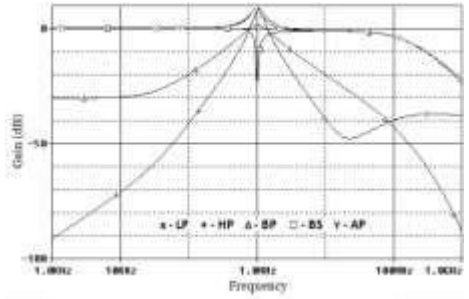


Figure 15: Various responses of proposed universal filter (Biquad 2)

5. Conclusions

The work describes a new FGMOS realization of voltage differencing buffered amplifier. The proposed implementation is observed to operate at low voltage and power consumption is highly reduced. Resistorless voltage mode biquad filters are also realized as practical applications of the proposed FGMOS based VDBA and are seen to implement all standard filter functions. The proposed FGMOS based VDBA and the biquad filters implementing standard filter operations are suitable to find applications in low voltage and low power analog signal processing as well as in consumer electronics.

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