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A ZVS Interleaved Power factor correction based Boost, Half Bridge And Full bridge AC/DC Converter Used in Plug-in Electric Vehicles

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***Abstract*—This paper presents a novel, yet simple zero-voltage switching (ZVS) interleaved boost power factor correction (PFC) ac/dc converter used to charge the traction battery of an electric vehicle from the utility mains. The proposed opology consists of a passive auxiliary circuit, placed between two phases of the interleaved front-end boost PFC converter, which provides enough current to charge and discharge the MOSFETs' output capacitors during turn-ON times. Therefore, the MOSFETs are turned ON at zero voltage. The proposed converter maintains ZVS for the universal input voltage (85 to 265 V_{rms}), which includes a very wide range of duty ratios (0.07–1). In addition, the control system optimizes the amount of reactive current required to guarantee ZVS during the line cycle for different load conditions. This optimization is crucial in this application since the converter may work at very light loads for a long period of time. Experimental results from a 3 kW ac/dc converter are presented in the paper to evaluate the performance of the proposed converter. The results show a considerable increase in efficiency and superior performance of the proposed converter compared to the conventional hard-switched interleaved boost PFC converter**

***Index Terms*—AC/DC converter, continuous current mode (CCM), dc/dc converter, interleaved boost converter, power factor correction (PFC), zero-current switching (ZCS), zero-voltage switching (ZVS).**

NOMENCLATURE

Δi_{LA}	Inductor current ripple of boost A (A).
ω_l	Line frequency (rad/s).
ψ	Phase-shift between leading leg and lagging leg pulses.
C_{So}	Output capacitance of the boost MOSFET (F).
D	PFC duty ratio.
F_s	Switching frequency (Hz).
i_{in}	Input current of power factor correction (PFC) (A).
i_{LA}	Inductor current of boost A (A).
i_{LB}	Inductor current of boost B (A).
i_{SA1}	Switch S_{A1} current (A).
I_{BAT}	Battery current (A).
I_o	DC output current (A).
I_P	Peak current of the boost inductor (A).
I_{ref}	Peak value of the auxiliary circuit reference current
I_V	Valley current of the boost inductor (A).
k_1	Controller coefficient.
p_{in}	Instantaneous input power (W).
p_{ref}	Instantaneous input power reference value (W).
$P_{in,pk}$	Peak input power (W).
P_{ref}	Power reference value (W).
R_o	Load incremental resistance (Ω).
P_{sw}	Switching losses
R_e	Converter effective load resistance (Ω).
R_L	PFC inductor series resistance (Ω).
t	Time (s).
t_d	Dead time (s).
u	Control input.
v_{AUX}	Voltage across auxiliary circuit (V).
v_{in}	Instantaneous input voltage of PFC (V).
V_{BAT}	Battery voltage (V).
V_d	Output diode forward voltage drop (V).
V_o	DC output voltage (V).
x	State variables.
ESR	Equivalent series resistance (Ω).
SiC	Silicon carbide.

I. INTRODUCTION

electric vehicle (EV) power conditioning systems usually utilize a high-energy battery pack to store energy for the electric traction system [1]. A typical block diagram of the power conditioning system in an EV is shown in Fig. 1. The high-energy battery pack is typically charged from a utility ac outlet [2]. This energy conversion during the battery charging is performed by an ac/dc converter. Such ac/dc converters, which
are used to charge the high-energy battery, usually consist of two stages: front-end boost converter, which performs input PFC and ac/dc conversion, and full-bridge dc/dc converter for
battery charging and galvanic isolation [3]. PFC is essential to
improve the quality of the input current, which is drawn from
the utility so as to comply with the regulatory standards like IEC

Fig. 1. Block diagram of EV power conditioning system.

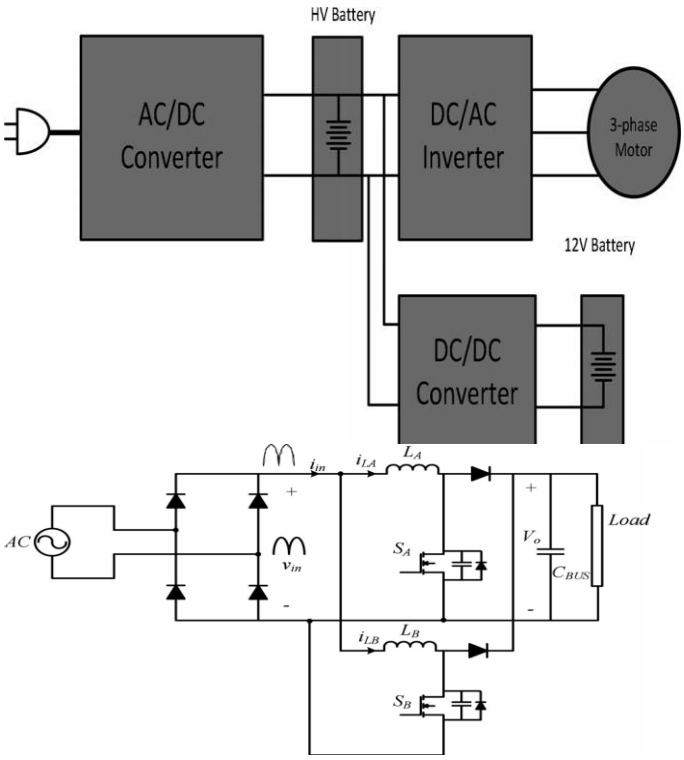


Fig. 2. Interleaved boost PFC schematic.

Boost converters are generally used to realize input PFC and ac/dc conversion [4]–[9] in the front end of an ac/dc converter. In high power applications, interleaving continuous current mode (CCM) PFC boost stages, as shown in Fig. 2, is a very common approach to effectively decrease the inductor footprint and volume as well as the output capacitor current ripple [7]–[14]. A typical boost PFC utilizes a switch and a diode. In the range of a few kilowatt, power MOSFETs are usually used to realize the boost converter. The main sources of switching losses in boost PFC converters are hard turn-ON of the MOSFET and the reverse recovery of the boost diode during its turn-OFF. In order to eliminate the switching losses in a MOSFET-based boost PFC converter, different auxiliary circuits have been proposed [15]–[25]. The typical placement of a zero-voltage switching (ZVS) auxiliary circuit is shown in Fig. 3. Commonly, these auxiliary circuits consist of a combination of passive components such as small inductors and capacitors and additional active components such as MOSFETs and diodes. Auxiliary circuits in ZVS-puslewidth modulation (PWM) single-switch converters are generally one of two types, nonresonant [15] and resonant [16]–[23], depending on whether there is an *LC* resonant network placed in series with the switch. Typical nonresonant and resonant ZVS auxiliary circuits are shown in Fig. 4(a) and (b)–(d), respectively. There is a third type, dual auxiliary circuits [23], that is a combination of both resonant and nonresonant circuits. These circuits, which were first categorized in [23], are shown in Fig. 4(e).

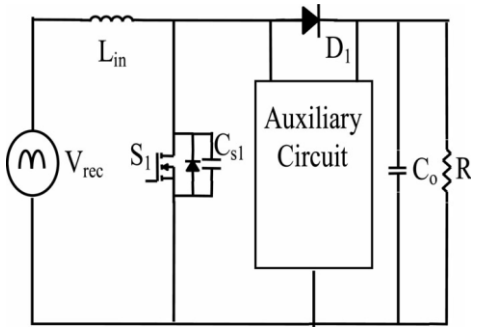


Fig. 3. Placement of ZVS auxiliary circuit in boost PFC converter.

For each converter in Fig. 4, the auxiliary switch is turned ON just before the main converter switch is to be turned ON.

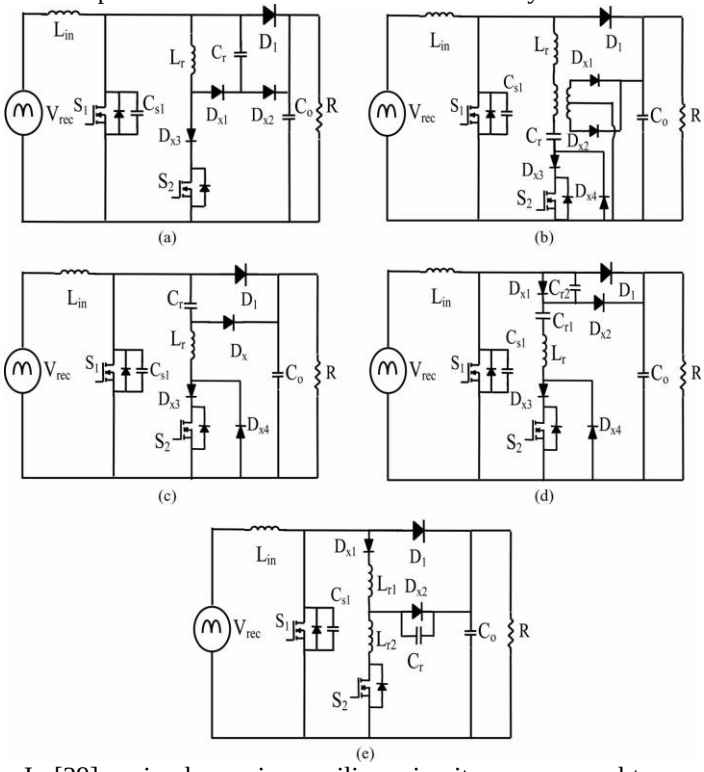
The auxiliary switch is used to discharge the capacitor across the main switch so that it can turn ON with ZVS. Some capacitance, either internal to the device and/or external, is needed to slow down the rise in voltage across the main switch so that it can turn OFF with ZVS. The auxiliary switch is turned OFF shortly after the main switch is turned ON, and all the energy in the auxiliary circuit is eventually transferred to the output.After this is done, the auxiliary circuit is fully deactivated and the converter operates like a conventional PWM converter. The components in the auxiliary circuit have lower ratings than those in the main power circuit because the circuit is active for a fraction of the switching cycle. This allows a device that can turn ON with fewer switching losses than the main switch to be used as the auxiliary switch.

The addition of an active auxiliary circuit to a PWM converter can also eliminate the reverse-recovery current of the main power boost diode if a Si device is used. It can be seen from Fig. 4 that all the auxiliary circuits have an inductor located in series with the auxiliary switch. This allows current to be gradually transferred away from the boost diode to the auxiliary switch when it is turned ON so that the charge in the diode is slowly removed during turn-OFF; with such a gradual transition from conduction state to OFF-state of the diode, its reverse-recovery current can be greatly reduced, thus, eliminating reverse recovery losses..

The key limitations of the previously proposed auxiliary circuits for single-switch boost PFC converters are the use of extra semiconductor devices such as diodes and MOSFETs [15]–[23] as well as passive components and the extra losses associated with the auxiliary circuit. In resonant-type auxiliary circuits, the main switch can suffer from addition current stress [20], while in nonresonant-type auxiliary circuits [15], the auxiliary switch may undergo hard switching; these key problems in ZVS auxiliary circuit tend to somewhat offset the gain in efficiency achieved by soft switching of the main boost switches. In addition, the gating pulse of the auxiliary switch needs to be precisely synchronized to that of the main switch, which adds to the complexity of the boost PFC control system.

Auxiliary circuits with active semiconductor devices have also been used to achieve ZVS in interleaved boost PFC converters [24]–[26]. The key issue related to such auxiliary

circuits isthat basically two auxiliary circuits are implemented to achieve ZVS in both phases. This leads to use ofmultiple semiconductor switching devices to implement the auxiliary circuits [24]–[26], which increases the cost and complexity of the overall converter. ZVS in interleaved boost converter can be easily achieved if the current in the boost inductors is always in critical conduction mode [27], but the main problem related to such critical conduction mode boost converters is the limitation of the maximum power handling capacity of the overall converter, typically such converters are applicable for operation around 1 kW and their inherent line current distortion. Magnetically coupled boost inductors in interleaved boost PFC converter can help achieving ZVS of the main switches [28], but design and mass replication of such coupled boost inductor cannot be done easily.



In [29], a simple passive auxiliary circuit was proposed to achieve ZVS in interleaved boost converter for dc–dc voltage conversion applications. The main drawback of this circuit is that the duty ratio of the boost switches has to remain strictly above 0.5, which cannot be guaranteed in PFC ac/dc applications
especially for universal ac inputs that vary from 85 to 265 V_{rms} . through this auxiliary circuit should be adjusted for the maximum load, so as to guarantee ZVS for all conditions. This causes excessive circulating current for light-load conditions and decreases the efficiency of the converter at light loads. In battery
charger applications, since the converter has to operate at light
loads for a long period of time, this constant circulating current
significantly deteriorates the performance of the converter. In this context, it should also be noted that in EV power conditioning systems, high efficiency of the power stages is imperative.

The front-end ac/dc boost PFC converter plays a key
role in transferring power from external utility mains to the EV battery packs, and the boost diodes in this converter are key source of losses. Presently, SiC diodes are gaining popularity
in ac/dc boost converters [30] since they have near-zero reverse
recovery losses but normally SiC diodes have greater forward
voltage drops, typically 2.4V and more as compared to 1.2V in
Si diodes for a 600V device, which is required in this application. For instance, a 600-V 10-A SiC diode C3D10060A, from CREE, Inc., Durham, NC, has a forward voltage drop of 2.4V compared to a 600-V 10-A fast recovery diode 10ETF06PBF, voltage drop. In addition, the thermal coefficient of SiC diodes on the forward voltage drop is positive, implying that the voltage drop increases with temperature, while the one for Si diode is
In this paper, a novel interleaved boost PFC converter is proposed to achieve soft switching in the main switches of the
converter. The proposed converter implements soft switching
through a simple passive auxiliary circuit placed in between the
two phases of the interleaved boost converter. This auxiliary circuit is able to provide reactive current to charge and discharge the output capacitors of the boost MOSFETs and guarantee ZVS. Since there are no extra semiconductors used in the auxiliary circuit, high efficiency and reliability are the main advantages of the proposed system. In addition, the proposed converter is able to optimize the amount of reactive current required to implement soft switching based on the load condition and the input voltage. Thus, the conduction losses caused by the auxiliary circuit are minimized based on the operating condition.
This paper is organized as follows. In Section II, the steadystate
analysis of the proposed interleaved boost PFC converter is explained.

II. Steady-State Analysis of the ZVS Interleaved Boost PFC Converter

Fig. 5 shows the power circuit of the ZVS interleaved boost PFC converter. In this converter, two boost converters operate
with 180◦ phase shift in order to reduce the input current ripple
of the converter. This 180◦ phase shift can be used to provide
reactive current for realizing ZVS for power MOSFETs. This
auxiliary circuit consists of a HF inductor and a dc-blocking capacitor. Since there may be a slight difference between the duty ratios of the two phases, this dc-blocking capacitor is necessary to eliminate any dc current arising from the mismatch of the duty ratios of the main switches in the practical circuit.
Fig. 6 shows the key waveforms of the converter for $D >$ 0.5. According to this figure, there are eight operating modes in one switching cycle of the converter. The operating modes are explained as follows.
Mode I ($t_0 < t < t_1$*):* This mode starts when the gate pulse is applied to S_{A1} . Once the voltage is applied to the gate, S_{A1} is turned ON under zero voltage. Since S_{A1} and S_{B1} are ON during this interval, the voltage across the auxiliary inductor is zero. Thus, the current through the auxiliary circuit remains

constant at $I_{Aux,p}$. During this interval, the switch S_{A1} current,
i_{SA1} , is given by:

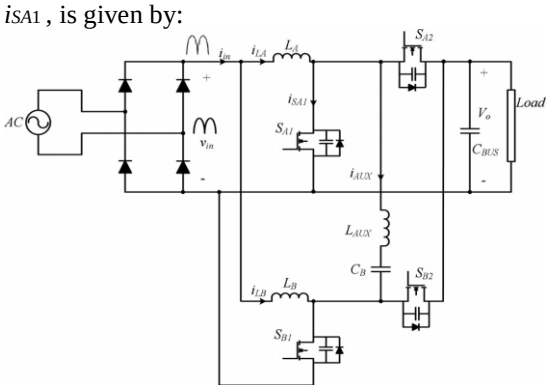
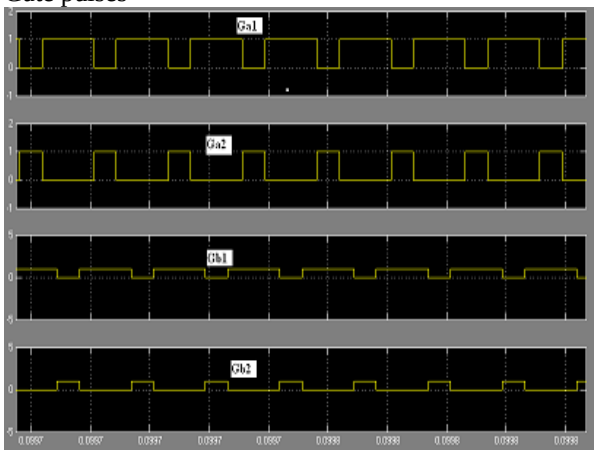


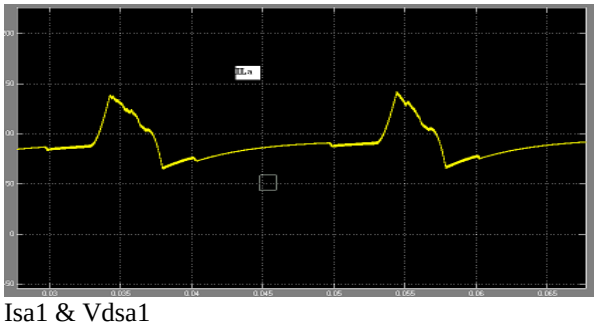
Fig. 5. Proposed ZVS interleaved boost PFC schematic.

$$i_{SA1}(t) = I_V - I_{Aux,p} - v_{in}/L_A(t - t_0) \text{ ----------(1)}$$

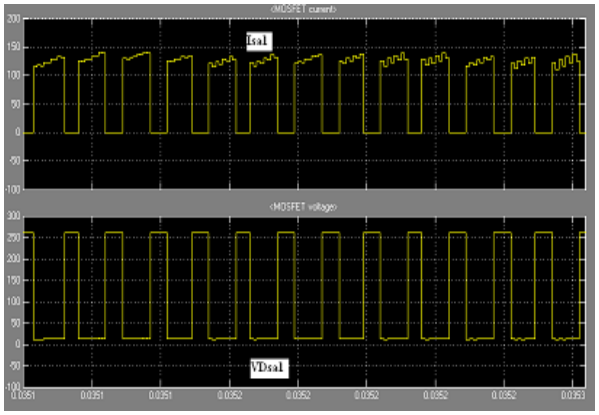
Gate pulses



inductor current ILa



Isa1 & Vdsa1



Vaux and Iaux

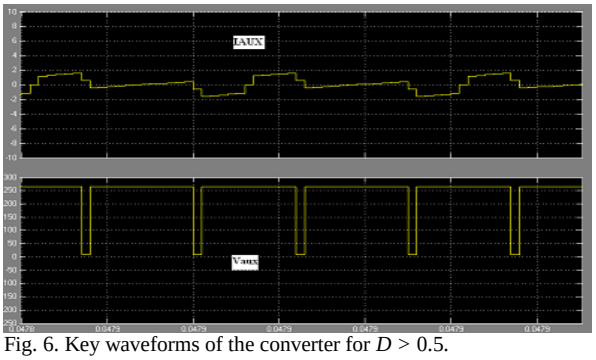


Fig. 6. Key waveforms of the converter for $D > 0.5$.

Since the two phases have 180◦ phase shift, the value of t_1 is given by:

$t_1 - t_0 = (D - 0.5)\, T_s$.---------- (2)

Therefore, the duty ratio is given by

$D = (t_1 - t_0)\, f_s + 1/2$.---------- (3)

Inserting (2) into (1), the value of the switch current is calculated
at t_1

$I_1 = I_V - I_{Aux,p}(t) - v_{in}/2L_A f_s - v_{2in}/L_A f_s V_o$ --------(4)

This mode ends once the gate voltage has been removed from
S_{B1} .

Mode II ($t_1 < t < t_2$): This mode is the dead time between the
phase B MOSFETs. During this interval, the auxiliary circuit current charges the output capacitance of S_{B1} and discharges
the output capacitance of S_{B2} . In this mode, the average voltage
across the boost inductance L_B is zero. Therefore, the current through L_B remains constant at its peak value. The voltage across the auxiliary inductor is given by:

$v_{AUX}(t) = -(V_o/(t_2 - t_1))(t - t_1)$. ----------(5)

Thus, the current through auxiliary circuit is given by:

$i_{AUX}(t) = I_{Aux,p} - V_o/(2(t_2 - t_1)L_{AUX})(t - t_1)^2$----- (6)

$t_2 - t_1 = t_d$ is the dead time between S_{B1} and S_{B2}. During
this period, the output capacitors of the MOSFETs should fully
charge and discharge in order to guarantee ZVS for S_{B1} and S_{B2} . Thus, the dead time is calculated as follows:

$$I_P + I_{Aux,p} - \frac{V_o}{2L_{AUX}} t_d = 2C_{So}\frac{V_o}{t_d} \qquad (7)$$

$$t_d = \frac{(I_P + I_{Aux,p})L_{AUX}}{V_o} + \sqrt{\frac{(I_P + I_{Aux,p})^2 L_{AUX}^2}{V_o^2} - 4C_{So}L_{AUX}} \qquad (8)$$

.

the current through switch S_{A1} is calculated as follows

\

$$i_{SA1}(t) = I_V - I_{Aux,p} - \frac{v_{in}}{L_A}(t - t_0) + \frac{V_o}{2t_d L_{AUX}}(t - t_1)^2 . \qquad (9)$$

This mode ends when the output capacitors completely charged and discharged. The switch current i_{SA1} at this point is
given by:

$$I_2 = I_V - I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{L_A}(t_d + t_1 - t_0) + \frac{V_o}{2L_{\mathrm{AUX}}}t_d. \quad (10)$$

Mode III ($t_2 < t < t_3$): Once the output capacitors of S_{B1} and S_{B2} have been charged and discharged completely, the gate signal of S_{B2} is applied and S_{B2} is turned ON under ZVS.During this interval, the voltage across the auxiliary circuit is $-V_o$. The current through the auxiliary inductor, inductor L_A and switch S_{A1}, is given by

$$i_{\mathrm{AUX}} = I_{\mathrm{Aux},p} - \frac{V_o}{2L_{\mathrm{AUX}}}t_d - \frac{V_o}{L_{\mathrm{AUX}}}(t - t_2) \quad (11)$$

$$i_{LA}(t) = I_V + \frac{v_{\mathrm{in}}}{L_A}(t - t_0). \quad (12)$$

$$i_{SA1}(t) = I_V - I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{L_A}(t - t_0) + \frac{V_o}{2L_{\mathrm{AUX}}}t_d + \frac{V_o}{L_{\mathrm{AUX}}}(t - t_2). \quad (13)$$

This mode ends once the gate signal of S_{B2} has become zero ($t_3 = t_0 + 0.5\,T_s - t_d$). The value of i_{SA1} at this point is given by:

$$I_3(t) = I_V - I_{\mathrm{Aux},p} + \frac{v_{\mathrm{in}}}{2f_sL_A} - \frac{v_{\mathrm{in}}t_d}{L_A} + \frac{V_o}{2L_{\mathrm{AUX}}}t_d + \frac{V_o}{f_sL_{\mathrm{AUX}}}(1 - D) - \frac{2V_o}{L_{\mathrm{AUX}}}t_d. \quad (14)$$

Mode IV ($t_3 < t < t_4$): During this mode, the output capacitor of S_{B2} is charging from zero to V_o and the output capacitor of S_{B1} is discharging from V_o to zero. This period is actually the dead time between S_{B2} and S_{B1} ($t_4 - t_3 = t_d$). The auxiliary inductor current, the boost inductor current, and the switch current, during this mode, is given by:

$$i_{\mathrm{AUX}}(t) = I_{\mathrm{Aux},p} + \frac{3V_o}{2L_{\mathrm{AUX}}}t_d - \frac{V_o}{f_sL_{\mathrm{AUX}}}(1 - D) - \frac{V_o}{2t_dL_{\mathrm{AUX}}}(t - t_3)^2 \quad (15)$$

$$i_{LA}(t) = I_V + \frac{v_{\mathrm{in}}}{L_A}(t - t_0) \quad (16)$$

$$i_{SA1}(t) = I_V - I_{\mathrm{Aux},p} - \frac{v_{in}}{L_A}(t - t_0) + \frac{V_o}{2L_{\mathrm{AUX}}}t_d + \frac{V_o}{L_{\mathrm{AUX}}}(t - t_2). \quad (17)$$

This mode ends once the gate signal is applied to S_{B1}. The value of i_{SA1} at this instant is given by:

$$I_4(t) = I_V - I_{\mathrm{Aux},p} + \frac{v_{\mathrm{in}}}{2f_sL_A} + \frac{V_o}{L_{\mathrm{AUX}}}t_d + \frac{V_o}{f_sL_{\mathrm{AUX}}}(1 - D). \quad (18)$$

Mode V ($t_4 < t < t_5$): This mode starts when the gate signal is applied to S_{B1} .Once the gate has been applied, S_{B1} is turnedON under ZVS. Since S_{A1} and S_{B1} are ON during this period, the voltage across the auxiliary inductor is zero; hence, the auxiliary inductor current remains constant at its peak value, $I_{\mathrm{Aux},p}$. The boost inductor current and the switch current, during this mode, are given by:

$$i_{LA}(t) = I_V + \frac{v_{\mathrm{in}}}{L_A}(t - t_0) \quad (19)$$

$$i_{SA1}(t) = I_V + I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{L_A}(t - t_0). \quad (20)$$

Mode VI ($t_5 < t < t_6$): During this mode, the output capacitor of S_{A1} is charging from zero to V_o and the output capacitor of S_{A2} is discharging from V_o to zero. This period is actually the dead time between S_{A1} and S_{A2} ($t_6 - t_5 = t_d$). In this period, the current through the boost inductor L_A remains constant at its peak value. The auxiliary inductor current i_{AUX} is given by:
This mode ends once the gate signal is removed from S_{A1} . The value of i_{SA1} at this time is given by:

$$i_{SA1}(t) = I_V + I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{f_sL_A}D. \quad (21)$$

Mode VI ($t_5 < t < t_6$): During this mode, the output capacitor of S_{A1} is charging from zero to V_o and the output capacitor of S_{A2} is discharging from V_o to zero. This period is actually the dead time between S_{A1} and S_{A2} ($t_6 - t_5 = t_d$). In this period, the current through the boost inductor L_A remains constant at its peak value. The auxiliary inductor current i_{AUX} is given by:

$$i_{\mathrm{AUX}}(t) = -I_{\mathrm{Aux},p} + \frac{V_o}{2t_dL_{\mathrm{AUX}}}(t - t_5)^2. \quad (22)$$

This mode ends once the output capacitors have completely been charged and discharged.
Mode VII ($t_6 < t < t_7$): During this mode, the voltage across the auxiliary circuit is V_o ; hence, the current through the auxiliarycircuit is given by:

$$i_{\mathrm{AUX}}(t) = -I_{\mathrm{Aux},p} + \frac{V_o}{2L_{\mathrm{AUX}}}t_d + \frac{V_o}{L_{\mathrm{AUX}}}(t - t_6). \quad (23)$$

During this mode, the MOSFET channel S_{A2} is conducting the current to the output. The current through this switch is given by:

$$i_{SA2}(t) = I_{\mathrm{Aux},p} - \frac{V_o}{2L_{\mathrm{AUX}}}t_d + \frac{V_o}{L_{\mathrm{AUX}}}(t - t_6) + I_P - \frac{v_{\mathrm{in}} - V_o}{L_A}(t - t_6). \quad (24)$$

The peak value of this current is given by:

$$I_5(t) = -I_{\mathrm{Aux},p} + \frac{V_o}{2L_{\mathrm{AUX}}}t_d + I_P. \quad (25)$$

This mode ends when i_{SA2} reaches zero. Thus t_7 is given by

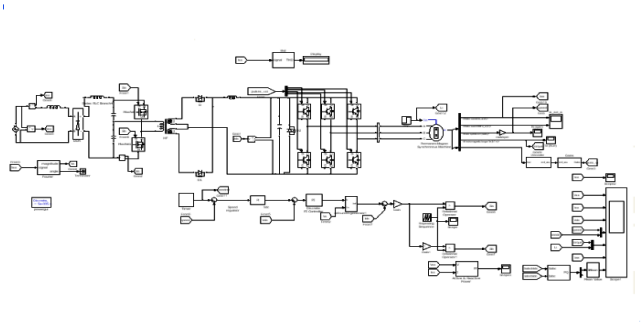
$$t_7 = t_6 + \frac{I_{\mathrm{Aux},p} - (V_o/2L_{\mathrm{AUX}})t_d}{(V_o/L_{\mathrm{AUX}}) + (v_{\mathrm{in}} - V_o/L_A)}. \quad (26)$$

Mode VIII ($t_7 < t < t_8$): During this mode, the output capacitor of S_{A1} is discharging from V_o to zero and the output capacitor of S_{A2} is charging from zero to V_o . In this mode, the current through L_A is at its minimum value I_V and the excess current from the auxiliary circuit charges and discharges the output capacitors. The auxiliary inductor current is given by:.

$$i_{\mathrm{AUX}}(t) = -I_{\mathrm{Aux},p} + \frac{V_o}{2L_{\mathrm{AUX}}} t_d + \frac{V_o}{L_{\mathrm{AUX}}} \frac{I_{\mathrm{Aux},p} - (V_o/2L_{\mathrm{AUX}})t_d}{(V_o/L_{\mathrm{AUX}}) + ((v_{\mathrm{in}} - V_o)/L_A)} + \frac{V_o}{2L_{\mathrm{AUX}}} (t - t_7)^2 . \quad (27)$$

Fig. 7. Key waveforms of the converter for $D < 0.5$.and discharged completely. Fig. 7 shows the key waveforms of the circuit for $D < 0.5$. According to this figure, the modes of operation are the same for the proposed circuit

III SIMULATION OF PFC BUCK HALF-BRIDGE CONVERTER BASED PMBLDCM DRIVE



The proposed PMBLDCM drive is modeled in Mat lab-Simulink , speed of which is controlled effectively by controlling the DC link voltage. The detailed data of the motor and simulation parameters are given in Appendix. The performance of the proposed PFC drive is evaluated on the basis of various parameters such as total harmonic distortion (THDi) of the current at input AC mains, power factor (PF) and efficiency of the drive system (ηdrive) at different speeds of the motor. Moreover, these parameters are (a)evaluated for variable speed at constant supply voltage(220v) and also (b)evaluated for variable input AC voltage at rated speed (1500 rpm) of the PMBLDCM.

A. Performance during Starting

The performance of the proposed PMBLDCM drive fed from 220 V AC mains during starting at rated torque and 600 rpm speed is shown in Fig. 8a. A rate limiter of 560 V/s is introduced in the reference voltage to limit the starting current of the motor as well as the charging current of the DC link capacitor. The PI controller closely tracks the reference speed so that the motor attains reference speed smoothly within 0.3 sec while keeping the stator current within the desired limits i.e. double the rated value. The current (is) waveform at input AC mains is in phase with the supply voltage (vs) demonstrating nearly unity power factor during the starting.

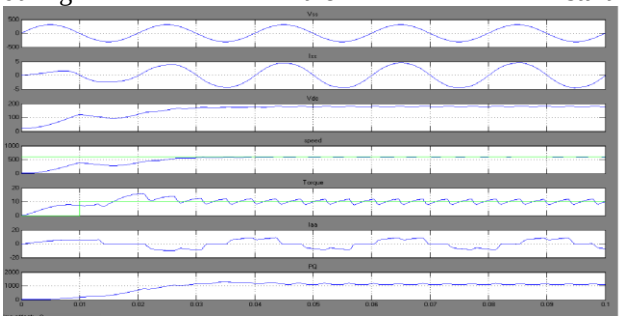


fig 8(a) performance during starting speed of 600rpm

B. Performance under Speed Control

Figs. 8(b)-8(d) show the performance of the proposed PMBLDCM drive under the speed control at constant rated torque (9.55 Nm) and 220 V AC mains supply voltage. These results are categorized as performance during transient and steady state conditions.

1) Transient Condition: Figs. 8b-c shows the performance of the drive during the speed control of the compressor. The reference speed is changed from 600 rpm to 1500 rpm for the rated load performance of the compressor; from 1500 rpm to 900 rpm for performance of the compressor at light load. It is observed that the speed control is fast and smooth in either direction i.e. acceleration or retardation with power factor maintained at nearly unity value. Moreover, the stator current of PMBLDCM is within the allowed limit (twice the rated current) due to the introduction of a rate limiter in the referencevoltage.

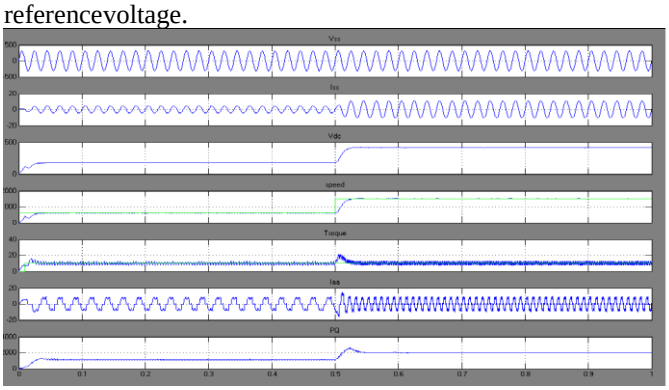


Fig8(b) performance during speed of 600 to 1500 rpm

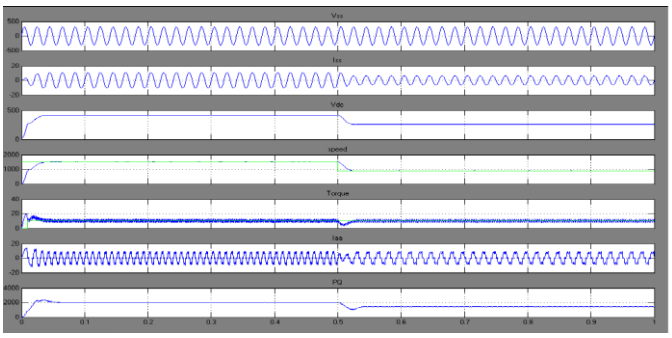


Fig8(c) performance during speed of 1500 to 900rpm

2) Steady State Condition: The speed control of the PMBLDCM driven compressor under steady state condition is shown below Table-II to demonstrate the effectiveness of the proposed drive in wide speed range. Figs of voltage (vs) and current (is) waveforms at AC mains, DC link voltage (Vdc), speed of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the motor for phase 'a' (Ia), and shaft power output (Po) at 1500 rpm speed are below.

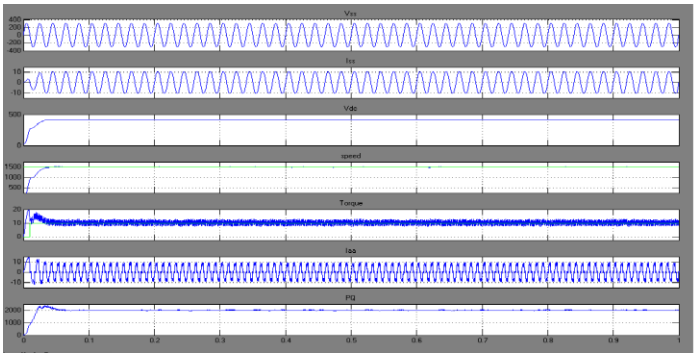


Fig8(d) performance during speed of 1500 rpm

Power Quality Performance: The performance of the proposed PMBLDCM drive in terms of various PQ parameters such as THD_i, and PF is summarized in Table(I)

Performance of drive under speed control at 220 v ac input

Speed (rpm)	Vdc (v)	THDi (%)	PF	Efficiency (%)
300	100	4.84**T**	0.9987	74.2
400	126	4.50	0.9991	79.1
500	153	2.99	0.9993	81.8
600	179	2.90	0.9995	83.8
700	205	2.74	0.9996	85.3
800	232	2.58	0.9996	86.1
900	258	2.29	0.9996	87.0
1000	284	2.24	0.9997	87.6
1100	310	2.20	0.9997	88.1
1200	334	2.18	0.9997	88.1
1300	363	2.14	0.9997	88.2
1400	390	2.11	0.9997	88.1
1500	416	2.09	0.9997	88.1

The following graphs (a) speed vs Vdc(b)Speed vs thd (c)Speed vs pf (d)Speed vs efficiency are shown below

IV. CONCLUSION

In this paper, a new interleaved boost PFC converter,and buck based half bridge based PFC converter is proposed, which provides soft switching for the power MOSFETs, In addition, the control system effectively optimizes the amount of reactive current required to achieve ZVS for the power MOSFETs. The frequency loop, which is introduced in the control system, determines the frequency of the modulator based on the load condition and the duty cycle of the converter.

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