

New topologies for Transformerless Single-Stage AC/DC Converter

K. Srinivas, M.V.Praveen reddy

Vaageswari college of engineering and technology

Abstract—This paper presents a high step-down transformerless single-stage single-switch ac/dc converter suitable for universal line applications (90–270 V_{rms}). The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 130 V) and low output voltage without a high step-down transformer. The absence of transformer reduces the component counts and cost of the converter. Unlike most of the boost-type PFC cell, the main switch of the proposed converter only handles the peak inductor current of dc/dc cell rather than the superposition of both inductor currents. Detailed analysis and design procedures of the proposed circuit are given and verified by experimental results.

Index Terms—Direct power transfer (DPT), integrated buck–buck–boost converter (IBuBuBo), power-factor correction (PFC), single-stage (SS), transformerless.

I. INTRODUCTION

Single stage ac/dc converters have received much attention in the past decades because of its cost effectiveness, compact size, and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation [1]–[7]. Their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V at high-line application [8]. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. For application with low output voltage (e.g., $\leq 48V$), this high intermediate bus voltage increases components stresses on the dc/dc cell. With a simple step-down dc/dc cell (i.e. buck or buck–boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance [9], [10]. Therefore, a high step-down transformer is usually employed even when galvanic isolation is not mandatory. For example, LED drivers without isolation may satisfy safety requirement [11]. Also, in

have been expended to develop active power filters and conditioner that can soften the power quality problems. some multistage power electronics system (e.g., in data center, electrochemical and petrochemical industries, and subway applications [12]), the isolation has been done in the PFC stage, the second transformer in the dc/dc cell for the sake of isolation is considered as redundant. Hence, nonisolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall

system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts [13]. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection [14].

To tackle the aforementioned problems, an effective way is to reduce the bus voltage much below the line input voltage. Several topologies have been reported [9], [10], [13], [15]–[18]. Although the recently reported IBoBuBo converter [13] is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell. On the other hand, the converters [9], [10], [15]–[18] employ different PFC cells to reduce the intermediate bus voltage. Among those converters, [9] and [15] use a transformer to achieve low output voltage either in PFC cell or dc/dc cell. Therefore, the leakage inductance is unavoidable. In [10], [17], and [18], the converters employ a buck–boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [18] and [10] process power at least twice resulting in low power efficiency. Moreover, the reported converters, in [16], and [17], consist of two active switches leading to more complicated gate control. Apart from reducing the intermediate bus voltage, the converter in [19] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e., $< 10\%$. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. More details on comparing different approaches will be

given in the Section V. In this paper, an intergrated buck–buck–boost (IBuBuBo) converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and outputmost common and probably it is widely used method.

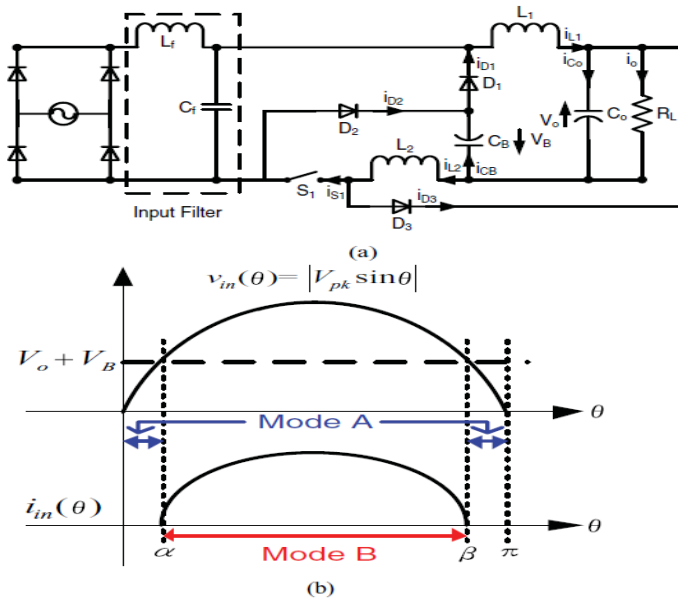


Fig. 1. (a) Proposed IBuBuBo SS ac/dc converter. (b) Input voltage and current

Waveforms

capacitors, further reduction of the bus voltage can be achieved.

Therefore, a transformer is not needed to obtain the low output

voltage. To sum up, the converter is able to achieve:

- 1) low intermediate bus and output voltages in the absence of transformer;
- 2) simple control structure with a single-switch;
- 3) positive output voltage;
- 4) high conversion efficiency due to part of input power is processed once and
- 5) input surge current protection because of series connection of input source and switch.

The paper is organized as follows: operation principle of the proposed IBuBuBo converter is depicted in Section II and followed by design consideration with key equations in Section III. Experimental result and discussion of the converter are given in Section IV and V, respectively. Finally, conclusion is stated in Section VI.

II. PROPOSED CIRCUIT AND ITS OPERATING PRINCIPLE

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L_1 , S_1 , D_1 , C_o , and C_B) and a buck–boost dc/dc cell (L_2 , S_1 , D_2 , D_3 , C_o , and C_B) is illustrated in Fig. 1(a). Although L_2 is on the return path of the buck PFC cell, it will be shown later in Section III-A that it does not contribute to the cell electrically. Thus, L_2 is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0 . Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

Mode A ($v_{in}(\theta) \leq V_B + V_o$): When the input voltage $v_{in}(\theta)$ is smaller than the sum of intermediate bus voltage V_B , and output

voltage V_o , the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage [20], owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period

and no input current is drawn as shown in Fig. 1(b). The circuit

operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 2(a),(b), and (f).

Fig. 3(a) shows its key current waveforms.

1) Stage 1 (period d_1T_s in Fig. 3) [see Fig. 2(a)]: When switch S_1 is turned ON, inductor L_2 is charged linearly by the bus voltage V_B while diode D_2 is conducting. Output capacitor C_o delivers power to the load.

2) Stage 2 (period d_2T_s in Fig. 3) [see Fig. 2(b)]: When switch S_1 is switched OFF, diode D_3 becomes forward biased and energy stored in L_2 is released to C_o and the load.

3) Stage 3 (period $d_3T_s - d_4T_s$ in Fig. 3) [see Fig. 2(f)]: The inductor current i_{L2} is totally discharged and only C_o sustains the load current.

Mode B ($v_{in}(\theta) > V_B + V_o$): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 2(c), (d), (e), and (f). The key waveforms are shown in Fig. 3(b).

1) Stage 1 (period d_1T_s in Fig. 3) [see Fig. 2(c)]: When switch S_1 is turned ON, both inductors L_1 and L_2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage ($v_{in}(\theta) - V_B - V_o$), while diode D_2 is conducting.

2) Stage 2 (period d_2T_s in Fig. 3) [see Fig. 2(d)]: When switch S_1 is switched OFF, inductor current i_{L1} decreases linearly to charge C_B and C_o through diode D_1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L_2 is released to C_o and the current is supplied to the load through diode D_3 . This stage ends once inductor L_2 is fully discharged.

3) Stage 3 (period d_3T_s in Fig. 3) [see Fig. 2(e)]: Inductor L_1 continues to deliver current to C_o and the load until its current reaches zero.

4) Stage 4 (period d_4T_s in Fig. 3) [see Fig. 2(f)]: Only C_o delivers all the output power.

III. DESIGN CONSIDERATIONS

To simplify the circuit analysis, some assumptions are made as follows:

- 1) all components are ideal;
- 2) line input source is pure sinusoidal, i.e. $v_{in}(\theta) = V_{pk} \sin(\theta)$ where V_{pk} and θ are denoted as its peak voltage and phase angle, respectively;
- 4)

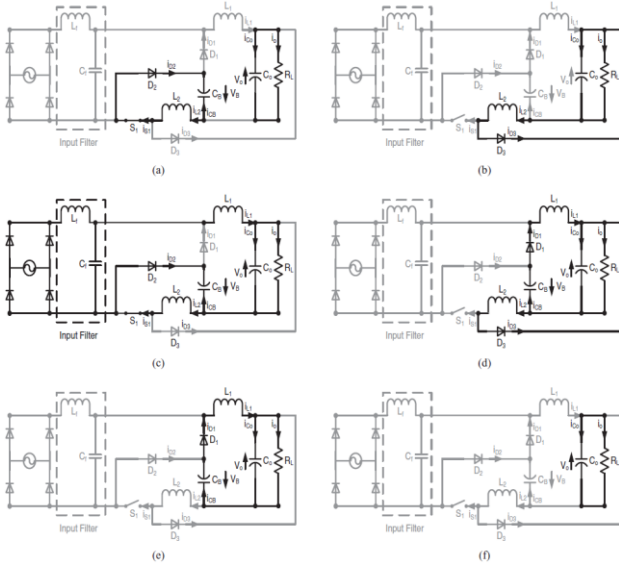


Fig. 2. Circuit operation stages of the proposed ac/dc converter

3) both capacitors C_B and C_o are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;

4) the switching frequency f_s is much higher than the line frequency such that the rectified line input voltage $v_{in}(\theta)$ is constant within a switching period.

A. Circuit Characteristics

According to Fig. 1(b), there is no input current drawn from the source in Mode A, and the phase angles of the dead-time α and β can be expressed as

$$\alpha = \arcsin\left(\frac{V_T}{V_{pk}}\right)$$

$$\beta = \pi - \alpha = \pi - \arcsin\left(\frac{V_T}{V_{pk}}\right).$$

where V_T is the sum of V_B and V_o . Thus, the conduction angle of the converter is

$$\gamma = \beta - \alpha = \pi - 2\arcsin(V_T/V_{pk}) \quad (2)$$

From the key waveforms (see Fig. 3), the peak currents of the

two inductors are

$$i_{L1pk} = \begin{cases} (v_{in}(\theta) - V_T)/L_1 d_1 T_s, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \quad (3)$$

$$\text{And } i_{L2pk} = (V_B/L_2)d_1 T_s \quad (4)$$

where T_s ($1/f_s$) is a switching period of the converter. In (3) and (4), the dependency of i_{L1pk} on θ has been omitted for clarity. It is noted that L_2 does not contribute in (3) even though it is on the current return path of the PFC cell. In addition, by considering volt-second balance of the L_1 and L_2 , respectively, the important duty ratio relationships can be expressed as follows:

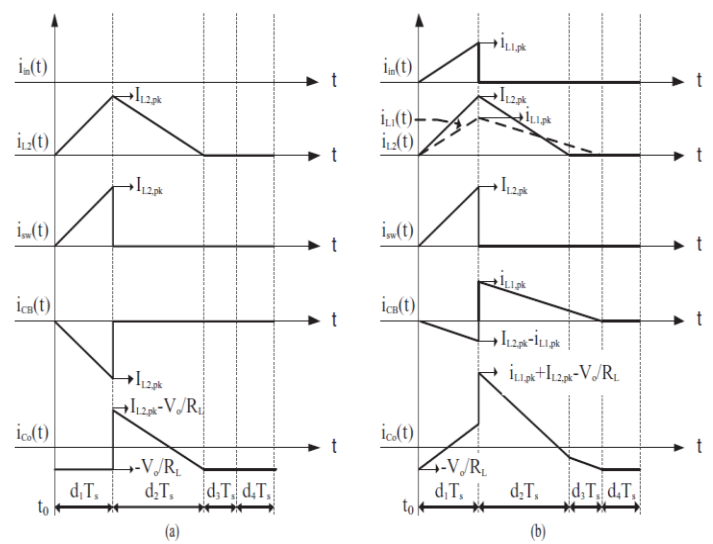
$$d_2 + d_3 = \begin{cases} (v_{in}(\theta) - V_T)/V_T d_1, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \quad (5)$$

$$d_2 = (V_B/V_o)d_1 \quad (6)$$

By applying charge balance of C_B over a half-line period, the

bus voltage V_B can be determined. From Fig. 3, the average current of C_B over a switching and half-line periods are expressed as follows:

Fig.3. Key waveforms of the proposed circuit.



$$\begin{aligned} \langle i_{CB} \rangle_{sw} &= \frac{1}{2}(i_{L1pk}(d_1 + d_2 + d_3) - I_{L2pk}d_1) \\ &= \frac{d_1^2 T_s}{2} \left[\frac{(v_{in}(\theta) - V_T)v_{in}(\theta)}{L_1 V_T} - \frac{V_B}{L_2} \right] \quad (7) \end{aligned}$$

and

$$\begin{aligned} \langle i_{CB} \rangle_{\pi} &= \frac{1}{\pi} \int_0^{\pi} \langle i_{CB} \rangle_{sw} d\theta \\ &= \frac{d_1^2 T_s}{2\pi} \left[\frac{V_{pk}}{L_1} \left(V_{pk} V_T \left(\frac{\gamma}{2} + \frac{A}{4} \right) - B \right) - \frac{\pi V_B}{L_2} \right] \quad (8) \end{aligned}$$

where the constants A and B are

$$A = \sin(2\alpha) - \sin(2\beta) \quad (9)$$

$$B = \cos(\alpha) - \cos(\beta) \quad (10)$$

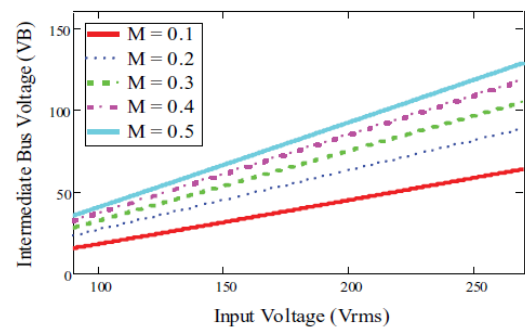


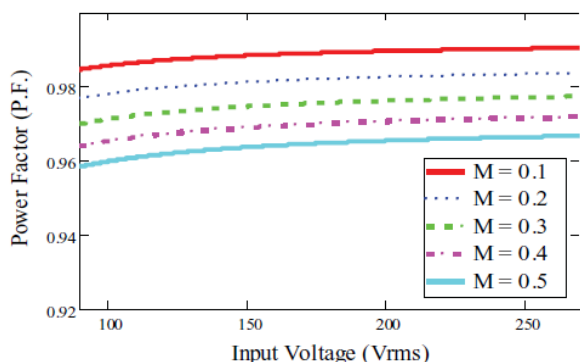
Fig. 4. Calculated intermediate bus voltage under different inductance ratios.

Putting (8) to zero due to the steady-state operation, this leads To

$$V_B = \frac{MV_{pk}^2}{2\pi(V_B + V_o)} \times \left[\pi - 2\arcsin\left(\frac{V_B + V_o}{V_{pk}}\right) - \frac{2(V_B + V_o)\sqrt{(V_{pk} + V_B + V_o)(V_{pk} - V_B - V_o)}}{V_{pk}^2} \right] \quad (11)$$

where M is the inductance ratio L_2/L_1 .

As observed from (11), the bus voltage V_B can be obtained easily by numerical method. It is noted that V_B is independent on the load, but dependent on the inductance ratio M. Fig. 4 depicts the relationship among V_B , rms value of the line voltage, and inductance ratio M. It is noted that the bus voltage is kept below 150 V at high-line input condition.



IV SIMULATION RESULTS TRANSFORMERLESS SINGLE STAGE SINGLE-SWITCH AC/DC CONVERTER

The performance of the proposed circuit is verified by the Matlab simulation. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage ($< 150V$) and high power ($> 96\%$), the inductance ratio has to be optimized according to Figs. 4 and 5. The lower the bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used.

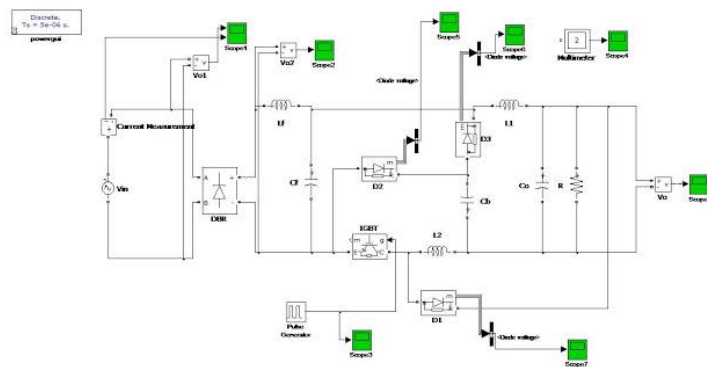


Fig. 7: simulation circuit

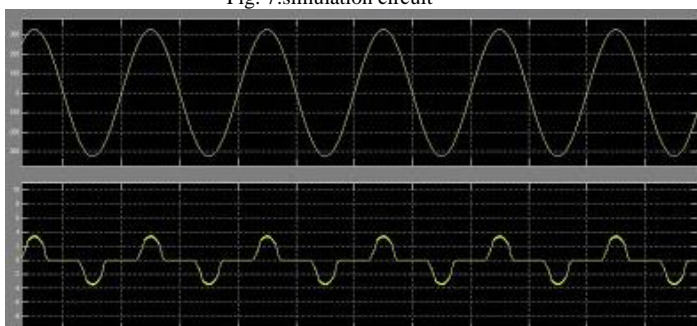


Fig. 8. Measured input characteristic of the converter at (a) 270 Vrms under 100-W condition

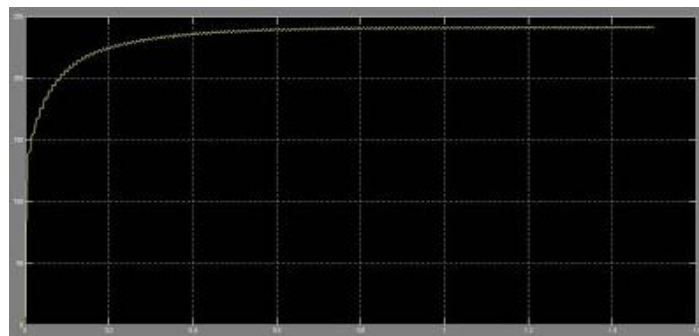


Fig. 9. Measured output voltage bus voltage at 270 Vrms under full load condition

V BUCK-BOOST-TYPE UNITY POWER FACTOR RECTIFIER WITH EXTENDED VOLTAGE CONVERSION RATIO

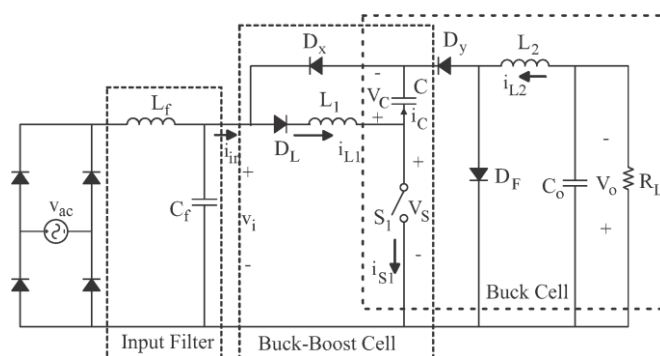


Fig. 10. Proposed single-stage PFC converter

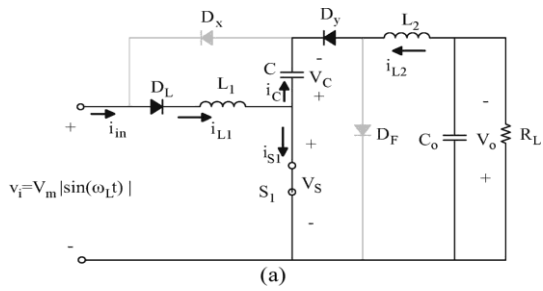
VI. CONVERTER OPERATION PRINCIPLE

The proposed converter shown in Fig. 1 is analyzed with six assumptions in this section.

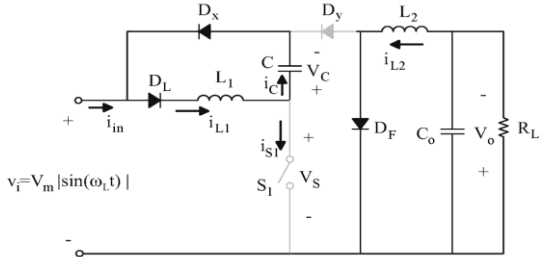
- 1) Input voltage v_{ac} is considered to be an ideal rectified sine wave, i.e., $v_i = V_m / \sin(\omega_L t)$, where V_m is the peak amplitude and ω_L is the line angular frequency.
- 2) All components are ideal; thus, the efficiency is 100%.
- 3) Switching frequency f_s is much higher than ac line frequency f_L , so that the input voltage can be considered constant during one switching period T_s .
- 4) Capacitor C is big enough such that voltage V_C can be considered constant during T_s . Furthermore, output voltage V_o is pure dc without twice the line frequency ripple.
- 5) Both inductors L_1 and L_2 operate in the DCM. Furthermore, the current in inductor L_1 (i_{L1}) reaches zero level prior to the current in L_2 (i_{L2}).
- 6) The phase shift of the input line current introduced by the input filter is minimal and can be neglected.

With these assumptions, the circuit operation over one switching period T_s can be described in three operating stages, as shown in Fig. 11

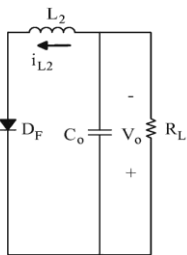
Fig.11. Operating stages of the proposed converter. (a) Stage 1. (b) Stage (c) Stage.



(a)



(b)



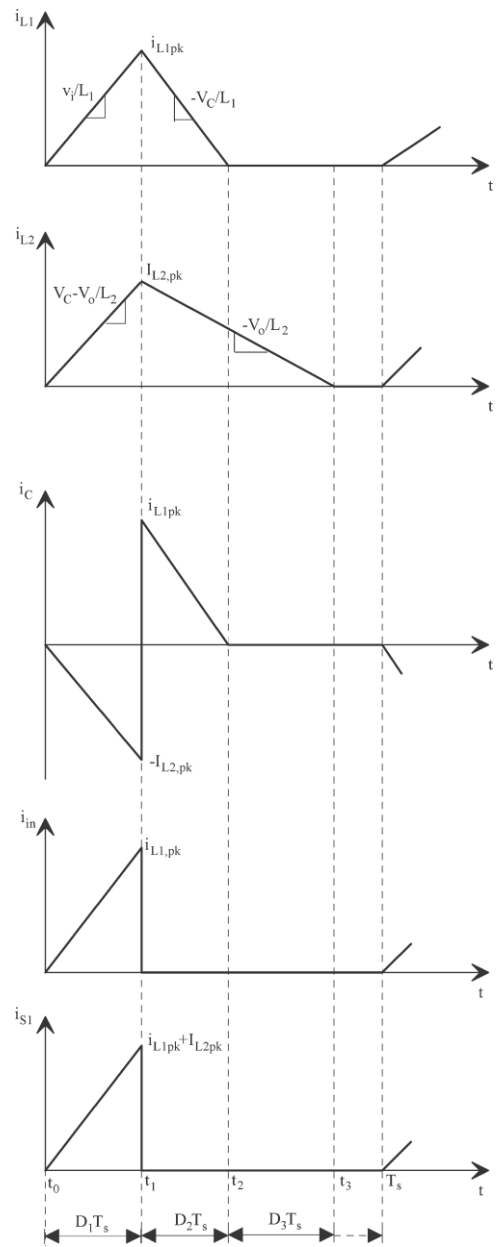
(c)

Stage 1 $[t_0, t_1]$: Prior to this interval, the currents through L_1 and L_2 are at ground level. When switch S_1 is turned on at $t = 0$, diode D_y becomes forward biased, and currents i_{L1} and i_{L2} begin to linearly increase. This interval ends when switch S_1 is turned off, initiating the next stage.

Stage 2 $[t_1, t_2]$: When the switch is turned off, diode D_y becomes reverse biased. Thus, current i_{L1} linearly decreases through diode D_x , whereas current i_{L2} linearly decreases at a rate proportional to output voltage V_o through the freewheeling diode D_F . This stage ends when current i_{L1} reaches the ground level. Diode D_L prevents current i_{L1} from becoming negative. **Stage 3** $[t_2, t_3]$: In this stage, current i_{L2} continues to decrease through the freewheeling diode D_F until it becomes zero. The converter stays in this stage until the switch is turned on again. To improve the overall efficiency, it is preferred to turn on the switch at $t = t_3$, which will reduce the current stresses through the semiconductor devices.

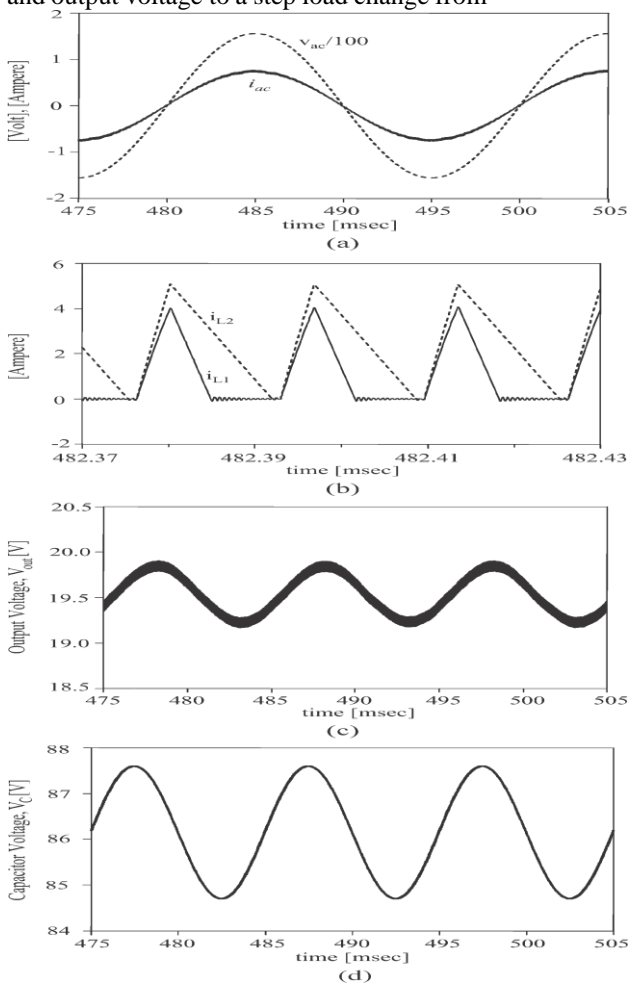
The characteristic ideal circuit waveforms during one switching period are shown in

Fig. 12.



V. SIMULATION AND EXPERIMENTAL RESULTS

Input inductor L_1 is designed for the DCM operation, whereas L_2 is designed for the BCM operation. The circuit components are calculated based on the analysis performed in previous sections, and they are given as $L_1 = 100 \mu\text{H}$, $L_2 = L_{2,\text{crit}} = 47 \mu\text{H}$, $C = 680 \mu\text{F}$, and $C_O = 100 \mu\text{F}$. Duty cycle D_1 is set to 0.22. A high-frequency input filter ($L_F = 2 \text{ mH}$, and $C_F = 0.68 \mu\text{F}$) is inserted after the bridge rectifier to filter the ripples in the rectified line current. The simulated waveforms are shown in Fig. 13, which correctly demonstrates the DCM/BCM operating mode. The simulation result gives a total harmonic distortion in the input line current of about 1%. Moreover, it is clear from Fig. 13(c) that output voltage V_O has a significant low-frequency ripple, which is unacceptable for some specific applications. However, as discussed in Section IV-C, the low-frequency ripple in V_O can be greatly reduced by simply regulating the output voltage. Therefore, a simple feedback controller has been implemented to regulate V_O at 20 V. The simulated transient response of the input line current and output voltage to a step load change from



IV. CONCLUSION

The proposed single-stage ac/dc converters has been simulated, and the results have shown good agreements with the predicted values. The intermediate bus voltage of the circuit is able to keep below 150V at all input and output

conditions, and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. Moreover, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance, and the cost of the proposed circuit are reduced compared with the isolated counterparts.

REFERENCES

- [1] Zhao, F. C. Lee, and F.-s. Tsai, "Voltage and current stress reduction in single-stage power-factor correction AC/DC converters with bulk capacitor voltage feedback," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 477–484, Jul. 2002.
- [2] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A survey," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749–755, May 2003.
- [3] S. Luo, W. Qiu, W. Wu, and I. Batarseh, "Flyboost power factor correction cell and a new family of single-stage AC/DC converters," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 25–34, Jan. 2005.
- [4] D. D. C. Lu, H. H. C. Iu, and V. Pjevalica, "A Single-Stage AC/DC converter With high power factor, regulated bus voltage, and output voltage," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 218–228, Jan. 2008.
- [5] M. K. H. Cheung, M. H. L. Chow, and C. K. Tse, "Practical design and evaluation of a 1 kW PFC power supply based on reduced redundant power processing principle," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 665–673, Feb. 2008.
- [6] D. D. C. Lu, H. H. C. Iu, and V. Pjevalica, "Single-Stage AC/DC Boost: Forward converter with high power factor and regulated bus and output voltages," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2128–2132, Jun. 2009.
- [7] H.-Y. Li and H.-C. Chen, "Dynamic modeling and controller design for a single-stage single-switch parallel boost-flyback-flyback converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 816–827, Feb. 2012.
- [8] R. Redl and L. Balogh, "Design considerations for single-stage isolated power-factor-corrected power supplies with fast regulation of the output voltage," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1995, vol. 1, pp. 454–458.
- [9] L. Antonio, B. Andrs, S. Marina, S. Vicente, and O. Emilio, "New power factor correction AC-DC converter with reduced storage capacitor voltage," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 384–397, Feb. 2007.
- [10] E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Buck-boost-type unity power factor rectifier with extended voltage conversion ratio," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1123–1132, Mar. 2008.
- [11] M. Ryu, J. Baek, J. Kim, S. Park, and H. Kim, "Electrolytic capacitor-less, nonisolated PFC converter for high-voltage LEDs driving," in *Proc. IEEE Int. Conf. Power Electron. and ECCE Asia*, 2011, pp. 499–506.
- [12] A. A. Badin and I. Barbi, "Unity power factor isolated three-phase rectifier with two single-phase buck rectifiers based on the scott transformer," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2688–2696, Sep. 2011.
- [13] S. K. Ki and D. D. C. Lu, "Implementation of an efficient transformerless single-stage single-switch ac/dc converter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4095–4105, Dec. 2010.

- [14] A. Abramovitz and K. M. Smedley, "Analysis and design of a tapped inductor buck-boost PFC rectifier with low bus voltage," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2637–2649, Sep. 2011.
- [15] J. M. Alonso, M. A. Dalla Costa, and C. Ordiz, "Integrated buck-flyback converter as a high-power-factor off-line power supply," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1090–1100, Mar. 2008.
- [16] K. Nishimura, K. Hirachi, S. Komiyama, and M. Nakaoka, "Two buck choppers built-in single phase one stage PFC converter with reduced DC voltage ripple and its specific control scheme," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2008, pp. 1378–1383.
- [17] T. J. Liang, L. S. Yang, and J. F. Chen, "Analysis and design of a singlephase ac/dc step-down converter for universal input voltage," *IET Electr. Power Appl.*, vol. 1, no. 5, pp. 778–784, Sep. 2007.
- [18] M. A. Al-Saffar, E. H. Ismail, and A. J. Sabzali, "Integrated buck-boost-quadratic buck PFC rectifier for universal input applications," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2886–2896, Dec. 2009.
- [19] X. Qu, S.-C. Wong, and C. K. Tse, "Resonance-assisted buck converter for offline driving of power LED replacement lamps," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 532–540, Feb. 2011.
- [20] Y. Jang and M. M. Jovanovic, "Bridgeless high-power-factor buck converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011.
- [21] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "An alternative to supply DC voltages with high power factor," *IEEE Trans. Ind. Electron.*