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Simulation of a Zero-Voltage-Switching and Zero-Current-Switching Interleaved Boost And Buck Converter

MD.Imran, K. Chandra mouli
Vaageswari College of engineering and technology

***Abstract*—**A novel interleaved boost and buck converter with zero-voltage switching (ZVS) and zero-current switching (ZCS) characteristic is proposed in this paper. By using the interleaved approach, this topology not only decreases the current stress of the main circuit device but also reduces the ripple of the input current and output voltage. Moreover, by establishing the common soft-switching module, the soft-switching interleaved converter can greatly reduce the size and cost. The main switches can achieve the characteristics of ZVS and ZCS simultaneously to reduce the switching loss and improve the efficiency with a wide range of load. This topology has two operational conditions depending on the situation of the duty cycle. The operational principle, theoretical analysis, and design method of the proposed converter are presented. Finally, simulations results are used to verify the feasibility and exactness of the proposed converter.

***Index Terms*—**Interleaved boost converter, zero-current switching (ZCS), zero-voltage switching (ZVS).

INTRODUCTION

A Interleaved boost converter usually combines more than two conventional topologies, and the current in the element of the interleaved boost converter is half of the conventional topology in the same power condition. Besides, the input current ripple and output voltage ripple of the interleaved boost converter are lower than those of the conventional topologies. The single boost converter can use the zero-voltage switching (ZVS) and/or zero-current switching (ZCS) to reduce the switching loss of the high-frequency switching [1]–[4], [13]–[16], [18]. However, they are considered for the single topology. Many soft-switching techniques are then introduced to the interleaved boost converters. The interleaved boost converters with ZCS or ZVS are proposed in [5]–[8], [17]. These topologies have higher efficiency than the conventional boost converter because the proposed circuits have decreased the switching losses of the main switches with ZCS or ZVS. Nevertheless, these circuits can just achieve the junction of ZVS or ZCS singly or need more auxiliary circuits to reach the soft switching. In [9],

soft-switching circuit for the interleaved boost converter is proposed. However, its main switches are zero-current turn-ON and zero-voltage turn-OFF and the converter works in the discontinuous mode. The maximum duty cycle of the converter is also limited. In [10], it does not reduce the switching losses of the interleaved boost converter by the soft-switching techniques, but itdecreases the voltage stresses of the switches by the doublevoltage technique with the help of the double-voltage capacitor. This topology has a characteristic that the operational analysis is not equivalent in$D$ >50% and$D$ <50%. A soft-switching bridgeless power factor correction circuit is shown in [11]. and costs less. And this circuit reduces the switching losses and improves the efficiency by ZVS technique, but it does not improve the turn-OFF switching losses by a ZCS technique. This paper proposes a novel interleaved boost converter with both characteristics of zero-voltage turn-ON and zero-current turn-OFF for the main switches to improve the efficiency with a wide range of load. The voltage stresses of the main switches and auxiliary switch are equal to the output voltage and the duty cycle of the proposed topology can be increased to more than 50%. The proposed converter is the parallel of two boost converters and their driving signals stagger 180◦ and this makes the operation assumed symmetrical. Moreover, by establishing the common soft-switching module, the soft-switching interleaved converter can further reduce the size and cost.

ANALYSIS OF OPERATION

Fig. 1 shows the proposed circuit. It uses the interleaved boost topology and applies the common soft-switching circuit. The resonant circuit consists of the resonant inductor L_r , resonant capacitor C_r , parasitic capacitors C_{sa} and C_{sb}, and auxiliary switch S_r to become a resonant way to reach ZVS and ZCS mfunctions. Fig. 2 shows the two operating modes of this circuit,depending on whether the duty cycle of the main switch *A. Operational Analysis ofD <50% Mode*

The operating principle of the proposed topology is described

in this section. There are 24 operational modes in the complete

cycle. Only the 12 modes related to the main switch S_a are analyzed, because the interleaved topology is symmetrical. Fig. 3 shows the related waveforms when the duty cycle of the main

Fig. 1 A novel interleaved boost converter with characteristics of zero-voltage switching and zero-current switching.

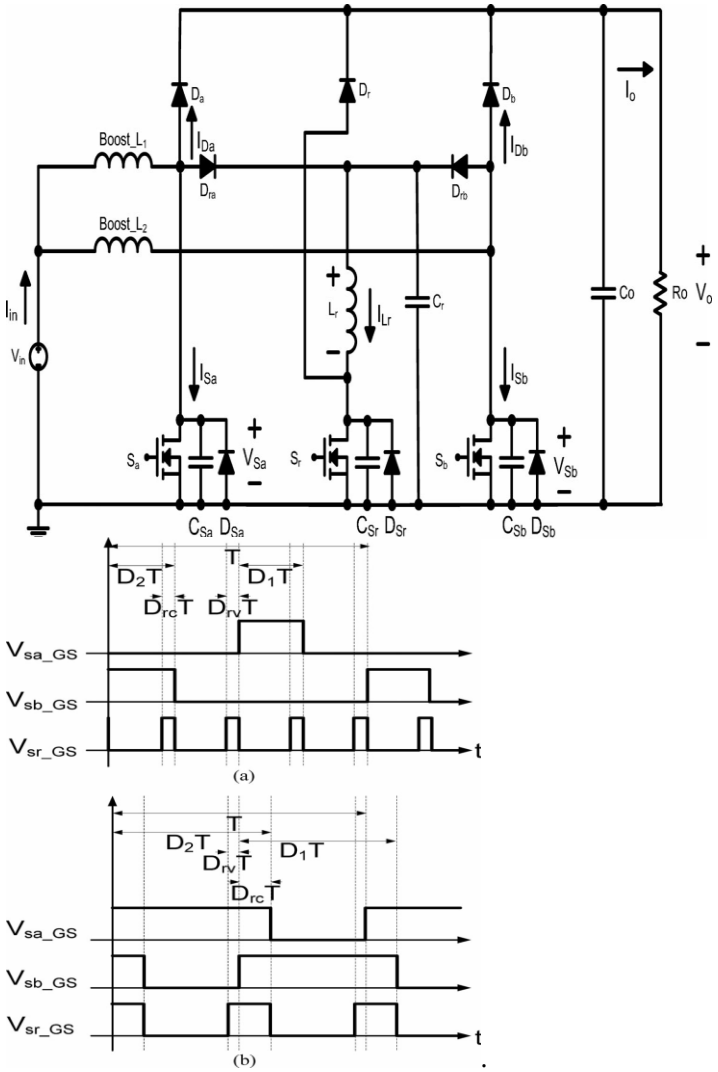


Fig. 2 Switching waveforms of the main switches *Sa* and *Sb* and auxiliary switch *Sr* . (a)*D* < 50% mode. (b)*D* > 50% mode.

switch is less than 50%. There are some assumptions to simplify
the circuit analysis.

1) All power switches and diodes are ideal.
2) The input inductor and output capacitor are ideal.
3) The two inductors are equal; Boost_L1 = Boost_L2 .
4) The duty cycles of the main switches are equal; $D_1 = D_2$.

Mode 1 [t_0 –t_1]: Fig. 4(a) shows the equivalent circuit. In this mode, the main switches *Sa* and *Sb* are turned OFF, the auxiliary
switch *Sr* and the rectifier diodes *Da* and *Db* are turned ON,and the clamped diode *Dr* is turned OFF. The voltages across the parasitic capacitors *Csa* and *Csb* of the main switches and the resonant capacitor *Cr* are all equal to the output voltage;i.e., *Vsa* = *Vsb* = *Vsr* = *Vo* in the previous mode. The resonant inductor current *ILr* linearly ramps up until it reaches *Iin* at *t* = t_1 . When the resonant inductor current *ILr* is equal to *Iin*, the mode 1 will end. Then, the rectifier diodes are turned OFF. The interval time t_{01} is $t_{01} = L_r I_{in}/V_o$---------- (1)

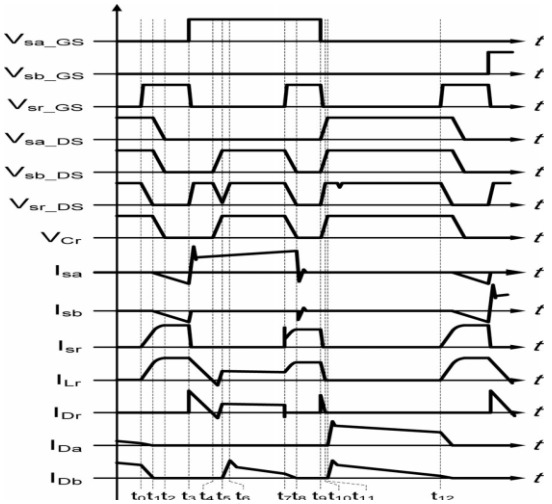


Fig. 3 Related waveforms (*D* < 50%).

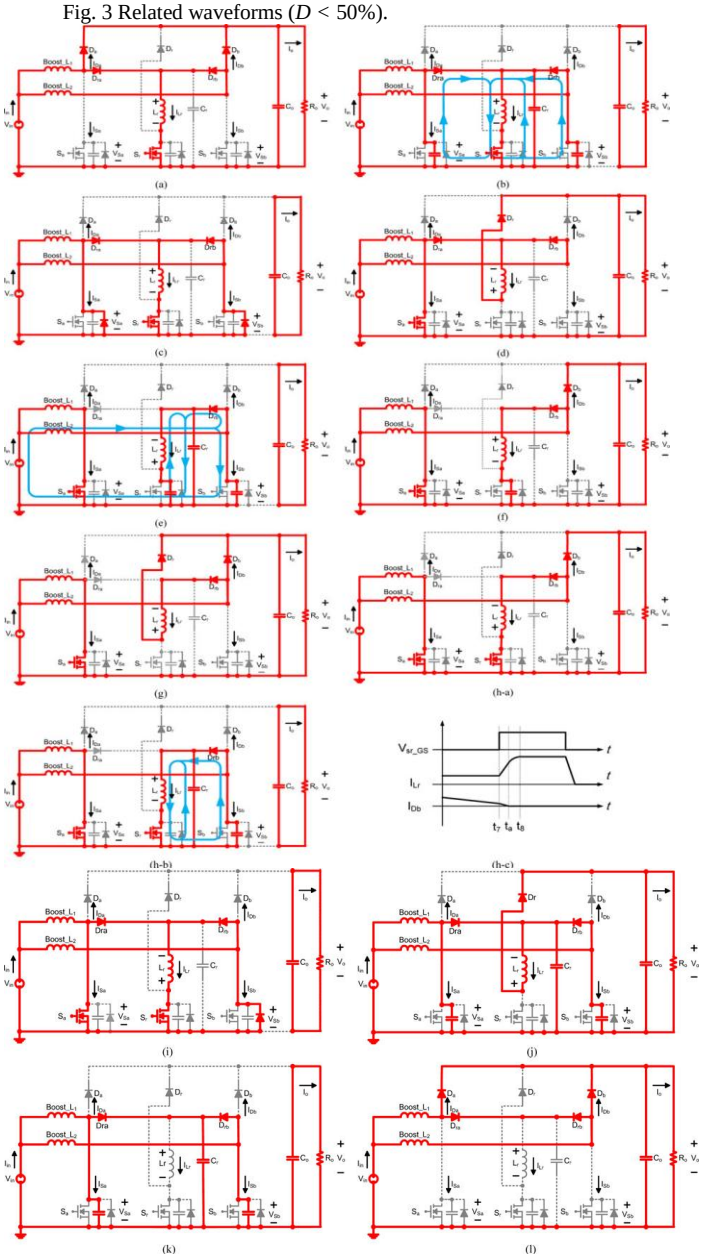


Fig. 4 Equivalent circuits of different modes (*D* < 50%). (a) Mode 1 [t_0 –t_1]. (b) Mode 2 [t_1 –t_2]. (c) Mode 3 [t_2 –t_3]. (d) Mode 4 [t_3 –t_4]. (e) Mode 5 [t_4 –t_5].
(f) Mode 6 [t_5 –t_6] (g) Mode 7 [t_6 –t_7]. (h-a) Mode 8 [t_7 –t_a]. (h-b) Mode 8 [t_a–t_8]. (h-c) Detailed waveform of the Mode 8. Equivalent circuits of different modes (*D* <50%). (i) Mode 9 [t_8 –t_9]. (j) Mode 10 [t_9 –t_{10}]. (k) Mode 11 [t_{10} –t_{11}]. (l) Mode 12 [t_{11} –t_{12}].

Mode 2 [t_1 –t_2]: In mode 2, the resonant inductor current continues to increase to the peak value, and the main switch voltages V_{Sa} and V_{Sb} decrease to zero, because the resonance occurs among C_{Sa}, C_{Sb}, C_r and L_r . Then, the body diodesD_{Sa} (S_a) and D_{Sb} (S_b) can be turned ON.The resonant time t_{12} and resonant inductor current i_{Lr} (t_2) Are

$$t_{12} = \frac{\pi}{2\omega_0} = \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sa} + C_{Sb} + C_r)} \quad (2)$$

$$i_{Lr}(t_2) = I_{\text{in}} + \frac{V_o}{Z_0} = I_{\text{in}} + \frac{V_o}{\sqrt{L_r/(C_{Sa} + C_{Sb} + C_r)}} \quad (3)$$

where

$$\omega_0 = \frac{1}{\sqrt{L_r (C_{Sa} + C_{Sb} + C_r)}}$$

$$Z_0 = \sqrt{\frac{L_r}{(C_{Sa} + C_{Sb} + C_r)}}.$$

Mode 3 [t_2 –t_3]: Fig. 4(c) shows the equivalent circuit of this mode. At the end of mode 2, the main switch voltage V_{Sa} decreases to zero, so the body diode D_{Sa} of S_a is turned ON at t_2 . At this time, the main switch can achieve ZVS. The on-time t_{03} of the auxiliary switch S_r needs to be more than t_{01} + t_{12} to achieve the function of ZVS. The interval time t_{03} is

$$t_{03} \geq t_{01} + t_{12} = L_r \cdot \frac{I_{\text{in}}}{V_o} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sa} + C_{Sb} + C_r)}. \quad (4)$$

Mode 4 [t_3 –t_4]: Fig. 4(d) shows the equivalent circuit of this mode. In this mode, the auxiliary switch S_r is turned OFF, and the clamped diode D_r is turned ON. During this interval, the energy stored in the resonant inductor L_r is transferred to the output load. The resonant inductor current I_{Lr} decreases to zero
and the clamped diode D_r is turned OFF at t_4 . The energy discharge time of the resonant inductor is

$$t_{34} = \frac{L_r}{V_o} \left(I_{\text{in}} + \frac{V_o}{\sqrt{L_r/(C_{Sa} + C_{Sb} + C_r)}} \right). \quad (5)$$

Mode 5 [t_4 –t_5]: In this mode, the clamped diode D_r is turned
OFF. The energy of the boost_L_2 is transferred to C_r and C_{Sb} and the energy stored in the parasitic capacitor C_{Sr} of the auxiliary switch is transferred to the resonant inductor L_r and resonant capacitor C_r at this time. The rectifier diode D_b is turned ON when the voltage across the main switch S_b reaches V_o at t = t_5 .

Mode 6 [t_5 –t_6]: Fig. 4(f) shows the equivalent circuit. The parasitic capacitor C_{Sr} of the auxiliary switch is linearly charged
by I_{L2} − I_o to V_o . Then, the clamped diode D_r is turned ON at t_6 .The interval time t_{56} is

t_{56} = (C_{Sr} • V_o)/I_{L2} − I_o

. The resonant inductor current i_{Lr} (t) is

$$i_{Lr}(t) = -V_o \sqrt{\frac{CC_{Sr}}{L_r (C + C_{Sr})}} \sin \sqrt{\frac{C + C_{Sr}}{L_r C C_{Sr}}} t + \frac{I_{L2} C_{Sr}}{C + C_{Sr}} \times \left(1 - \cos \sqrt{\frac{C + C_{Sr}}{L_r C C_{Sr}}} t \right). \quad (6)$$

The resonant time t_{45} is

$$t_{45} = \pi \sqrt{\frac{L_r C C_{Sr}}{C + C_{Sr}}} \quad (7)$$

where $C = C_r + C_{Sb}$.

Mode 7 [t_6 –t_7]: Fig. 4(g) shows the equivalent circuit. In this
mode, the clamped diode D_r is turned ON. The energy stored in the resonant inductor L_r is transferred to the output load by
the clamped diode D_r. At t_7 , the clamped diode D_r is turned OFF because the auxiliary switch Sr is turned ON. The interval time t_{67} and the resonant inductor current are
t_{67} = D_1T − ($D_{rc}T$ + t_{36}) ---------- (9)
i_{Lr} (t_7) ≈ i_{Lr} (t_6) = I_{L2} − I_o ----------. (10)

Mode 8 [t_7 –t_8]: In the interval [t_7–t_a], the resonant inductor
current I_{Lr} increases linearly until it reaches I_{L2} and the rectifier
diode current I_{Db} decreases to zero at t = t_a , so the rectifier diode D_b is turned OFF. Fig. 4(h-a) shows the equivalent circuit and the detailed waveform is shown in Fig. 4(h-c). The interval time t_{7a} is
t_{7a} = L_r • I_o/V_o ----------. (11)

As for the interval time [t_a–t_8], Fig. 4(h-b) shows the equivalent
circuit. The resonant inductor current continues to increase to the peak value and the main switch voltage V_{Sb} decreases to zero because of the resonance among C_{Sb}, C_r , and L_r. At t = t_8 , the body diode D_{Sb} of S_b is turned ON. The interval time t_{a8} is

$$t_{a8} = \frac{\pi}{2\omega_1} = \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sb} + C_r)}. \quad (12)$$

Then, t_{78} is

$$t_{78} = t_{7a} + t_{a8} = L_r \cdot \frac{I_o}{V_o} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sb} + C_r)}. \quad (13)$$

Mode 9 [t_8 –t_9]: In this mode, the resonant inductor current I_{Lr} is equivalent to a constant current source. In order to meet the demand that the main switch S_a is turned OFF under the ZCS condition, i_{Lr} (t_8) ≈ i_{Lr} (t_9) must be greater than I_{in} . Then the main switch currents I_{Sa} and I_{Sb} are less than or equal to zero,
so the main switch S_a is turned OFF under the ZCS condition.
The interval time t_{89} is
t_{89} = D_1T − t_{38}. (14)
And, the zero-current switching conditions are

1) $i_{Lr}(t_8) \approx i_{Lr}(t_9) = i_{Lr}(t_a) + \dfrac{V_o}{\sqrt{L_r/(C_{Sb}+C_r)}} \geq I_{\text{in}}$ (15)

2) the duty time of ZCS is longer than the interval time t_{78} ($D_{rc}T > t_{78}$).

Mode 10 [t_9 –t_{10}]: When the main switch S_a and the auxiliary switch S_r are turned OFF, the energy stored in the resonant inductor L_r is transferred to the output load by the clamped diode D_r . When the resonant inductor current I_{Lr} decreases to zero at t_{10}, the clamped diode D_r is turned OFF. Then, the capacitors C_{Sa}, C_{Sb}, and C_r are charged by I_{in} .

The interval time t_{9-10} and capacitor voltages of C_{Sa}, C_{Sb}, and C_r are

$$t_{9-10} = \frac{L_r}{V_o}\left(i_{Lr}(t_a) + \frac{V_o}{Z_1}\right) = \frac{L_r}{V_o}\left(i_{Lr}(t_a) + \frac{V_o}{\sqrt{L_r/(C_r + C_{Sb})}}\right) \quad (16)$$

$$V_{Cr}(t_{10}) = V_{Sa}(t_{10}) = V_{Sb}(t_{10}) = \frac{1}{(C_{Sa}+C_{Sb}+C_r)}\int_{t9}^{t10}[I_{\text{in}} - i_{Lr}(t)]\,dt. \quad (17)$$

Mode 11 [t_{10}–t_{11}]: The capacitors C_{Sa}, C_{Sb}, and C_r are linearly charged by I_{in} to V_o , and the rectifier diodes D_a and D_b are turned ON at t_{11}.This charged time t_{10-11} is

$t_{10-11} = (C_{Sa} + C_{Sb} + C_r)\,.\,(V_o - V_{Cr}(t_{10}))/I_{\text{in}}$------. (18)

Mode 12 [t_{11}–t_{12}]: In this mode, the operation of the interleaved boost topology is identical to that of the conventional boost converter. Fig. 4(l) shows the equivalent circuit. The ending time t_{12} is equal to the starting time t_0 of another cycle, because the operation of the interleaved topology is symmetrical.

The interval time t_{11-12} is

$t_{11-12} = T/2 - (D_1T + t_{03} + t_{9-11})$---------- (19)

1) *Voltage Ratio of D < 50% Mode:* Fig. 5(a) shows the real waveforms of the proposed circuit and Fig. 5(b) shows thesimplified waveforms.We can ignore some trivial stages. Table I shows the correspondence between the real stages and simplified ones. Fig. 6 shows the equivalent circuits about the operation for the boost inductor Boost_L1 . The inductor Boost_L2 has the similar results. So, when the switch is turned ON, the boost inductor current can be derived to be (2)

$$\sum_{Sa=\text{on}} \Delta i_{L1} = \frac{V_{\text{in}} \times (\Delta t_{bc} + \Delta t_{de} + \Delta t_{ef} + \Delta t_{fg} + \Delta t_{hi})}{L_1} = \frac{V_{\text{in}} \times (D_1 + D_{rc} + 2D_{rv})\,T}{L_1}. \quad (20)$$

And when the switch is turned OFF, the boost inductor current is

$$\sum_{Sa=\text{off}} \Delta i_{L1} = \frac{(V_{\text{in}} - V_o) \times (\Delta t_{ab} + \Delta t_{cd} + \Delta t_{gh})}{L_1} = \frac{(V_{\text{in}} - V_o) \times [1 - (D_1 + D_{rc} + 2D_{rv})]T}{L_1}. \quad (21)$$

Then, the voltage conversion ratio can be derived to be

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1 - (D_1 + D_{rc} + 2D_{rv})}. \quad (22)$$

…

Fig. 5 Switching stages (D <50%). (a) Real switching stages. (b) Simplified switching stages.

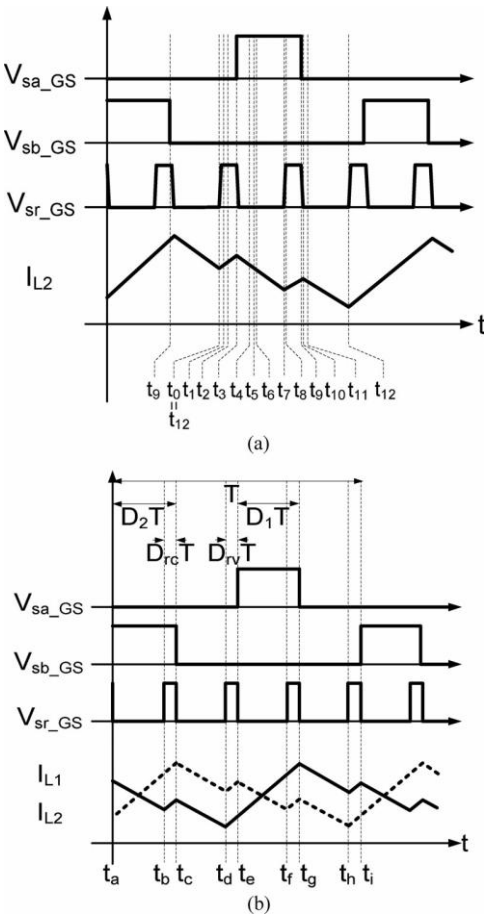


TABLE I
CORRESPONDENCE BETWEEN THE REAL STAGES AND THE SIMPLIFIED ONES (D< 50%)

Real operation stages	Simplified operation stages (Boost_L_1)	Simplified operation stages (Boost_L_2)
$[t_0\text{-}t_3]$	$[t_d\text{-}t_e]$	$[t_h\text{-}t_i]$
$[t_3\text{-}t_7]$	$[t_e\text{-}t_f]$	$[t_a\text{-}t_b]$
$[t_7\text{-}t_{10}]$	$[t_f\text{-}t_g]$	$[t_b\text{-}t_c]$
$[t_{10}\text{-}t_{12}]$	$[t_g\text{-}t_h]$	$[t_c\text{-}t_d]$

B. Operational Analysis ofD >50% Mode

The principle of the proposed topology operated in *D* >50% mode is described in this section. There are 14 operational modes in the complete cycle. Only seven modes related to the main switch S_a are analyzed, because the interleaved topology is symmetrical. Fig. 7 shows the waveforms when the duty cycle of the main switch is more than 50%. Some assumptions simplifying the circuit analysis are like those in*D*<50% mode

.

Mode 1 [t_0 –t_1]: Fig. 8(a) shows the equivalent circuit. In this mode, all switches S_a , S_b , and S_r are turned ON, and the rectifier diodes D_a and D_b and clamped diode D_r are turned OFF. The main switch currents I_{Sa} and I_{Sb} are less than

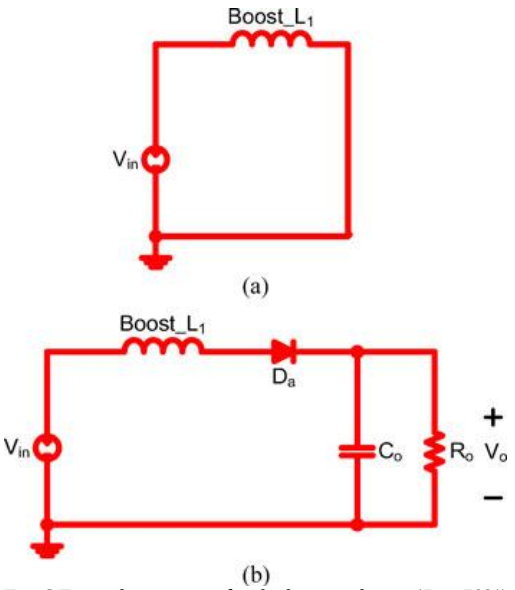
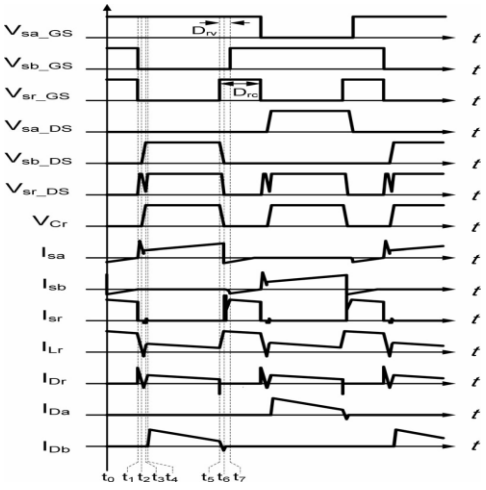


Fig. 6 Equivalent circuits for the boost inductor (*D* < 50%). (a) Boost_L_1 in
the stage [t_b –t_c], stage [t_d –t_e], stage [t_e –t_f], stage [t_f –t_g] and stage [t_h –t_i]. (b) Boost_L_1 in the stage [t_a –t_b], stage [t_c –t_d] and stage [t_g –t_h].

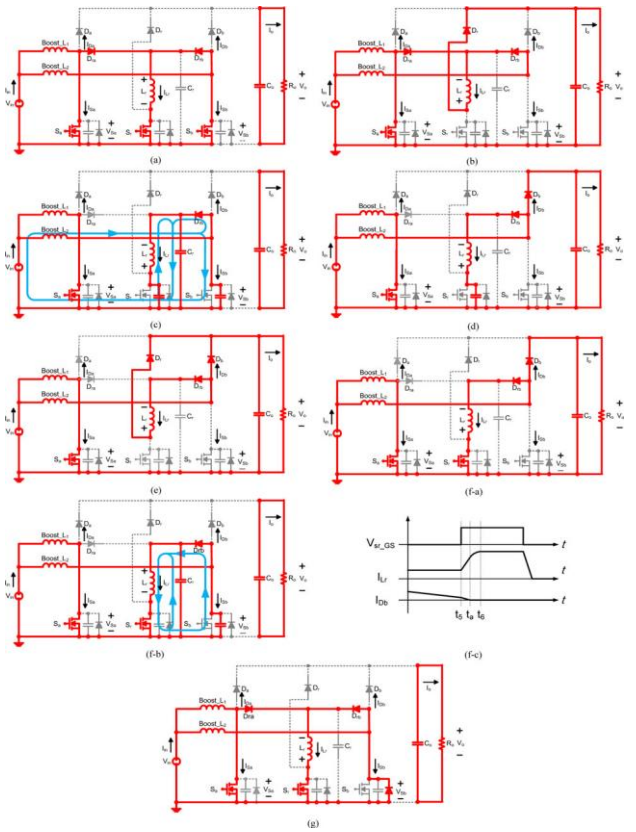
equal to zero when the previous mode ends. The main switch
S_b can achieve the ZCS characteristic at $t = t_1$ if the condition
in (24) can be met.The interval time t_{01} and the resonant inductor current are



$$t_{01} = (D_1 - t_{07})T = (D_1 - 0.5)T \qquad (23)$$

$$i_{Lr}(t_1) = i_{L2}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{Sb} + C_r)}} \geq I_{\text{in}}. \qquad (24)$$

Fig. 8 Equivalent circuits of different modes (*D* > 50%). (a) Mode 1 [t_0 –t_1]. (b) Mode 2 [t_1 –t_2]. (c) Mode 3 [t_2 –t_3]. (d) Mode 4 [t_3 –t_4]. (e) Mode 5 [t_4 –t_5].
(f-a) Mode 6 [t_5 –t_a]. (f-b) Mode 6 [t_a –t_6]. (f-c) Detailed waveform of the Mode 6. (g) Mode 7 [t_6 –t_7].



Mode 2 [t_1 –t_2]: The energy stored in the resonant inductor L_r is transferred to the output load by the clamped diode D_r , because the auxiliary switch S_r is turned OFF. When the resonant inductor current I_{Lr} decreases linearly until it reaches zero at $t = t_2$, the clamped diode D_r is turned OFF. The interval time t_{12} is

$t_{12} = L_r V_o / I_{\text{in}}$ ----------. (25)

Mode 3 [t_2 –t_3]: In this mode, the clamped diode D_r is turned OFF. The energy stored in the boost_L_2 and the energy stored in the parasitic capacitorC_{Sr} of the auxiliary switch are transferred to the resonant inductor L_r , resonant capacitor C_r , and parasitic capacitor C_{Sb} of the main switch at this time. The rectifier diode D_b is turned ON when the main switch voltage V_{Sb} and resonant capacitor voltage V_{Cr} increase to V_o at $t = t_3$.

$$i_{Lr}(t) = -V_o\sqrt{\frac{CC_{Sr}}{L_r(C+C_{Sr})}}\sin\sqrt{\frac{C+C_{Sr}}{L_rCC_{Sr}}}t + \frac{I_{L2}C_{Sr}}{C+C_{Sr}} \times \left(1-\cos\sqrt{\frac{C+C_{Sr}}{L_rCC_{Sr}}}t\right). \quad (26)$$

The resonant time t_{23} is

$$t_{23} = \pi\sqrt{\frac{L_rCC_{Sr}}{C+C_{Sr}}}. \quad (27)$$

Mode 4 [t_3 –t_4]: After t_3 , the parasitic capacitor C_{Sr} of the auxiliary switch is linearly charged by $I_{L2} - I_o$ to V_o . Then, the clamped diode D_r is turned ON at t_4 .
The interval time t_{34} is

$t_{34} \approx C_{Sr} \cdot V_o/I_{L2} - I_o$---------- (28)

Mode 5 [t_4 –t_5]: Fig. 8(e) shows the equivalent circuit. At t_4 , the clamped diodeD_r is turned ON. The energy stored in the inductor L_r is transferred to the output load by the clamped diode D_r . The clamped diode D_r is turned OFF when the auxiliary switch S_r is turned ON at $t = t_5$.

$t_{45} = 0.5T - t_{04} - D_{rv}T$---------- (29)
$i_{Lr}(t_5) = i_{Lr}(t_4)$.---------- (30)

Mode 6 [t_5 –t_6]: Fig. 8(f-a) shows the equivalent circuit and the detailedwaveform is shown in Fig. 8(f-c). In the interval [t_5– t_a], the resonant inductor current I_{Lr} increases linearly until it reaches I_{L2} and the rectifier diode current I_{Db} decreases to zero at $t = t_a$, then the rectifier diode D_b is turned OFF.
The interval time t_{5a} is

$t_{5a} = L_r \cdot I_oV_o$.---------- (31)

As for the interval time [t_a–t_6], Fig. 8(f-b) shows the equivalent circuit. The resonant inductor current continues to increase to the peak value and the main switch voltage V_{Sb} decreases to zero because of the resonance among C_{Sb}, C_r , and L_r. At t_6 , the body diode D_{Sb} of S_b is turned ON.

The interval time t_{6a} is

$$t_{a6} = \frac{\pi}{2\omega_1} = \frac{\pi}{2}\cdot\sqrt{L_r\cdot(C_{Sb}+C_r)}. \quad (32)$$

And the interval time t_{56} is

$$t_{56} = t_{5a} + t_{a6} = L_r\cdot\frac{I_o}{V} + \frac{\pi}{2}\cdot\sqrt{L_r\cdot(C_{Sb}+C_r)}. \quad (33)$$

Mode 7 [t_6–t_7]: When the resonant capacitor voltage V_{Cr} and the main switch voltage V_{Sb} are equal to zero, the body diode D_{Sb} of S_b is turned ON. Then, Mode 7 will start. In this mode, the resonant inductor current I_{Lr} is equal to a constant current source. If the condition of $i_{Lr}(t_6) \approx i_{Lr}(t_7) \geq I_{in}$ can be satisfied, the main switch currents I_{Sa} and I_{Sb} can be less than or equal to zero. Then, the main switch S_a can be turned OFF under the ZCS condition. And the main switch S_b reaches ZVS because of the conduction of the body diode D_{Sb} in this mode. The interval time t_{67} is

$t_{67} = 0.5T - t_{06}$. (34)

And the zero-current switching conditions are

1)

$$i_{Lr}(t) = i_{L2}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{Sb}+C_r)}} \geq i_{in}(t) \quad (35)$$

2) the duty time of ZCS is longer than the interval time $t56$ ($DrcT > t56$).

1) Voltage ratio of D > 50% Mode: Fig. 9(a) shows the real waveforms and Fig. 9(b) shows the simplified waveforms in this mode. Some trivial stages are ignored. Table II shows the correspondence between the real stages and the simplified ones. Fig. 10 shows the equivalent circuits of the operation for the boost inductor Boost_L1 .

$$\sum_{Sa=\text{on}}\Delta i_{L1} = \frac{V_{in}\times(\Delta t_{ab}+\Delta t_{bc}+\Delta t_{cd}+\Delta t_{de}+\Delta t_{fg})}{L_1} = \frac{V_{in}\times(D_1+D_{rv})T}{L_1}. \quad (36)$$

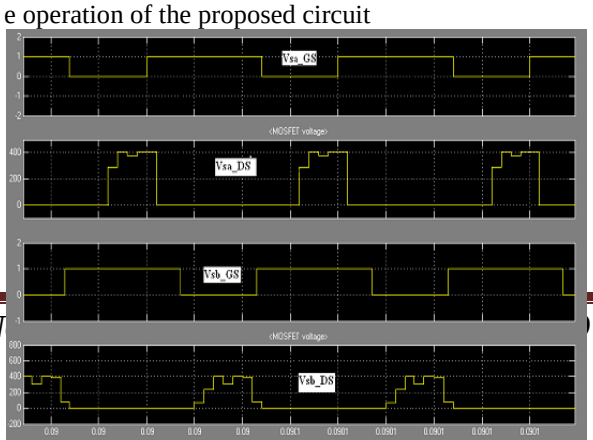
And when the switch is turned OFF, the boost inductor current is

$$\sum_{Sa=\text{off}}\Delta i_{L1} = \frac{(V_{in}-V_o)\times(\Delta t_{ab}+\Delta t_{cd}+\Delta t_{gh})}{L_1} = \frac{(V_{in}-V_o)\times[1-(D_1+D_{rc}+2D_{rv})]T}{L_1}. \quad (37)$$

Then, the voltage conversion ratio can be derived to be
$V_o/V_{in}=1/(1-(D_1+D_{rv}))$ ---------- (38)

SIMULATION RESULTS OF ZCS AND ZVS INTERLEAVED BOOST CONVERTER

Figs. 12–13 show the simulation results. They verify th e operation of the proposed circuit



(b)

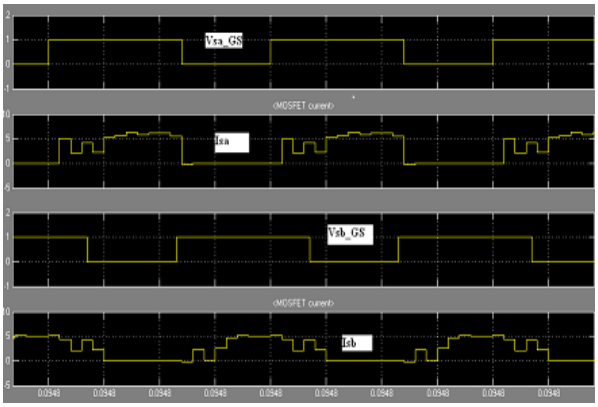
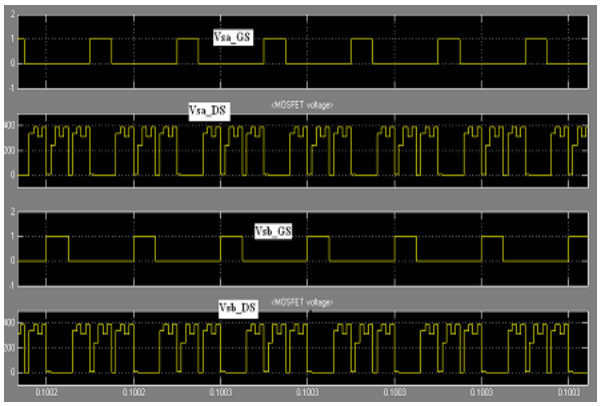


Fig. 12 Simulation waveforms of the main switches S_a and S_b (D > 50% and load current 1.5A). (a) ZVS. (b) ZCS



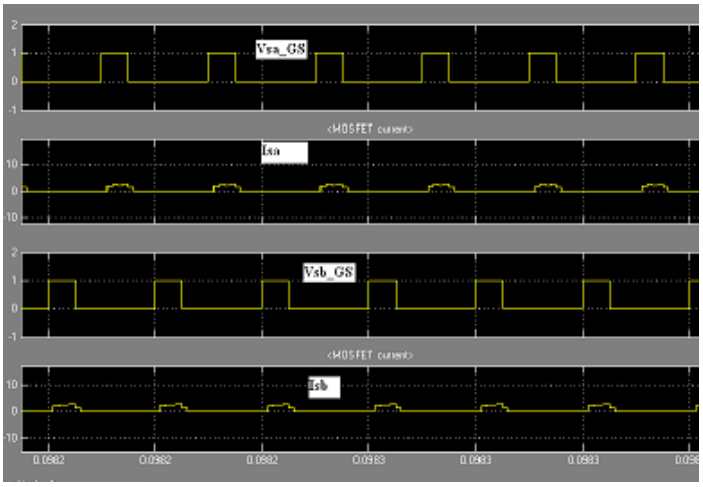


Fig. 13 Simulation waveforms of the main switches S_a and S_b (D < 50%).
(a) ZVS. (b) ZCS

ZCS AND ZVS INTERLEAVED BOOST CONVERTER

Design of Interleaved Buck Converter The switches of the zero current switching (ZCS) Buck converter turn on and off at zero current. The circuit shown in the fig.14 consists of the inductor connected in series with the switch to achieve ZCS. This type of connection is called as L type connection which is advantageous than the other type of connection called the M type. In M type of connection an amount of energy is trapped in the inductor due to the recovery times of the practical devices. This results in the voltage transients across the switch. This condition favors the L type over M type

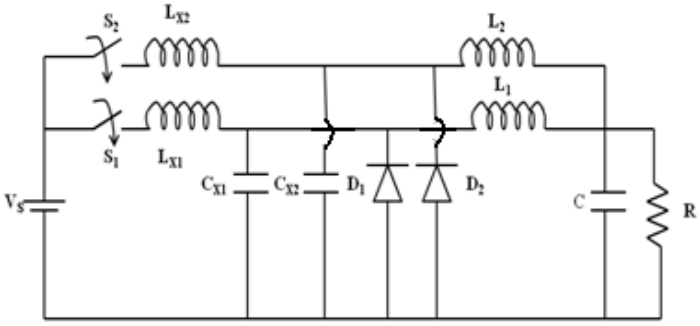


Fig:14-schematic diagram of ZCS interleaved buck converter

The ZCS Interleaved Buck Converter comprises of the resonant component inductors LX1, LX2 and capacitors CX1 and CX2, inductors L1 and L2, a capacitor C, two semiconductor switches, two diodes D1 and D2 and a load resistor R.The resonant components can be determined as follows: The ratio between the peak resonant current and the load current is given by the following equation

$$x = \frac{I_m}{I_o} = \frac{V_S}{I_o}\sqrt{\frac{C_x}{L_x}}$$

CLOSED LOOP CONTROL SCHEME FOR DC

The closed loop control system for the ZCS Interleaved Buck converter with PID controller feedback is shown in the Figure Figure 3. Functional Block diagram of closed loop control of dc

The ultimate aim in designing the controller is to minimize the error between V from the Figure 15, the important functional blocks that are evident are: PID Controller, PWM (Pulse Width

Modulation) and dc-dc converter. The PID Controller acts as a c

by compensating the error signal (Ve).PWM block is for the generation of driver signal obtained from the compensator. The error (Ve) between the output voltage (Vo) and reference voltage (Vref) is processed by the compensator block with PID Controller algorithm to generate control signal. The control signal significantly affects the converter characteristics and therefore effective tuning of the controller is one of the desired aspects of the control system. The f corresponding to the error signal which is then converted as switching pulses using the PWM functional block.

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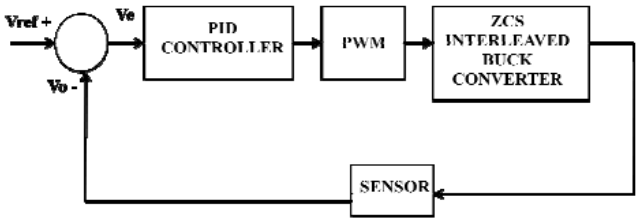

Fig:15 Functional Block diagram of closed loop control of interleaved buck converter

SIMULATION RESULTS OF ZCS AND ZVS INTERLEAVED BOOST CONVERTER

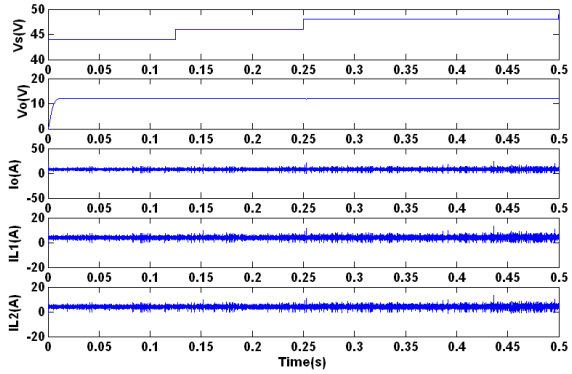

Fig. 16. Simulation results for ZCS Interleaved Buck Converter(V_SInput Voltage, V_O-Outpur Voltage, I_O-Load Current, I_{L1} and I_{L2} –Inductor Currents)

It is obviously understood from the simulation results that for the input transients of 44V-46V-48V, the output voltage is maintained constant, which is considered as 12V.The output voltage settles down much faster and hence the dynamic performance of the converter is improved. No undershoots and overshoots are evident. The output voltage ripple is almost negligible. It is understood from fig.16 that the two inductors L1 and L2 share the current equally and hence good current sharing is being achieved which is one of the major advantages in designing the controller. The simulation results reveal the fact that the PID controller is the robust one in which the results are in concurrent with the mathematical calculations. The converter is designed in time domain and hence the converter specifications are very well met. The output current contains some ripple which is evident from fig16 needs some improvement..

CONCLUSION

A novel interleaved boost and converter with both zero-voltage switching and zero-current-switching functions and A closed loop control system has been designed for them ZCS Interleaved Buck converter in continuous time domain using robust PID controller. The simulation results thus obtained using MATLAB/Simulink is in agreement with the mathematical calculations. is proposed in this paper. The duty cycle of this topology can be more or less than 50%.s rudeness to perturbations on the ac network.

1) The main switches S_a and S_b can achieve both ZVS and ZCS.
2) The voltage stress of all switches is equal to the output voltage.
3) It has the smaller current stress of elements.
4) It uses the resonant inductor L_r , resonant capacitor C_r , parasitic capacitors C_{sa} and C_{sb}, and auxiliary switch S_r to become a common resonant way to reach ZVS and ZCS of the main switches S_a and S_b .
5) The driving circuit can automatically detect whether the driving signals of the main switches are more than 50% or not and get the driving signal of the auxiliary switch.
6) The users can only apply the ZVS or ZCS function just by the adjustment of the driving circuit
7) The efficiency is 94.6% with output power of 600W and input voltage of 150V and it is 95.5% with output power of 400W and input voltage of 250V
8)The study show that the ZCS interleaved buck converter with PID controller thus designed achieves tight output voltage regulation and good dynamic performances

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