

# Parallel Prefix Algorithm for OTIS-HHC Architecture

Abdul Hannan Akhtar<sup>1</sup>, Keny Thomas Lucas<sup>2</sup>

<sup>1</sup>Department of Electronics and Communication Engineering,  
Government Polytechnic, Ranchi, Jharkhand, India  
abdulhannan.akhtar@gmail.com

<sup>2</sup>Principal, Xavier Institute of Polytechnic and Technology,  
Ranchi, Jharkhand, India  
kenny.lucas@gmail.com

**Abstract:** The OTIS (Optical Transpose Interconnection System) has become one of the popular models for developing parallel algorithms solving various computation and communication intensive problems. Various real life problems including job scheduling, knapsack, loop optimization, evaluation of polynomials, solutions of linear equations, and polynomial interpolation depend on the time complexity of prefix computation for the efficiency for their respective solutions. In this paper, we have proposed an algorithm for parallel prefix computation on OTIS-Hyper Hexa-cell. In this architecture, the time complexity of the algorithm for  $n^2$  data elements is  $O(n)$  electronic moves and  $O(n)$  OTIS moves.

**Keywords:** Interconnection network, OTIS-HHC, time complexity, parallel algorithm, prefix.

## 1. Introduction

When you submit your paper print it in two-column format, including figures and tables. In addition, designate one author as the “corresponding author”. This is the author to whom proofs of the paper will be sent. Proofs are sent to the corresponding author only.

The OTIS (Optical transpose Interconnection System) [1], [2], [3] is a hybrid system that exploits the best features of electronic links as well as optical links for developing parallel architectures. The optical links are superior to electronic links in terms of power, speed and crosstalk properties if the connect distance between processors is more than a few millimeters. The electronic links are preferred to optical links for smaller distance between processors. The total number of processors in the network is divided into groups and each group can be assumed to be a microchip in an OTIS model. All the processors within a group are connected through the electronic links whereas the processors of one group are connected to the processors of different groups through the optical links. The number of groups in an OTIS network can be equal to the number of processors in each group for maximized bandwidth and minimized power consumption [4], [5]. The interconnection pattern of processors within each group determines the overall model of such system, i.e. an OTIS-G has G interconnection pattern for all of its groups. Some of the OTIS models are OTIS-Ring, OTIS-Mesh, OTIS-Hypercube, OTIS-Torus, OTIS-Mesh of trees. The OTIS-HHC is a newly proposed architecture of OTIS family [6].

In the recent years, researchers have proposed many parallel algorithms for various OTIS models that includes basic operations [7], matrix multiplication [8], [9], BPC permutation [10], sorting [11], [12], [13], [14], [15], [16], [17], routing

[11], [13], [17], image processing [18], construction of conflict graph [19], load balancing [20], [21], polynomial root finding [22], [23], polynomial interpolation [22], [24], prefix computation [25], [26], [27], [28], [29], [30], gossiping [31], [32], [33].

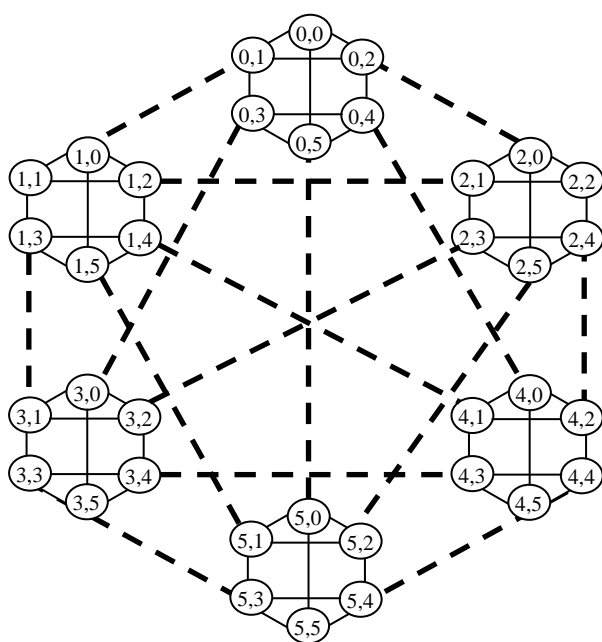
Many real-life problems, such as job scheduling, knapsack, loop optimization, evaluation of polynomials, solutions of linear equations, and polynomial interpolation depend on the efficiency of prefix computation for their solutions. For a given set of data elements, i.e.  $x_1, x_2, x_3, \dots, x_N$  belonging to a domain  $\mathcal{R}$ , the prefix computation can be given as  $P_i = x_1 \oplus x_2 \oplus x_3 \dots \oplus x_i$ ,  $1 \leq i \leq N$ , where  $\oplus$  is an associative operator over the domain  $\mathcal{R}$ . The algorithm proposed in for extended multi-mesh network requires  $O(N^{1/4})$  on  $N$  processors. The algorithm proposed for optical multi-trees requires  $O(\log n)$  electronic moves + 4 optical moves for  $n^3$  data elements on  $n^3 - n^2$  processors. In this paper we propose a parallel algorithm for prefix computation on a newly proposed OTIS model called OTIS-HHC [6]. Our proposed algorithm requires  $(3.5n+2)$  electronic moves and  $2(n-1)$  OTIS moves.

The rest of the paper is organized as follows. Section 2 describes the topology of the OTIS-HHC. Our proposed algorithm is discussed in section 3 followed by conclusion in section 4.

## 2. Topology of OTIS-HHC

The OTIS-HHC topology combines the attractive properties of both OTIS and hyper hexa-cell (HHC) topologies, where HHC is based on the properties of hypercube. The hypercube is one of the most versatile and efficient networks discovered so far for parallel computation. The topological structure and properties of an OTIS-HHC is based on that of hypercube, hyper hexa-cell (HHC) and OTIS topologies [6]. The topology

of each group in an OTIS-HHC is a hyper hexa-cell. A  $d_h$ -dimensional HHC constitutes a hypercube of dimension  $d_h+1$ . Various topological properties have been in discussed in detail [6]. The diameter of OTIS-HHC is  $(2d_h + 3)$ . The maximum and minimum degrees are  $(d_h+3)$  and  $(d_h+2)$  respectively. In an OTIS-HHC, the number of groups can be equal to the number of processors within each group or the number of groups can be half the number of processors within each group. The network size is  $(6 \times 2^{d-1})^2$  for  $G=P$  and  $((6 \times 2^{d-1})/2)^2$  for  $G=P/2$ . The bisection width of an OTIS-HHC is  $((6 \times 2^{d-1})/2)^2$  for  $G=P$  and  $((6 \times 2^{d-1})/4)^2$  for  $G=P/2$ . The OTIS-HHC is better in terms of diameter, minimum node degree, bisection width and optical cost than that of OTIS-Mesh. The topology of one-dimensional OTIS-HHC is shown in Fig. 1. The thin solid lines represent the electronic links connecting intra-group processing nodes. The dashed thick lines represent free space optical links representing inter-group processing nodes.



**Figure 1:** Topology of one-dimensional OTIS-HHC

In this architecture, the processing nodes of a hexa-cell are connected to processing nodes of other hexa-cells through the optical links using transpose rule. The processing elements represented by two indices. The first represents the group's number in the overall architecture and the second indicates the processor's number. Let any processing node be represented by  $(g,p)$ , then  $g$  indicates the position of group in the architecture in which processor  $p$  is located. The processor  $(g,p)$  is connected to the processor  $(p,g)$  through optical link as shown in Fig. 1.

### 3. Proposed Algorithm

The local prefix computation (within the group) is illustrated below through Table 1.

**Table 1:** Illustration of Prefix computation within the group

Step	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	P <sub>4</sub>	P <sub>5</sub>
1	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	A <sub>5</sub>
2		A <sub>0</sub>	A <sub>1</sub>		A <sub>3</sub>	A <sub>4</sub>

3			A <sub>0</sub>			A <sub>3</sub>
4	A <sub>pp</sub>	A <sub>pp</sub>	A <sub>pp</sub>			
5	A <sub>pr</sub>	A <sub>pr</sub>	A <sub>pr</sub>	A <sub>pr</sub>	A <sub>pr</sub>	A <sub>pr</sub>
6						A <sub>pg</sub>

It is obvious from the illustration presented in Table 1 that in step 1, all the processing nodes within each group are initialized with the data elements. It is also clearly seen that each group has two triangles and to exploit parallelism, we intend to compute partial prefix within the two rings in parallel. The content of the last processor of the upper triangle obtained in step 3 is broadcasted locally and then sent to the concerned connected processors of the lower ring in step 5. The final prefix computation is achieved in step 6 as shown in Table 1. This procedure is named as *LocalPrefix*. In our proposed algorithm, we will be using this procedure.

### Algorithm Prefix-HHC

```

Step 1: For all the groups, do in parallel
        LocalPrefix
Step 2: For all the groups, do in parallel
        j=0;
        for i = j to n-1
        {
            Broadcast the content of Pj locally in Gi
            Group Move (i)
            Calculate Sum
            j = j+1
        }

```

Time Complexity: Step 1 takes  $0.5n+1$  electronic moves. Step 2 needs  $3(n-1)$  electronic moves and  $2(n-1)$  OTIS moves. The overall requirement is  $(3.5n+2)$  electronic moves and  $2(n-1)$  OTIS moves.

## 4. Conclusion

In this paper, we have presented an algorithm for prefix computation on OTIS-HHC architecture. The time complexity of the algorithm has been represented in terms of data movement through the links;  $O(n)$  electronic moves and  $O(n)$  OTIS moves for  $n^2$  data elements.

## References

- [1] G. Marsden, P. Marchand, P. Harvey, and S. Esner, "Optical Transpose Interconnection System Architectures", *Optics Letters*, Vol. 18 (13), pp. 1083-1085, 1993.
- [2] F. Kiamilev, P. Merchand, A. Krishnamoorthy, S. Esener and S. Lee, "Optoelectronic and VLSI Multistage Interconnection Networks", *Journal of Lightwave Technology*, Vol. 9 (12), pp. 1674-1692, 1991.
- [3] F. Zane, P. Merchand, R. Paturi and S. Esener, "Scalable Architecture using the Optical Transpose Interconnection System (OTIS)", In *Proceedings of the International Conference on Massively Parallel Processing using Optical Interconnections*, MPPOI'96, San Antonio, Texas, pp. 114-121, 1996.
- [4] A. Krishnamoorthy, P. Merchand, F. Kiamilev and S. Esener, "Grain-size Consideration for Optoelectronic Multistage Interconnection Networks", *Applied Optics*, Vol. 21 (26), pp. 5480-5507, 1992.

- [5] M. Feldman, S. Esener, C. Guest, and S. Lee, "Comparison between Electrical and Free-space Optical Interconnects Based on Power and Speed Considerations", *Applied Optics*, Vol. 27 (9), 1988.
- [6] B. A. Mahfzah, A. Sleit, N. A. Hamad, E. F. Hamad, E. F. Ahmad and T. M. Abu-Kabeer, "The OTIS-Hyper hexa-cell Optoelectronic Architecture", *Computing*, Vol. 94 (5), pp. 411-432, 2012.
- [7] C. F. Wang and S. Sahni, "Basic Operations on the OTIS Mesh Optoelectronic Computer", *IEEE Transaction on Parallel and Distributed Systems*, Vol. 19 (12), pp. 1226-1236, 1998.
- [8] C. F. Wang and S. Sahni, "Matrix Multiplication on the OTIS-mesh Optoelectronic Computer", *IEEE Transactions on Computers*, Vol. 50 (7), pp. 635-646, 2001.
- [9] D. K. Mullick and P. K. Jana, "Matrix Multiplication on OTIS k-ary n-cube Network", In *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications*, pp. 224-228, 2008.
- [10] S. Sahni and C. F. Wang, "BPC Permutation on OTIS Hypercube Optoelectronic Computer", *Informatica*, Vol. 22 (3), pp. 263-269, 1998.
- [11] S. Rajasekaran and S. Sahni, "Randomized Routing, Selection, and Sorting on the OTIS-Mesh", *IEEE Transactions on Parallel and Distributed Systems*, Vol. 9 (9), pp. 833-840, 1998.
- [12] A. Osterloh, "Sorting on the OTIS-Mesh", In the *Proceedings of the 14th International Parallel and Distributed Processing Symposium (IPDPS\_S2000)*, pp. 269-274, 2000.
- [13] K. T. Lucas and P. K. Jana, "Sorting and Routing on OTIS-Mesh of Trees", *Parallel Processing Letters*, Vol. 20 (2), pp. 145-154, 2010.
- [14] K. T. Lucas, "Parallel Enumeration Sort on OTIS-Hypercube", In *Proceedings of the International Conference on Contemporary Computing*, pp. 21-31, 2010.
- [15] K. T. Lucas, "Parallel Algorithm for Sorting on OTIS-Ring Computer", In *proceedings of the Annual Computer Conference (COMPUTE 2009)*, Bangalore, India, pp. 1-5, 2009.
- [16] A. H. Akhtar and K. T. Lucas, "Enumeration Sort on OTIS k-ary n-cube Architecture", *International Journal of Engineering and Computer Science*, Vol. 3 (7), pp. 7173-7176, 2014.
- [17] A. H. Akhtar and K. T. Lucas, "Routing and Sorting on OTIS-Hyper Hexa-cell", *International Journal of Engineering and Computer Science*, Vol. 3 (7), pp. 7388-7393, 2014.
- [18] C. F. Wang and S. Sahni, "Image Processing on the OTIS-Mesh Optoelectronic Computer", *IEEE Transactions on Parallel and Distributed Systems*, Vol. 11 (2), pp. 97-109, 2000.
- [19] K. T. Lucas, D. K. Mallick, and P. K. Jana, "Parallel algorithm for the conflict graph on OTIS-Triangular array", In *Proceedings of the International Conference on Distributed Computing and Networking*, Springer-Verlag Berlin, Heidelberg, pp. 274-279, 2008.
- [20] B. Mahafzah and B. Jaradat, "The Load Balancing Problem in OTIS-Hypercube Interconnection Networks", *Journal of Supercomputing*, Vol. 46 (3), pp. 276-297, 2008.
- [21] C. Zhao, W. Xiao and B. Parhami, "Load-Balancing on a Swapped or OTIS Networks", *Journal of Parallel and Distributed Computing*, Vol. 69 (4), pp. 389-399, 2009.
- [22] P. K. Jana, "Polynomial Interpolation and Polynomial Root Finding on OTIS-mesh", *Parallel Computing*, Vol. 32 (4), pp. 301-312, 2006.
- [23] K. T. Lucas and P. K. Jana, "Parallel Algorithms for Finding Polynomial Roots on OTIS-Torus", *Journal of Supercomputing*, Vol. 46 (2), pp. 139-153, 2010.
- [24] K. T. Lucas, "Parallel algorithms for polynomial interpolation on OTIS-Hypercube parallel computer", in *Proceedings of the International Conference on Parallel and Distributed Techniques and Applications (PDPTA08)*, Las Vegas, Nevada, USA, Vo. 1, pp. 333-339, July 2008.
- [25] R. Cole and U. Vishkin, "Faster Optimal Parallel Prefix Sum and List Ranking", *Journal of Information and Control*, Vol. 4, pp. 334-352, 1989.
- [26] R. Lander and M. Fisher, "Parallel Prefix Computation," *Journal of ACM*, Vol. 27, pp.831-839, 1980.
- [27] C. P. Kriushkal, T. Madege and L. Rodolf, "Parallel Prefix on fully Connected Direct Connection Machines", In *Proceedings of the International Conference on Parallel Processing*, pp. 278-284, 1986.
- [28] C.P. Krushkal, L. Rudolph and M. Snir, "The Power of Parallel Prefix", *IEEE Transactions on Computers*, Vol. 100 (10), pp.965, 1985.
- [29] P. K. Jana, "Improved parallel prefix computation on optical multi-trees", in the *Proceedings of IEEE India Annual Conference (INDICON)*, pp.414-418, 2004.
- [30] A. Nicolan and H. Hwang, "Optimal Schedule for Parallel Prefix Computation with Bounded Resources", in the *Proceedings of 3rd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pp. 1-10, 1991.
- [31] K. T. Lucas, "The gossiping on OTIS-Hypercube optoelectronic parallel computer", in the *Proceedings of the International Conference on Parallel and Distributed Techniques and Applications*, Las Vegas, Nevada, USA, Vol. 1, pp. 185-189, June 2007.
- [32] K. T. Lucas, "The gossiping on OTIS-k-ary n-cube parallel computer," in the *Proceedings of the International Conference on Parallel and Distributed Techniques and Applications*, Las Vegas, Nevada, USA, Vol. 1, pp. 253-257, July 2007.
- [33] A. H. Akhtar and K. T. Lucas, "Comparison of Communication Algorithms on OTIS-HHC and OTIS-Ring Parallel Architectures", Vol. 3 (10), pp. 8741-8745, 2014.