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Exploiting a Low Power Self Timed Ternary CAM Architecture Using RWOS Mechanism

Silna George[1], I. Rabeek Raja[2], M. Prakash[3]
[1&3]P.G Scholar, Department of Electronics and communication, Ranganathan engineering college, Coimbatore.
[3]Assitant Professor, Department of Electronics and communication, Ranganathan engineering college, Coimbatore.

Abstract—***Content addressable memories are mostly used in computer networking devices. Power consumption is a major problem for these memories because of the parallel search operation. When compared to binary content addressable memories the mask cell increases the complexity and number of transistors. This paper introduces a new architecture for ternary content addressable memories. The proposed architecture called dual TCAM modifies the mask cell configuration so that the area and power consumption of the design can considerably be reduced. The search output from two CAM cells is used in the mask cell to work as a TCAM. As design example, a 8 × 4 bit TCAM is implemented and simulated by Tanner EDA Tool. The proposed TCAM achieves significant reduction in terms of power and number of transistors.***

***Index Terms*—Content addressable memory, low power, NAND type CAM, ternary CAM.**

I. INTRODUCTION

CAM is a memory that performs the look-up table function in a single clock cycle. The memory stores some data and the incoming data is compared against this stored data. If a matching data is finding from the memory locations then the memory returns the address of the data location. Some computer network applications require this type of operations. So this memory is widely used in network switches and network routers. The other applications include Hough transformation [1], image coding [2], intrusion prevention systems, and the periodic event generator [3]. As the requirement of CAM for various applications increases, the power consumption and area makes some critical challenges.

The content addressable memory mainly divides into two types called the binary CAM (BCAM) and ternary CAM (TCAM). One of the simplest CAM cell is the BCAM, in that memory the data search words consisting entirely 0's and 1's. But the TCAM allows one more state called the don't care so that it provides more flexibility and reliability in the search operation. As an example, the ternary cells have a stored word 100XX which will give a matched output for any of the four search words 10000, 10001, 10010, and 10011. This gives the additional flexibility to TCAM cells over binary cells. This feature is implemented to memory by adding mask cells to each memory cells.

A. CAM Fundamentals

A detailed model of CAM is shown in Fig. 1. The figure shows the CAM cell for 3 words and each word having 3 bits. That is each word corresponds to 3 CAM cells. There is a matchline is connected to each words and each CAM cell is connected with searchline pairs. The matchlines are connected to matchline sense amplifiers. Each CAM cell is stored with some data and the search operation starts with loading the register with search data. And also the matchlines are precharged to high value. The high value in the matchline shows a matched state. That is, at the beginning matchlines are temporarily in a matched state.

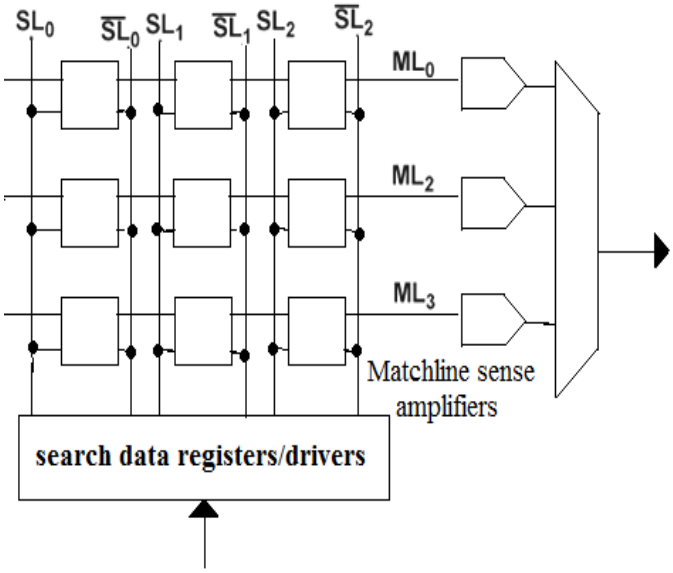

Fig.1. Detailed model of a CAM with 3 words having 3 bits. The schematic model shows matchlines, searchlines, and matchline sense amplifiers.

Next the search data from the register is given to the searchlines. The CAM cell compares the stored data against the search data bits on the searchlines. If the comparison result is a mismatched condition then the matchlines are discharged otherwise matchlines are remain in the precharged high state. The matchline sense amplifier finds the matched or mismatched condition. And the encoder encodes the matching location to its encoded address.

We arrange the reminder of this paper by giving a detailed look into CAM cells and explaining the proposed dual TCAM architecture. The different CAM core cells are explained in the next section, section II. In section III RWOS mechanism is reviewed. Section IV explains the proposed dual TCAM

architecture, which uses the concept of dual matchline TCAM.

II. BASICS OF CAM CORE CELLS

CAM cells are mainly meant to do bit storage and comparison. NOR type and NAND type CAM core cells are the two main CAM cells. SRAM cells are used for the storage of bits in both the types. For a simplified schematic, the NMOS access transistors and bit lines are not included in the figures.

A. NOR Cell

The comparison between the stored bit D and the search bit SL is carried out in the NOR cell. The schematic of a CAM cell is shown in Fig. 2. The cell uses the complementary of these bits to carry out the correct operations. The schematic also uses four transistors M_1, M_2, M_3, and M_4. A pulldown path is created by these transistors from the matchline. The pairs M_1/M_3 and M_2/M_4 creates the pulldown path. If the comparison of SL and D results in a mismatch, then it will create a pulldown path and connecting ML to ground. If the comparison results in a match output then it will disables all the pulldown paths and disconnecting ML from ground. For creating a CAM word, multiple cells are connected by shorting ML of each cell. This exploits the parallel nature of the architecture that is the NOR nature of this cell.

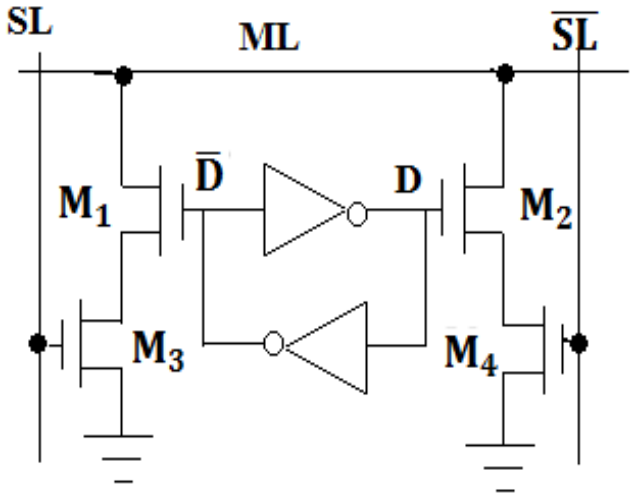

Fig.2. Schematic of a NOR cell

B. NAND Cell

The NAND cell also implements the comparison between the search data on the searchlines and the stored data bit D. Mainly three transistors M_1, M_D, and $M_{\bar{D}}$ are used by this cell for the comparison process. The working of this cell can be explained through an example. First consider the mismatch condition that is SL ≠ D. In this case at node A the logic value is "0" so that transistor M_1 gets turned off. For the other case SL = D the node A gets a logic value 1, so that M_1 gets turned on and passes the ML_n value to ML_{n+1} .NAND nature can be seen when multiple cells are serially connected. If every cell in a word results in a match condition then only it show the matching of the entire word. When we compare both of these cells we can see that NOR type works at high speed but power dissipation is high. While in NAND type cell power dissipation is less but it operates at medium speed. So NAND type cells are used in many applications.

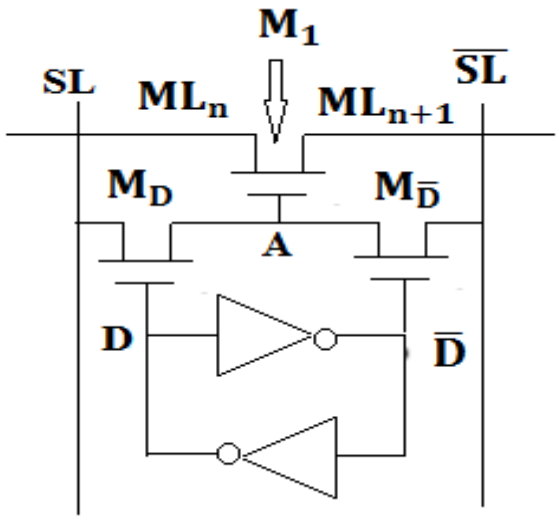

Fig.3. Schematic of a NAND cell

C. Ternary Cells

A traditional TCAM cell includes mainly three components. First one is the CAM cell next is the mask cell and last the evaluation logic. Fig. 4 shows a typical schematic of a ternary CAM cell. One of the main feature of TCAM is that it can store three states "0", "1", and "X". But in binary CAM it can store only two states "0", and "1". The mask bit (M) and stored data(D) inside the CAM cell determines the state of the CAM cell. If M = 0 there is always a match without considering the search data. And also if M = 1 then it will be a normal match based on the search data and stored data.

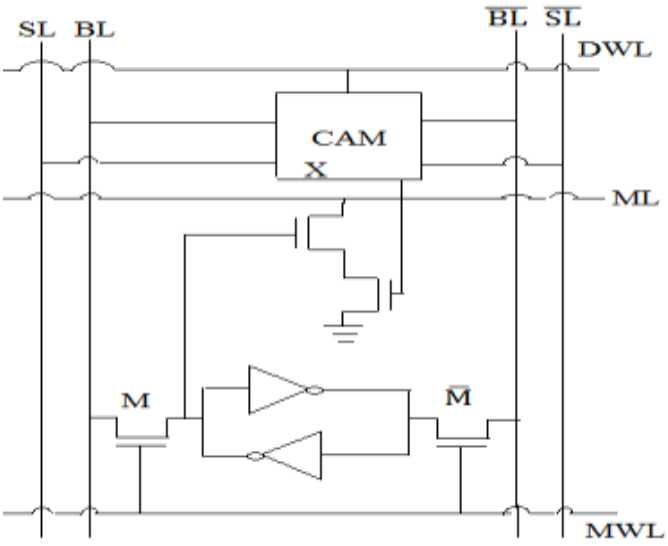

Fig.4. Schematic of a Ternary CAM cell

III. REVIEW OF RWOS MECHANISM

In our work we used the reordered word overlapped search mechanism for the implementation of the architecture. The basic idea behind this mechanism is that, by searching few bits a search words we can find most of the mismatches. And also locally generated timing signal is used for the circuit implementation. And there are two phases for their local operation pre-charge and evaluate.

A. Overlapped Search Mechanism

There are mainly two approaches for overlapped search mechanism. First one is word overlapped search mechanism and the second one is phase overlapped processing.

1) Word Overlapped Search

Fig. 5 shows a more detailed structure of a CAM circuit based on WOS scheme having an input controller.

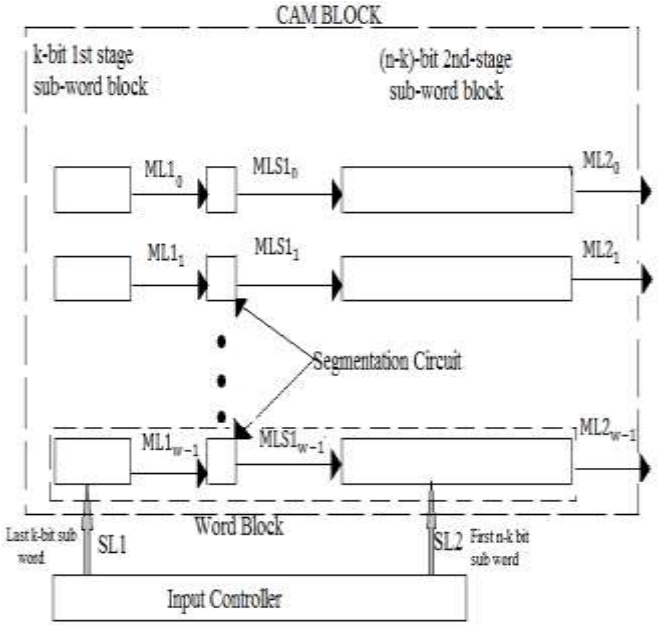

Fig.5. Detailed structure of a CAM having an input controller

From figure itself we can see that each word circuit is partitioned into different sections. The input controller controls the mode of operation of the CAM cell. If the consecutive input words are the same then the CAM works at slow mode and if the consecutive words are not same then the CAM works at fast mode. In the first segment of the word circuit last k bits of the sub word is compared if that result in a match then only goes for the next segment. If that is results in a mismatch then go for the next word because some bits are mismatched means the whole word is mismatched. If the consecutive sub search words are the same then the next search is initiated only after the current search is completed in both the segments. This results in the slow operation of the CAM word circuit. Then if the consecutive sub search words are not same then there is no need for going to the next segment. So that we can go for the next word search without going for the full word comparison process. This results in the fast operation of the CAM word circuits.

2) Phase Overlapped Processing

A typical CAM word circuit is implemented using NAND type cells shown in Fig. 6. These circuits works in two phases, precharge and evaluate phases.

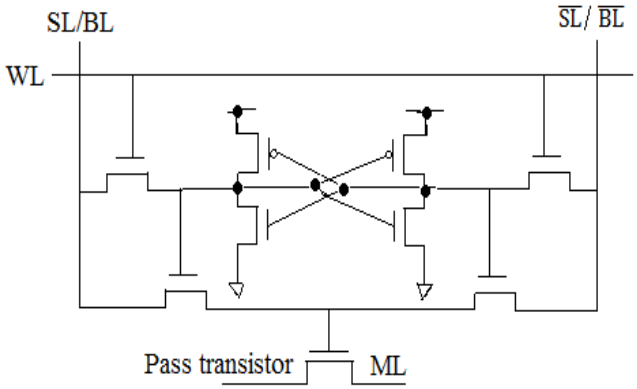

Fig.6. A typical NAND type CAM cell

The match line is connected with a PMOS transistor shown in Fig. 7 and in pre-charge phase ML is charged through this transistor. The match and mismatch operations are done in evaluate phase. If a search word matches with the stored word all pass transistors get turned on and discharges the ML capacitance.

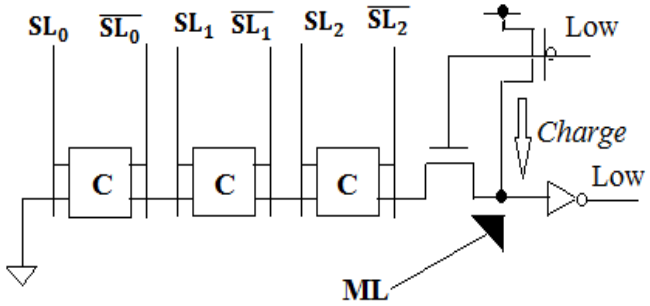

Fig.7. Schematic on precharge phase

When the stored word does not match with the search word pass transistors get turned off and the matchline voltage remains high.

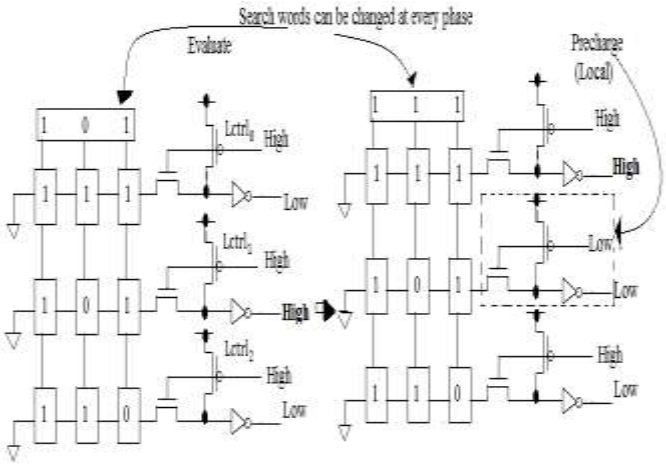

Fig.8. Phase overlapped processing scheme

Fig. 8 shows the schematic of phase overlapped processing scheme. In that each circuit is controlled by its local control signal. In this scheme local control signal is used only when a matching occurs in the previous phase then only charging occurs in the current phase. The other word circuits will be in the evaluate phase because of their high value in the lctrl signal.

B. Reordered Word Overlapped Search Mechanism

The Fig. 9 shows the schematic of RWOS mechanism. In which last k bits of a search word is compared with the last k bits of consecutive m search words and an extra word.

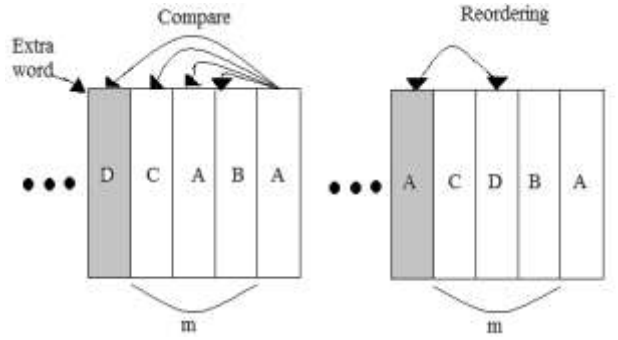

Fig.9. Schematic of RWOS scheme

Then any of the consecutive words are same as the current search word then that word is replaced with the extra search word that is different from the search word. So that circuit works at fast mode otherwise it will works at slow mode.

IV. DUAL TCAM ARCHITECTURE

In our work we are introducing a new architecture for ternary CAM cells. That is the dual TCAM.

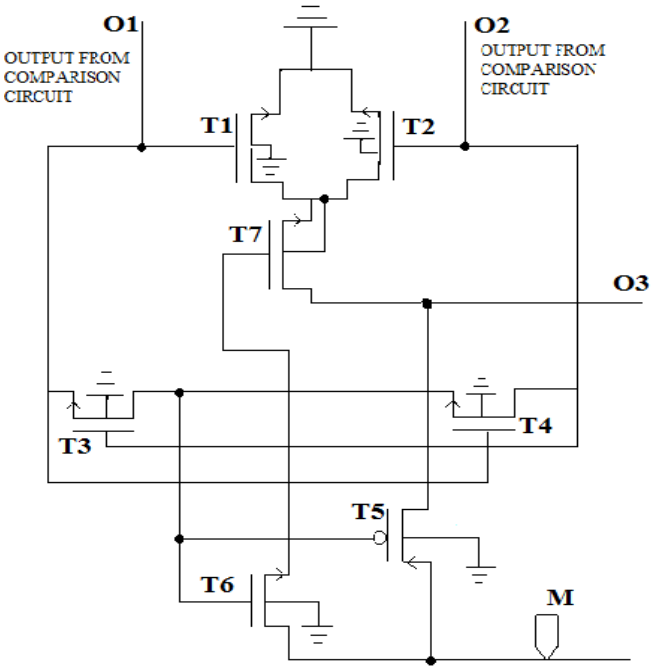

Fig.10. Proposed dual TCAM architecture

In which comparison output from two CAM cells are used for the mask cell operation. The proposed architecture is shown in Fig. 10.This architecture is derived from the dual matchline [4] concept. In a typical CAM cell only one bit comparison is taken place in one cell. And each cell uses a mask cell also. But in this architecture for two one bit comparison cells there is only one mask cell is present. So that for two cells, instead of using 34 transistors we can design it by 23 transistors.

Whenever the output value of this design, that is o3 is “0” value it shows a matching condition. That is stored data equals to the search data. And also when M value equals “1” then TCAM operates like a normal CAM memory. That is when the stored value equals to the search value it shows a matching condition. Otherwise it shows the mismatched condition. When the value of M is set to “0” value it always shows a matched condition irrespective of the search data. That is it performs a wild match. The output value o3 goes to the next CAM cell circuitry. That cell performs search operation based on this o3 output value.

For example o1 and o2 values are “1” that is a matched condition in both the CAM cells. Then the transistors T1, T2, T3, and T4 are activated. T1 and T2 pass the value “0” to T7. T3 and T4 activate the transistor T6. If the M value is set to “1” then T6 pass the value “1” to T7. So that T7 activated and pass the value “0” to output o3. That is the condition for matching. When o1 and o2 are “0” or any one of them is “0” then T1 and T2 may be in off condition or any one of them will be in off condition. This will activates T5 and passes the value “1” to output o3. That shows a mismatched condition.

V. EXPERIMENTAL RESULTS

Based on the proposed architecture TCAM is designed and simulated using Tanner EDA tool. The power results and number of transistors are compared for BCAM and TCAM that are designed using RWOS mechanism.

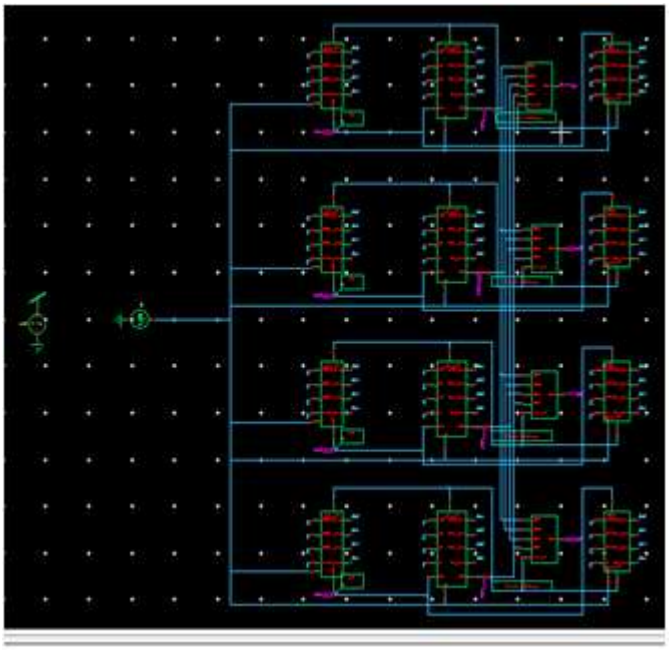

Fig.11. The schematic of the proposed 4×8 bit TCAM

TABLE I: Comparison with Different Methods

Properties	BCAM (RWOS Scheme)	TCAM (RWOS Scheme)	DUAL TCAM
Power (Micro Watts)	28	19	17
Number of transistors (For two CAM cells)	18	34	23

From the comparison table itself we can see the significant reduction in the number of transistors and power.

VI. CONCLUSION

In this work we proposed the dual TCAM architecture and simulated using tanner EDA tool. In the proposed architecture the comparison output from two CAM cells are used for the mask cell operation. In a conventional CAM word circuit each CAM cell needs one mask cell to work as a ternary CAM word circuit. We designed and simulated the TCAM and BCAM using the RWOS mechanism and also by using the proposed dual TCAM. A simulation result shows significant reduction in the power values and the number of transistors.

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