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CPS-PWM Based Cascaded H-Bridge MLI with Voltage Balancing Capability

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Abstract

This paper presents a specially designed cascaded H bridge multilevel inverter to increase the number of levels with reduced no of switches and best suited for medium voltage drive applications. An efficient approach to the voltage balancing issue is addressed by implementing third harmonic injection. To enhance the balanced distribution of power in each cell, Multi carrier phase shifted pulse width modulation switching scheme is employed. The midpoint capacitor voltage in unit cells is achieved with total harmonic injection method. This new topology of inverter offers less amount of THD when comparing with the conventional one. The validity of the proposed inverter is verified through MATLAB Simulink model and the scaled down prototype model is implemented in hardware.

Keywords*— Multilevel inverter, Cascaded H-bridge, Five-level inverter, multicarrier phase-shifted pulse-width modulation (CPS-PWM), Total harmonic distortion*

I. INTRODUCTION

In recent years, multilevel inverters have become an important technology and attaining more attention in a high-power conversion system. We can increase the number of levels by extending the unit cells. The research in this sector is an on going process for further improvement of its control techniques, balancing techniques and also to minimize the no of components (especially power semiconductor switches) used and the manufacturing cost.

With reduced no of switches, the output waveform obtained is in superior quality. Therefore the requirement of filters and system size is reduced so much. Switching losses also reduced to a greater extend as the no of switches are reduced. The topologies, such as single and three-phase neutral-point-clamped inverters, cascaded H-bridge inverter, and flying capacitor inverter, are well developed configurations in medium voltage drive applications. Different modulation strategies are available for producing the switching patterns for switches. For obtaining really good and high quality output, the perfect selection of modulation strategy is essential.Pulsewidth modulation (PWM) and space-vector modulation (SVM) are the most important modulation techniques for power converters. Handful of modulation strategies have been developed to generate a stepped switched waveform. Most of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical Shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition (APOD) PWM), or with horizontal displacements (phase-shifted carrier (CPS-PWM). Space-vector modulation (SVM) is also extended for the MLI operation, offers good harmonic performance .In this paper, cascaded multilevel inverter topology is focused. In the three conventional topologies, the cascaded H bridge MLI having more reliable and less no of components.

The cascaded MLI typically comprises several identical single phase H-bridge cells cascaded in series .By adding more number of stacks in cascaded manner we can raise the no of levels. There are two types. Symmetrical and unsymmetrical. If DC bus voltages are equal in all series connected power cells or else unsymmetrical. Therefore the designing of inverter is complex as in case of asymmetrical MLI. Therefore symmetrical type is more flexible design than the other. In this paper, the proposed topology is designed with symmetrical cascaded H-bridge MLI in which, the increase of voltage levels is possible without varying DC voltages.

The proposed configuration in this paper is a new topology that uses five switches in H-Bridge as a power cell that can produce a five level output instead of three level in the conventional inverter. For each unit the number of switches is lower, and for obtaining the same output quality, more no of cells are required. So the number of isolated dc sources and bulky transformers requirement increases. The proposed inverter is designed for medium voltage drive applications. This paper first describing the new topology of MLI configuration, PS-PWM strategy, analysis of output voltages and the total harmonic injection method for balancing the capacitor voltages, experimental

implementation and verification of results and finally the conclusion.

II.NEW MLI TOPOLOGY

In the general configuration of single cell Cascaded H bridge MLI, that uses 4 switches to produce three level output (V_{dc} ,-V_{dc}, 0).In our new topology, additionally a switch with bidirectional capability is connected across the first leg and the input side capacitor. The proposed configuration which uses 5 switches to produce five level output (+Vdc,+0.5Vdc,0,-0.5 Vdc,-1Vdc) is shown in fig 1 and the different open.

The switching sequence of our new topology is given in table I.

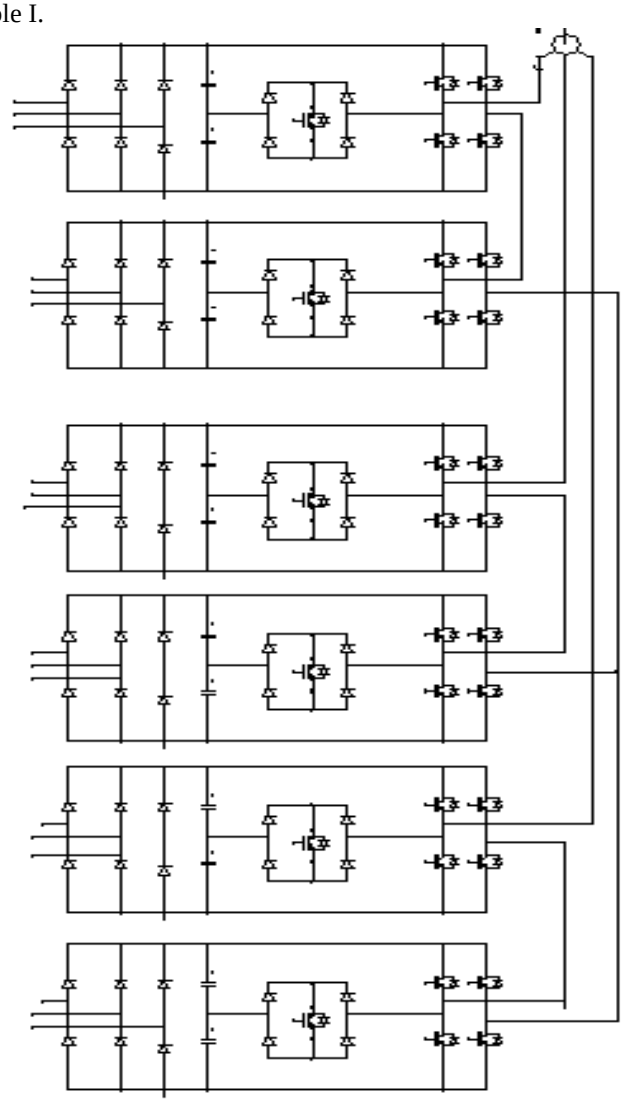


Fig.1.Proposed topology for medium drive applications

TABLE 1 Switching schemes for different operating modes

Q_1	Q_2	Q_3	Q_4	Q_5	V_{an}
0	1	0	0	1	V_{dc}
1	0	0	0	1	½ V_{dc}
0	0/1	1/0	0/1	1/0	0
1	0	0	1	0	-1/2 V
0	0	1	1	0	-V_{dc}

1-Switch on 0-Switch off

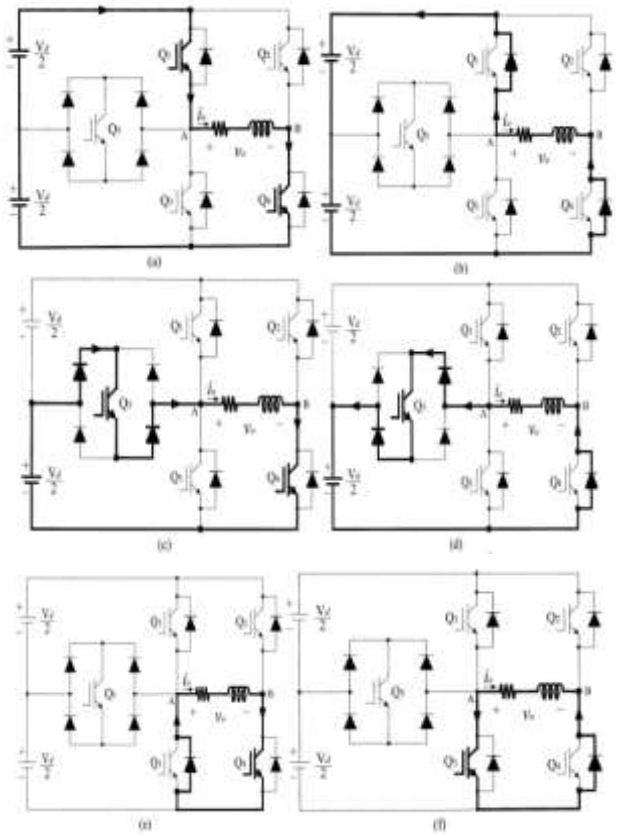


Fig.2.Proposed topology – different modes of operationposed inverter topology in represented in table 1.

III PWM MODULATION STRATEGY

The switching patterns for switches are generated through different kinds of PWM techniques. Phase-shifted carrier (PSC) pulse width modulation (PWM) in its conventional form is a good solution for multilevel inverters.In this topology, multi carrier phase shifted pulse width modulation (CPS-PWM) is used for generating the switching pulses. For signal generation in each cell, two voltage references and one carrier signals are used.Multi carrier means, two or more carrier signals are used .In this, triangular signals are used as carrier waveforms, with 1 KHz frequency. The frequency and magnitude are same for adjacent carriers. The phase shift angle between adjacent carriers are determined by using the formula,

$\Theta Cr,n=2\pi(n-1)/NC$, n=1 ,2...NC.

So for this topology, the triangular signals are phase shifted by 180 deg.The reference voltages are termed as Vref1, Vref2.

$V_{ref} = M \sin\omega t$

$V_{ref1} = V_{ref} = M \sin\omega t$

$V_{ref1} = |V_{ref}|$

$V_{ref2} = vref1 - 1/2$

Both references are identical but displaced by an offset equal to the carrier's amplitude which is ½.The amplitude and frequency of all carrier triangular carriers are the same and phase shifted by 180 deg according to this formula for this topology.

The detailed block diagram of CPS-PWM scheme is shown in figure 3. These two reference signals are identical to each other, but displaced by an offset voltage equal to magnitude of carrier's amplitude and the simulation of that signals are shown in fig 4.The respective switching sequences that are generated based on CPS-PWM scheme (for single cell/single phase) and the reference and carrier waveforms are shown in fig 5.The developed topology for single phase unit is shown in fig 6 .The generated output voltages shown in fig 6.

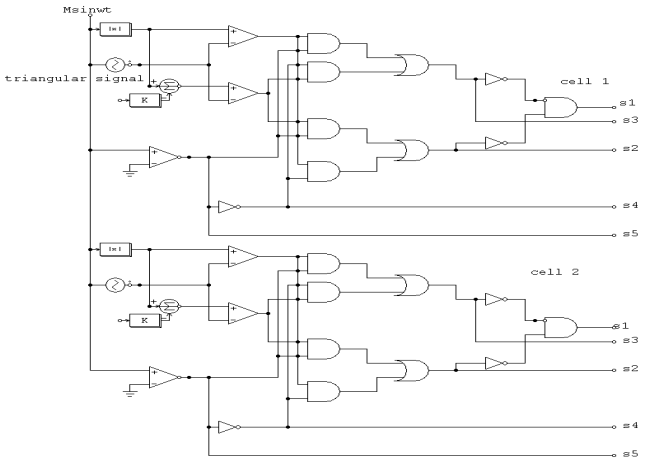


Fig. 3.Multi carrier phase shifted PWM signal generation for phase A.

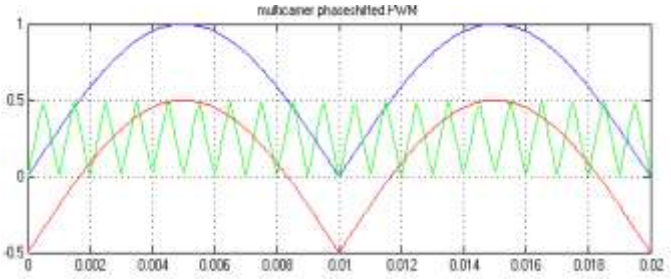


Fig.4.Reference and multi carrier phase shifted waveforms

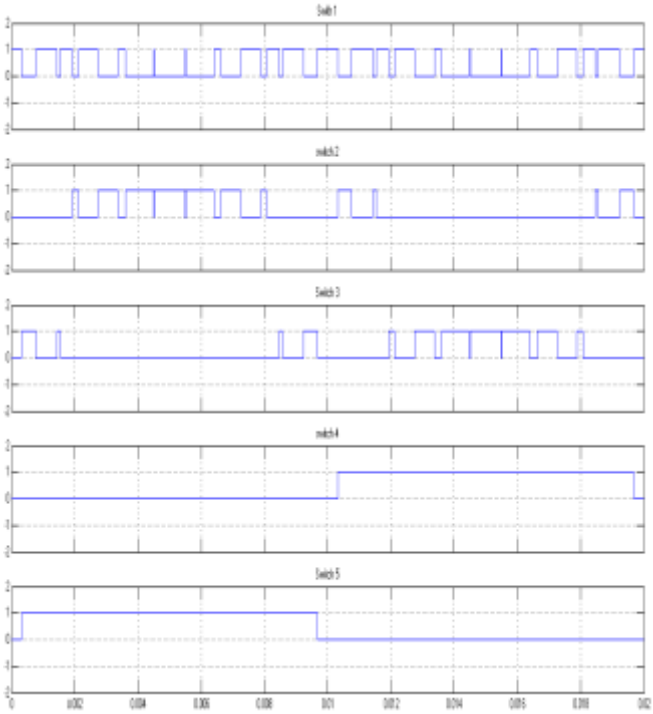


Fig.4.The simulated switching patterns for single cell unit

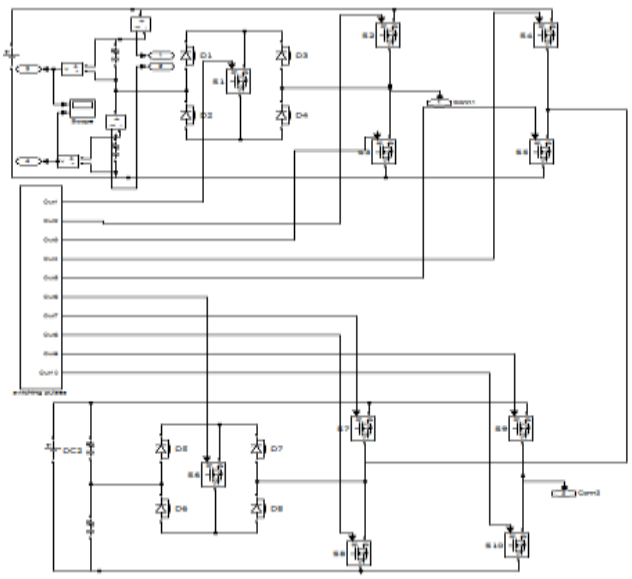
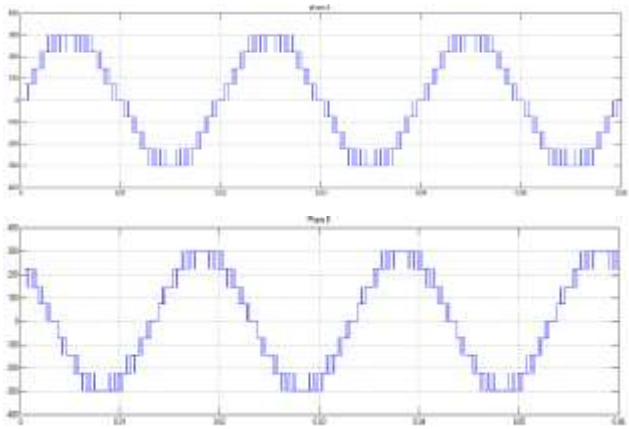


Fig.5.Matlab profile for proposed inverter topology for phase A



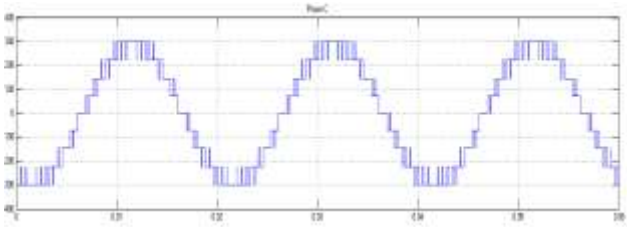


Fig.6.Output voltages for three phases

IV CAPACITOR VOLTAGE BALANCING SCHEME

Under the normal operating conditions, the midpoint voltage of capacitor is achieved in each cell by natural balancing itself. But, if any abnormal circumstances, such as transients, sudden large disturbances, the power cells become unbalanced.Therfore the average current drawn from capacitor midpoint is not equals to zero. Due to the issues, capacitor voltage away from ½ Vdc.This will lead to system instability and cause damage to the overall system.

Therefore for ensuring good and reliable operation of system, the proper balancing scheme must be incorporated. Switching state redundancy is avoided due to implementation of CPS-PWM scheme. Here the mechanism for voltage balancing is achieved via controlling the Iavg with third harmonic offset injection method. It uses two offset voltages represented by equations. Two offset voltages are used here, termed as Vic, dec and Vic, inc as shown in fig 7(a) and 7(b).

In each cell to regulate the midpoint capacitor voltage, combination of these two offset voltages are used. Using only one offset voltage in one fundamental period is not applicable. Since the capacitor current varies by the same amount in both the off cycles producing Iavg=0 & therefore resulting in no voltage balancing. The equations for voltage increment and decrement solutions are given below.

$$V_{ic,\,dec} = V_{offset,\,pk}\sin 3wt - V_{offset,\,dc} \quad \text{if } V_{offset,pk}\sin 3wt \geq 0$$
$$V_{offset,\,pk}\sin 3wt + V_{offset,\,dc} \quad \text{if } V_{offset,pk}\sin 3wt < 0 \quad (1)$$

$$V_{ic,\,inc} = V_{offset,\,pk}\sin 3wt + V_{offset,\,dc} \quad \text{if } V_{offset,pk}\sin 3wt \geq 0$$
$$V_{offset,\,pk}\sin 3wt - V_{offset,\,dc} \quad \text{if } V_{offset,pk}\sin 3wt < 0 \quad (2)$$

Voffset, pk and Voffset, dc are the variables for controlling amplitude and dc offset levels. If these offset values added with voltage reference, duty cycle is changed. The maximum condition of duty cycle is achieved when Vref is ½ and its minimum at Vref is 0 or 1.

$$V_{offset,inc} = \begin{cases} V_{ic,dec} & 0<wt<\pi \\ V_{ic,inc} & \pi<wt\leq 2\pi \end{cases} \quad (3)$$

$$V_{offset,dec} = \begin{cases} V_{ic,inc} & 0<wt<\pi \\ V_{ic,dec} & \pi<wt\leq 2\pi \end{cases} \quad (4)$$

Different offset voltages used in balancing technique results in positive or negative average current, depends upon the combination used. The developed Voffset,inc injection voltages with Vref and Vref*using MATLAB is shown in fig 8. Adding the offset voltage Vic,dec , forces the voltage reference away from ½., thus reducing the duty cycle and midpoint capacitor current .Whereas adding the offset voltage Vic,inc , forces the voltage reference close to ½, thus increasing the duty cycle and midpoint capacitor current .

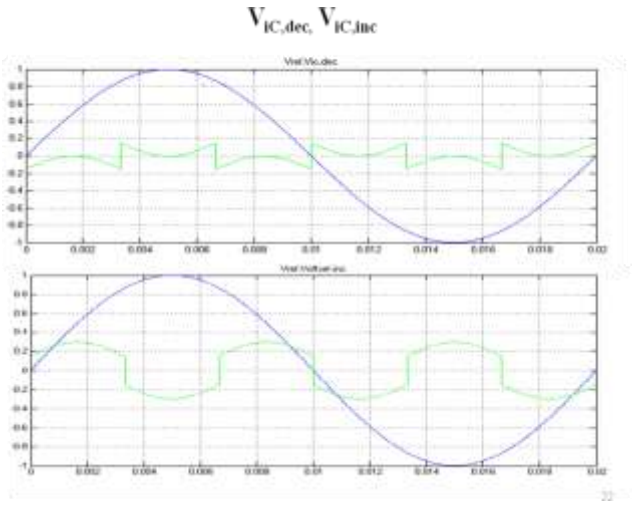


Fig.7 .Developed offset injection voltages in third harmonic injection scheme a)to decrease mid point capacitor current b)to increase midpoint capacitor current

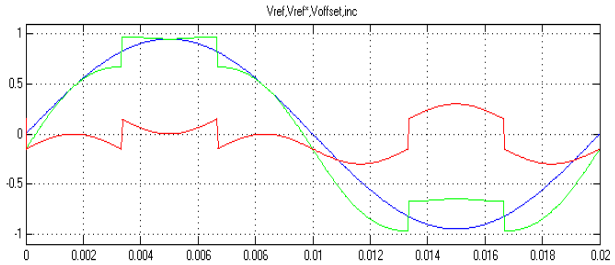


Fig. 8 .Proposed method for improving mid point capacitor volatge with voltage reference.

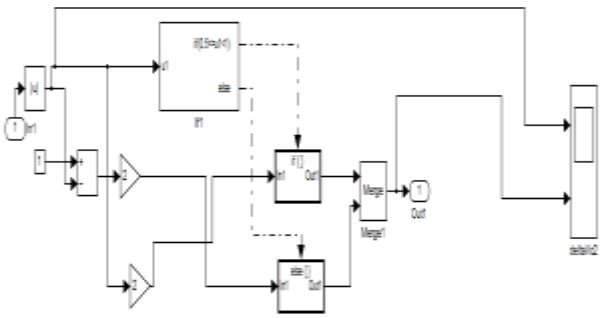


Fig. 9 .Profile for generating duty cycle.

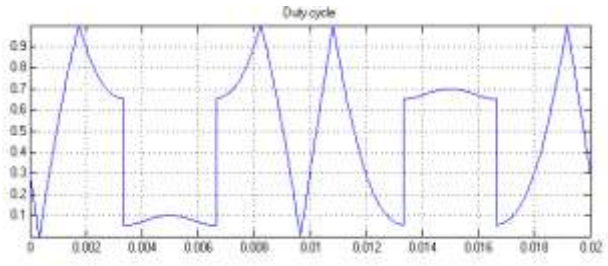


Fig.10.Duty cycle for midpoint capacitor voltage increment condition.

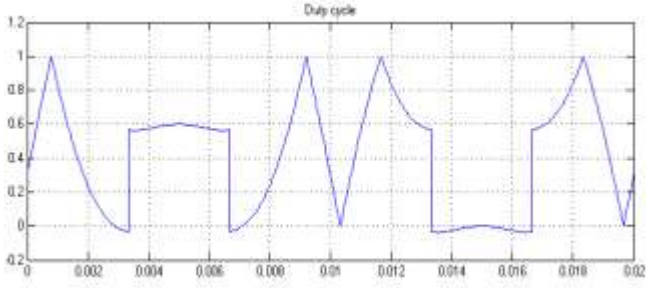


Fig.11 .Duty cycle for midpoint capacitor voltage decrement condition

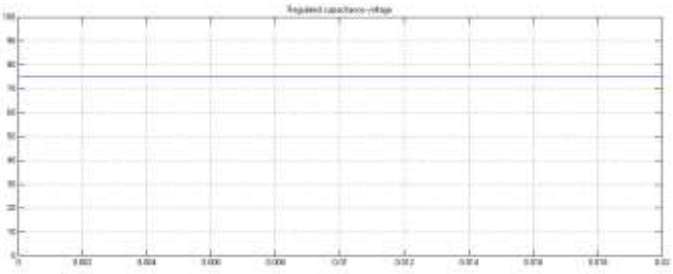


Fig.12..Regulated capacitor voltage after implemented with hysterisis controller

V. HARDWARE RESULTS

For verification, the scaled down prototype is developed to validate the simulation results. With the help of logical gate units, the required signals (carrier and reference) generated. Then the circuits designed for getting offset level between sine signals and phase shift between carrier signals. The table II shows the components list used in hardware development. The different output levels that are obtained in different levels of hardware development is shown in subsequent fig 13,fig 14,fig 15.

TABLE II LIST OF COMPONENTS USED IN PROTYPE MODEL

CIRCUIT	IC USED
Sine and triangular wave generator	Lm 324
Precision rectifier	Op-amp lm 324
Offset generation	Op-amp lm 324
And gate	Ic 7486
Or gate	Ic 7408
Not gate	Ic 7404
Mosfet	Irf 510
Diode	In 4001
Capacitor	Values as required
Opto coupler	MCT 2E
Resistor	Different values
Transformer	12 V
Battery	9 V

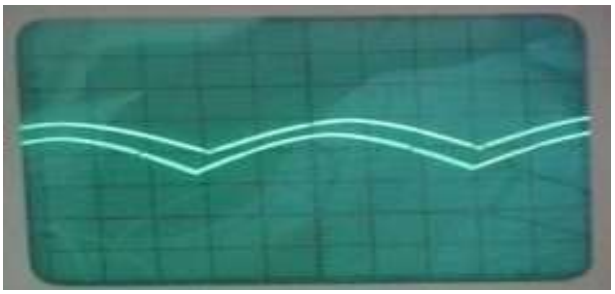


Fig.13 .Reference sine signals with 0.5 offset

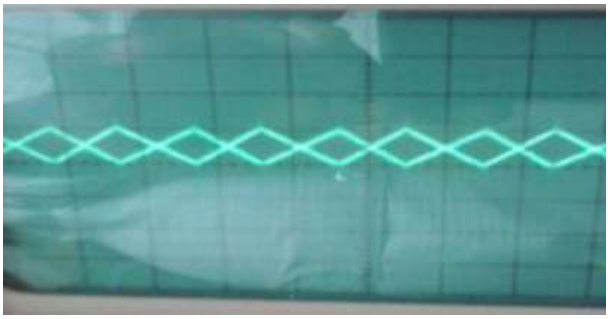


Fig.14 .Phase shifted triangular carrier signals with 1KHz frequency

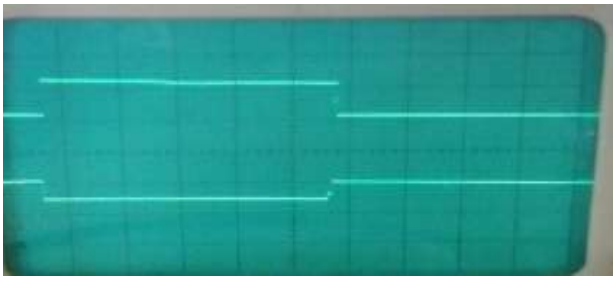


Fig.14.Switching pulses

Fig.15 .Multilevel inverter output

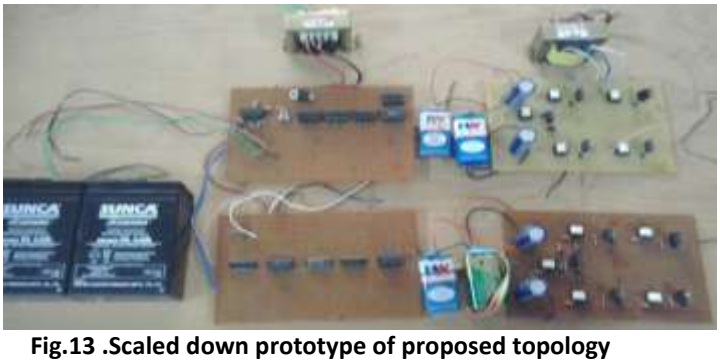


Fig.13 .Scaled down prototype of proposed topology

VI CONCLUSION

In this paper ,multi carrier phase shifted PWM based new topology of cascaded H-bridge system is developed.The

main problematic scenerio is the voltage balancing issues in source and load side.The capacitor volatge balancing method is developed based on third harmonic offset injection by implementing hysterisis controller The system is simulated in matlab and output voltage waveforms are obtained.By implementing small prototype of the system in hardware the results are validated.

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