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POWER QUALITY IMPROVEMENT USING 5-LEVEL FLYING CAPACITOR MULTILEVEL CONVERTER BASED DYNAMIC VOLTAGE RESTORER FOR VARIOUS FAULTS

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Abstract— This paper presents the application of dynamic voltage restorers (DVR) on power distribution systems for mitigation of voltage sags, harmonics and imbalances at sensitive loads. The dynamic voltage restorer (DVR) has become popular as a cost effective solution for the protection of sensitive loads from voltage sags and swells. It would be advantageous that a DVR could also be used to compensate any steady state load voltage harmonics, since this would increase the Power Quality. The DVR, which is based on a five-level flying-capacitor voltage Source converter (VSC), has been proved suitable for the task of compensating voltage disturbances. The performance of the DVR depends on control technique involved. This paper presents the control system based on the so-called repetitive control. Unlike other control schemes with a comparable range of applicability, only one controller is needed to cancel out all three disturbances simultaneously, while exhibiting good dynamic performance. Simulation results are presented to illustrate and understand the performances of DVR in supporting load voltage. To evaluate the quality of the load voltage during the operation of DVR, Total Harmonic Distortion (THD) is calculated.

Index Terms—Dynamic voltage restorer (DVR), flying capacitor multilevel converter, Total harmonic distortion (THD) power quality (PQ), repetitive control, voltage sags.

I. INTRODUCTION

POWER quality (PQ) has become an important issue over the past two decades due to the relentless integration of sensitive loads in electrical power systems, the disturbances introduced by nonlinear loads, and the rapid growth of renewable energy sources. Arguably, the most common PQ disturbance in a power system is voltage sags [1], but other disturbances, such as harmonic voltages and voltage imbalances, may also affect end user and utility equipment leading to production downtime and, in some cases, equipment terminal damage.

The dynamic voltage restorer (DVR) is one of the most efficient and economic devices to compensate voltage sags [2]. The DVR is basically a voltage-source converter in series with the ac grid via an interfacing transformer, conceived to mitigate voltage sags and swells [3]. For low-voltage applications, DVRs based on two-level converters are normally used [4] and, therefore, much of the published literature on DVRs deals with this kind of converter. Nevertheless, for higher power applications, power-electronic devices are usually connected to the Medium-voltage (MV) grid the use of two-level voltage converters becomes difficult to justify owing to the high voltages that the switches must block.

One solution is to use multilevel voltage-source converters which allow high power-handling capability with lower harmonic distortion and lower switching power losses than the two- level converter [5].

Among the different topologies of multilevel converters, the most popular are: neutral-point-clamped converters (NPC), flying-capacitor converters (FC), and cascaded-multimodal or H-bridge converters [6]. NPC converters require clamping diodes and are prone to voltage imbalances in their dc capacitors. The H-bridge converter limitations are the large number of individual inverters and the number of isolated dc voltage sources required. The main drawback of FC converters is that the number of capacitors increases with the number of levels in the output voltage. However, they offer more flexibility in the choice of switching combinations, allowing more control of the voltage balance in the dc capacitors. Furthermore, the extension of a converter to a higher level one, beyond three levels, is easier in FC converters than in NPC converters [7], which make the FC topology more attractive. A more comprehensive list of the merits and drawbacks of each topology can be found in [8], while a detailed description of multilevel-converter topologies as well as control strategies and applications can be found in [9]–[11].

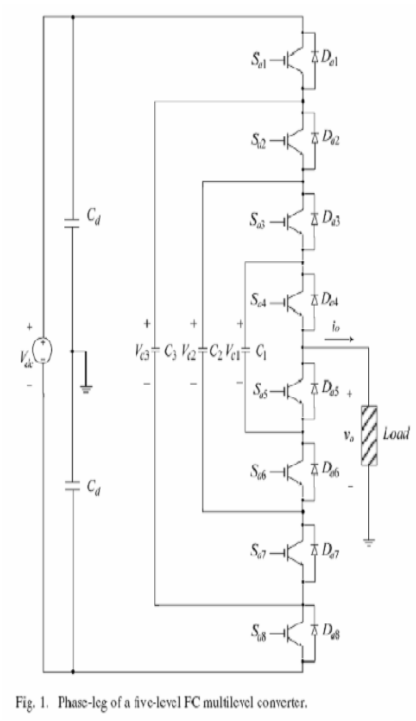
Research work has been reported on several DVR multilevel topologies [15]–[18], but so far, no work seems to have been published on DVR's by using FC multilevel converters.

This paper focuses on the design of a closed-loop

control system for a DVR by using a five-level flying capacitor converter, based on the so-called repetitive control. Repetitive control was originally applied to eliminate speed fluctuations in electric motors [19], [20], but it has also been successfully used in power-electronics applications, such as power-factor control in three-phase rectifiers and active-filter control.

The control system presented in this paper has a wide range of applicability. It is used in a DVR system to eliminate voltage sags, harmonic voltages, and voltage imbalances within a band- width. Unlike other control schemes with a comparable range of applicability, only one controller is needed to cancel out all three disturbances simultaneously, while exhibiting good dynamic performance. On the one hand, a closed-loop controller, which consists of a feedback of the load voltage and the repetitive controller, guarantees zero tracking error in steady state. On the other hand, the applied control strategy for the voltage balancing of the flying capacitors, along with a feed forward term of the grid voltage and a controller for the output voltage of the DVR filter, provides excellent transient response.

This paper is organized as follows. The model of a five-level flying-capacitor DVR is presented in Section II. The complete control-scheme structure is studied in Section III, including the three different control subsystems, namely, the filter output voltage controller, the repetitive control structure for the load voltage, and the flying-capacitor voltage regulator scheme, as well as the modulation method used to operate the multilevel converter. Simulation results obtained by implementing the control system and the five-level flying-capacitor DVR in MATLAB are presented in Section IV. Finally, the main conclusions are given in Section V.



v_o	Switching states			
	S_{a1}	S_{a2}	S_{a3}	S_{a4}
$+V_{dc}/2$	1	1	1	1
$+V_{dc}/4$	1	1	1	0
	1	1	0	1
	1	0	1	1
	0	1	1	1
0	1	1	0	0
	1	0	1	0
	0	1	1	0
	1	0	0	1
	0	1	0	1
	0	0	1	1
$-V_{dc}/4$	1	0	0	0
	0	1	0	0
	0	0	1	0
	0	0	0	1
$-V_{dc}/2$	0	0	0	0

Fig.1. Phase-leg of five-level FC multilevel converter and switching table.

II. CONFIGURATION OF THE DVR

A. Five-Level FC

Fig. 1 shows a phase leg of a five-level flying-capacitor converter, each phase leg has the same structure in three-phase converters, and the flying capacitors of one phase are independent from those of the other phases. One advantage of the flying capacitor multilevel converter topology is that the extension to converters with more than three levels is easier than in the neutral-point-clamped option (see [7] and [10]). Nevertheless, the number of capacitors becomes excessive as the number of levels increases.

Regarding the five-level topology shown in Fig. 1(b), the flying capacitorsC_1,C_2, and C_3 are charged to, $3V_{\rm dc}/4$, $V_{\rm dc}/2$ and $V_{\rm dc}/4$, respectively. Therefore, each switch must block only a voltage value equal to $V_{\rm dc}/4$, allowing the use of switches with lower-rated voltage compared with those used in a conventional two-level converter. There are several switching combinations for the same given output voltage, which is known as switching redundancy [7]. These switching combinations result in different charging or discharging states of the flying capacitors, which provide a degree of freedom for balancing the flying capacitor voltages. Comprehensive explanations of the switching combinations and their results can be found in [7] and [13].

B. DVR Connection System

The location of the DVR placed between the grid and the sensitive equipment is shown in Fig. 2. Different kinds of loads are assumed to be connected to the point of common coupling (PCC), such as linear loads (e.g., induction motors), nonlinear loads, and sensitive equipment. The DVR consists of a five-level flying-capacitor voltage-source converter and energy storage which provides the necessary voltage to the dc link. The series connection of the DVR is achieved by means of a coupling transformer. A passive filter has been used to filter out the high harmonics generated by the PWM process (see, for example, [16]).

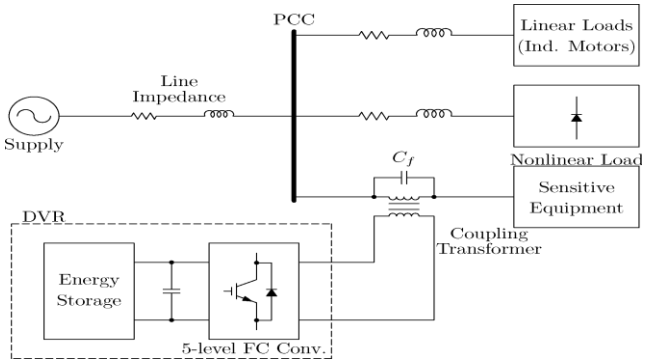


Fig. 2. Basic scheme of the system configuration with the DVR.

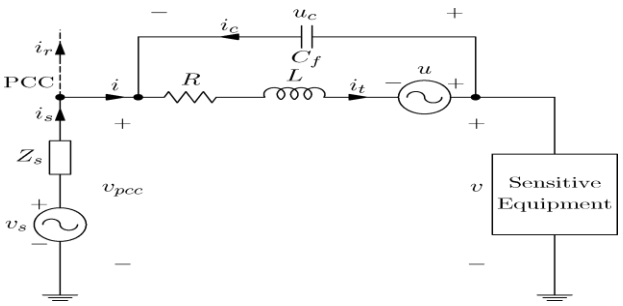


Fig. 3. Equivalent circuit for the DVR connection system.

The equivalent circuit for the one-line system in Fig. 2 is depicted in Fig. 3, where v_s is the supply voltage, Z_s models the line impedance, i_s is the current injected by the supply, which splits at the PCC into the current flowing through the sensitive equipment *i* (this current is divided into the current through the coupling transformer i_t and the current through the filter capacitor i_c), and the current injected into the loads i_r. The voltage V_{pcc} is the measured voltage at the PCC, u stands for the DVR voltage which has been modeled as an ideal voltage source, the parameters R and L are the resistance and the leakage inductance, respectively, of the coupling trans- former whereas C_f is the capacitor used together with the coupling-transformer leakage inductance to filter out the high-frequency harmonics. Finally, u_c and v are the voltages across the filter capacitor and the measured voltage across the sensitive equipment, respectively.

The equation of the sensitive-equipment voltage v can be written as

$$v(t) = v_{\text{pcc}}(t) + u_c(t) \qquad (1)$$

with the following state-variable model for the coupling trans- former and the capacitor set:

$$\frac{d}{dt}\begin{bmatrix} i_t(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_f} & 0 \end{bmatrix}\begin{bmatrix} i_t(t) \\ u_c(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C_f} \end{bmatrix}\begin{bmatrix} u(t) \\ i(t) \end{bmatrix} \qquad (2)$$

where the state variables are $i_t(t)$ and $u_c(t)$, the control input is $u(t)$ and $i(t)$ is a disturbance input.

III. CONTROL SYSTEM AND MODULATION STRATEGY

A. Control System for the Output Voltage of the LC Filter

System (2) is a second-order filter with natural frequency $\omega_n = 1/\sqrt{LC_f}$ and damping coefficient $\xi = R/2.\sqrt{C_f/L}$. This filter exhibits a large resonance since the resistance R usually has a very small value and, therefore, the damping coefficient is also very small. To overcome this problem, closed-loop control of the filter output voltage is required.

A proportional state-feedback controller plus a feed forward term are proposed for (2), with the following structure:

$$u(t) = -\overbrace{\begin{bmatrix} k_i & k_u \end{bmatrix}}^{\mathbf{K}}\begin{bmatrix} i_t(t) \\ u_c(t) \end{bmatrix} + u_c^*(t) + h(i(t)) \qquad (3)$$

Where K is the feedback-gain matrix, $u_c^*(t)$ is the reference value, and the feed forward term $h(i(t))$ is a function $i(t)$ of which will be calculated to cancel out the effect of the disturbance $i(t)$ on the voltage $u_c(t)$.

The gain matrix here has been designed in order to obtain a second-order closed-loop system with natural frequency $\omega_c = 1/\sqrt{LC_f}$ and damping coefficient ξ_c =1, which means that the closed-loop system has two identical real poles equal to $s_{1,2} = -1/\sqrt{LC_f}$ and the time response will not exhibit any over shoot. Furthermore, as will be shown in Section IV, this design implies that the gain is k_u equal to zero and, hence, there is no need to feed back the capacitor voltage.

In order to obtain the function $h(i(t))$, the Laplace transform is applied to (2) and (3), yielding

$$U_c(s) = \frac{U_c^*(s) + H(s)I(s) - (Ls + R + k_i)\,I(s)}{LC_f s^2 + C_f(R + k_i)s + 1} \qquad (4)$$

and H(s) is chosen so that the term I(s) has no effect in the capacitor voltage, which implies that
$H(s) = Ls + R + k_i$ and $h(i(t)) = Ldi/dt + (R + k_i)i(t)$.

The structure of this control scheme can be seen in Fig. 4.

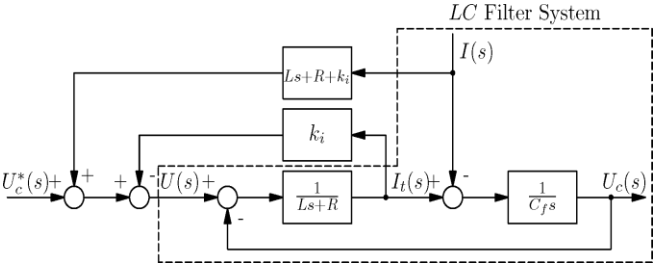


Fig. 4. Filter-output-voltage control scheme.

B. Load-Voltage Control Scheme

The control system developed in the previous section requires further development since it may be not able to guarantee a perfect compensation of the load voltage for every situation. In order to counteract possible disturbances which can affect the load voltage, an outer closed-loop control system is required. The control scheme proposed in this paper uses a feed forward term of the voltage at the PCC to improve the transient response and a feedback term of the load voltage to guarantee zero error in steady state against disturbances.

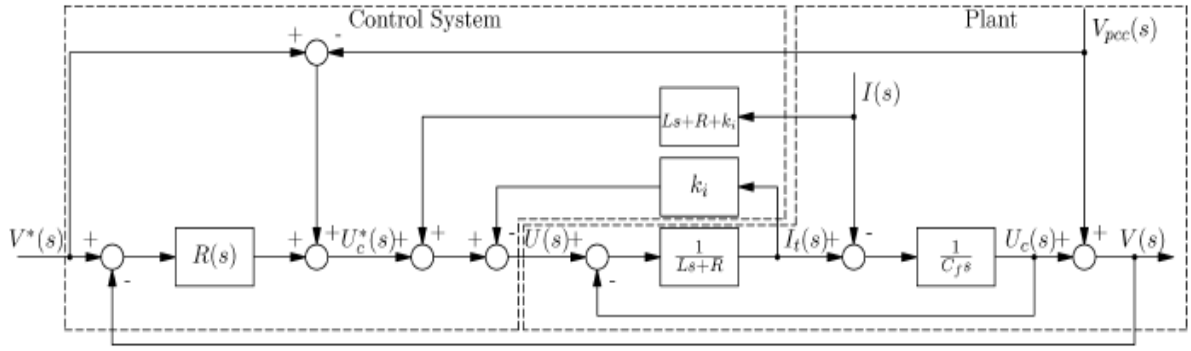


Fig. 5. Load-voltage closed-loop control scheme including the regulator for the filter output voltage

Fig. 5 shows the complete continuous-time control system for the load voltage. Assuming that there are no modeling errors and neglecting any delay in the control system, the DVR can be seen as an ideal linear amplifier (see [24]). The coupling transformer, together with the capacitor C_f, has been included in the figure as well as the detailed control system for the filter output voltage. The input *V*(S)* is the set point for the load voltage V(s), U(s) is the DVR voltage, and $V_{pcc}(s)$ is the supply voltage.

Recalling that

$$U_c(s) = \frac{U_c^*(s)}{LC_f s^2 + C_f(R+k_i)s + 1} = G_u(s)U_c^*(s) \quad (5)$$

Then, the load voltage can be calculated as

$$V(s) = F(s)V^*(s) + F_w(s)V_{pcc}(s) \quad (6)$$

With

$$F(s) = \frac{[1+R(s)]G_u(s)}{1+R(s)G_u(s)} \quad (7)$$

$$F_w(s) = \frac{1-G_u(s)}{1+R(s)G_u(s)} \quad (8)$$

In order to illustrate the main features of the repetitive control, a basic transfer function of the controller R(s) is proposed as

$$R(s) = \frac{1}{1-e^{-2\pi/\omega_1 s}} \quad (9)$$

Where w_1 is the fundamental frequency of the supply voltage.

C. Phase-Shifted Pulse width Modulation

Several modulation methods have been used in multilevel converters according to the switching frequency [10]. In normal conditions, a selective harmonic elimination-pulse width modulation (SHE-PWM) is used, which allows eliminating certain low-order harmonics by choosing the switching instants and provides a low switching power loss due to the low equivalent switching frequency. This kind of modulation produces triple harmonics in the converter output voltage which are eliminated by means of the delta or floating star-connected transformer secondary windings. Nonetheless, for asymmetrical faults, the converter is required to generate unbalanced three-phase voltages and large triple harmonics would appear on the grid side as they could not be completely cancelled out by the transformer. For those situations, the solution proposed is to change from the SHE-PWM to the phase-shifted PWM, which does not produces low-order harmonic voltages, although it exhibits a higher power loss than the SHE-PWM due to the higher switching frequency of the converter. In this paper, the well-known phase-shifted PWM method has been used since its implementation is simple and provides a certain degree of flying-capacitor voltage balance [7].

In a scheme with an n-level converter, n-1 triangular carriers with frequency f_c have to be compared with a common sinusoidal modulating signal with frequency f_m [27]. It is assumed that the carrier frequency is high enough to consider the modulating signal as a constant value in a period of the carrier. The switching instants are determined by the intersection between the modulating signal and the different carriers. A shifting phase of 2∏/(n-1) is introduced in each carrier, which ensures an effective switching frequency of (n-1) f_c and improves the total harmonic distortion of the output voltage, while the frequency modulation ratio yields $m_f = (n-1)\, f_c / f_m$. For the three-phase case, three modulating signals with a shifting phase of 120 are used. There are four regions in terms of the value of *m* shown in Fig. 6(a)–(d), respectively. The control switching signals g_1, g_2, g_3, and g_4 for the main switches of S_{a1} to S_{a2} as well as switching states and associated capacitor charging and discharging modes are also shown in Fig. 6.

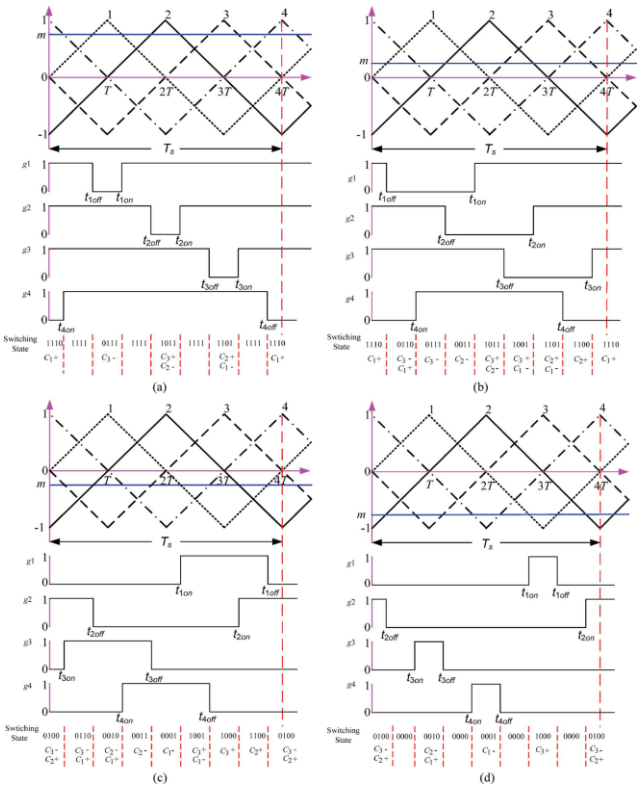


Fig. 6. Control signals for different modulating reference values. (a) 0.5 pu.<m <1.0 pu.; (b) 0 pu.<m < 0.5 pu.; (c) -0.5 pu. <m <0pu.; (d) -1 pu. < m <-0.5 pu

IV. STUDY CASE

In order to verify the proposed control algorithm in a five-level flying-capacitor DVR, the test system depicted in Fig. 2 has been implemented in MATLAB. The test system is comprised of a three-phase voltage source of 11 kV at 50 Hz which feeds a linear load, a nonlinear load, and a sensitive load: the linear load is a three-phase squirrel-cage induction motor of 1350 kW, the nonlinear load consists of an uncontrolled three-phase rectifier with a capacitive filter in the dc side of the rectifier in parallel with an inductive-resistive load. The sensitive load is made up of a 120-kW three-phase squirrel-cage induction motor and an inductive-resistive load of 300 kVA and power factor 0.92.

The five-level flying-capacitor converter is connected to the PCC by means of three single-phase coupling transformers of 160 kVA, with unity turns ratio and a star-connected secondary winding. The dc voltage of the multilevel converter is 8 kV. The output filter cutoff frequency was set at f_c = 2 kHz with a capacitor C_f = 1.05μF. Finally, the value of each flying capacitor is C_1=C_2=C_3=250μF [see Fig. 1(b)], while the switching frequency was set at f_{sw}=1650 Hz for each switch. For the five-level converter studied here (n=5), the effective switching frequency is (n-1)f_{sw}=6600 Hz. The main parameters of the test system are summarized in Table I.

TABLE I
PARAMETERS OF THE TEST SYSTEM

Supply voltage		11kv
Line impedance		R_s = 60mΩ L_s = 3mH
Linear load	Connection inductance	L_1 = 0.5μH
	Induction motor	P_m =1350kw
Non linear load	Connection inductance	L_2 = 0.5μH
	Capacitor	C_{dc}= 50μF
	Resistance	R_{dc} = 120Ω
	Inductance	L_{dc} = 0.6H
Sensitive load	RL load	S= 300KVA
	Induction motor	P_m= 120Kw
Filter	Capacitor	C_f =1.05μF
	Cut-off frequency	f_c= 2KHz
Flying capacitors		250 μF

Simulation Results

The test system shown in Fig. 2 is used to carry out a comprehensive simulation scenario where the multilevel DVR and its control system show their worth. The following sequence of events is assumed to take place: 1) the nonlinear load is connected at time t = 0s and the charging of the flying capacitors also starts at this point in time, a process that is fully completed at time t = 0.6s; 2) At this point, the whole control system is activated and the DVR is connected to the grid together with the inductive-resistive load (sensitive load); 3) in the time period 0.7–1.1s, induction motor 1 is assumed to be connected with a constant rotor speed of 0.98 p.u.; 4) from t = 0.8s to 1.1s, a two-phase-to-ground short-circuit fault is applied at the PCC via a 1.8-resistor; 5) a second induction motor comes into operation right through the fault period, at t = 0.9 s until the end of the simulation time; 6) the nonlinear load is disconnected at 1.3s and, at this point in time, a second short-circuit fault applied at the PCC takes place; this time, there is a three-phase-to-ground fault, with a duration of 200ms. The total simulation time is 1.6s.

Fig. 7(a) and (b) shows the rms voltages of phase A at the point where the sensitive load is connected and at the PCC, respectively. The two-phase-to-ground short-circuit fault produces a 30% voltage sag in the two affected phases in the time period 0.8–1.1 s. Also notice the minor voltage dip caused by induction motor 1 in the period 0.7–0.8 s. It is clear that in the period 0.8–1.1 s, the induction motor contributes to some minor extent to the voltage sag but, by and large, the major contributor to the sag is the short-circuit fault. It should be noticed that the 30% is not shown quite accurately in Fig. 9(b) since this is an unbalanced fault. At the time of fault clearing, 1.1 s, and before the second short-circuit fault takes place 1.3 s, no voltage sags are present at the PCC, and the only anomalous phenomenon is the harmonic voltages due to the nonlinear load. The three-phase-to-ground fault at 1.3s Produces 30% voltage sag since this is a symmetrical fault. As shown in Fig. 9(a), the

control system and DVR are able to maintain the rms voltage supply to the sensitive equipment close to 11 kV, notwithstanding the voltage fluctuations at the PCC caused by the various disturbances previously discussed.

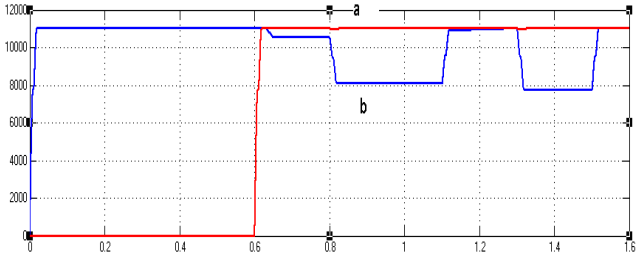


Fig. 7. rms voltage. (a) Across the sensitive equipment. (b) At the PCC.

Fig. 8(a) and (b) shows the results obtained when the linear load (induction motor 1) and the nonlinear load are connected. Fig. 8(a) plots the line-to-line voltage at the PCC (V_{pccab}): it can be seen that the waveform is distorted, owing to the harmonic currents that the rectifier produces. Also, the total current provided to the linear load, the rectifier, and the sensitive equipment causes a voltage drop at the PCC. The voltage at PCC has an rms value of 10.52 kV (95.6% of 11 kV) for the fundamental frequency component, while the voltage total harmonic distortion is THD=8.48%. However, Fig. 10(b) shows that the line-to-line voltage across the sensitive equipment is relatively sinusoidal: the fundamental-frequency component has an rms value of 11 kV, with a voltage total harmonic distortion THD=1.70%. The control system and the multilevel DVR are not only able to compensate the voltage drop at the PCC, but also cancel out the harmonic voltages caused by the rectifier.

Fig. 9(a) and (b) gives the harmonic spectrums of the line-to-line voltages at the PCC and across the sensitive equipment, respectively. It can be appreciated that in the frequency interval 0Hz<f<2000Hz, practically all harmonics have been removed from the voltage across the sensitive equipment (recall that the control system of the filter output voltage achieves a closed-loop system with a cutoff frequency of 2 kHz).

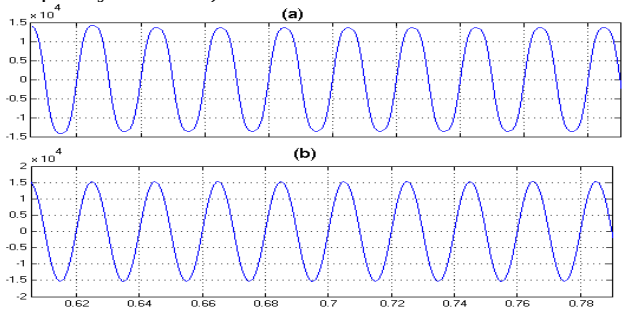


Fig. 8. Line-to-line voltage (0.6<t<0.8 s) (a) at the PCC and (b) across the sensitive equipment.

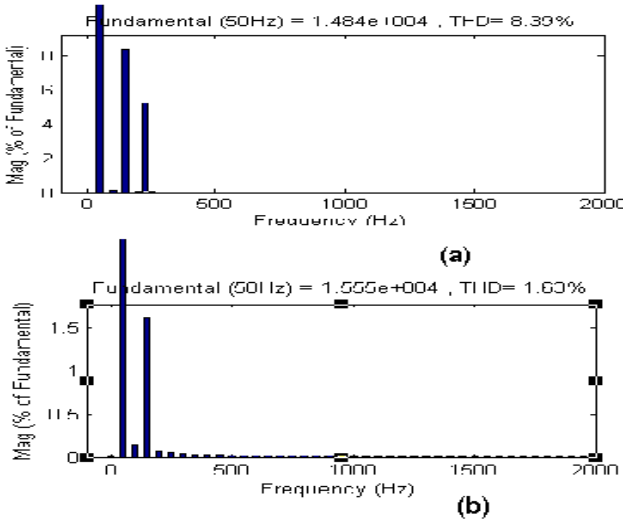


Fig. 9. Detail of the spectrum of the line-to-line voltage (a) at the PCC and (b) across the sensitive equipment.

At 0.8 s, the asymmetrical fault involving phases A-C and ground is applied at the PCC; hence, the three line-to-line voltages have been plotted to assess the DVR performance more fully. Fig. 10 shows the unbalanced line-to-line voltages at the PCC: the three voltage waveforms have different amplitudes and they also contain harmonic voltages caused by the rectifier.

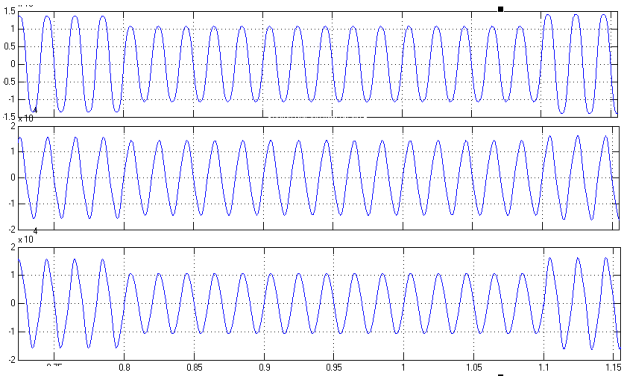


Fig. 10 Line-to-line voltages at the PCC in kilovolts (a) Vpccab , (b) Vpccbc, and (c) Vpccca . (0.7<t<1.2)

The rms values of the fundamental frequency components are V_{pccab} = 8.05 kV, V_{pccbc} = 9.87 kV, and V_{pccca}= 7.52 kV. The voltage total harmonic distortions are THD_{ab} = 6.25%, THD_{bc} = 5.13%, and THD_{ca} = 2.03%.

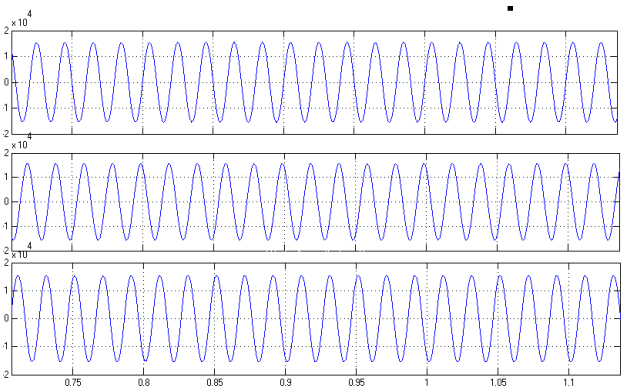


Fig. 11 Line-to-line voltages across the sensitive equipment in kilovolts (a) Vab , (b) Vbc, and (c) Vca . (0.7<t<1.2)

The voltage across the sensitive equipment is plotted in Fig. 11. The DVR, operated by the control system, compensates the unbalanced voltages with a fast transient response owing to the Feed forward term of the sensitive-equipment voltage, while the repetitive control ensures zero-tracking error in steady state. The rms values of the fundamental-frequency components are equal to 11 kV for the three line-to-line voltages across the sensitive load, while the voltage total harmonic distortions are THD_{ab} = 0.90%, THD_{bc} = 1.02% and THD_{ca} = 0.91%.

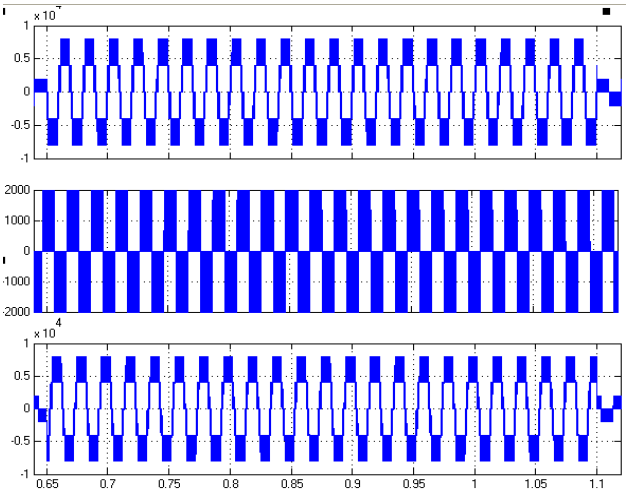


Fig. 12. Multilevel-converter output voltages in kilovolts (0.65<t< 1.14s)

Fig. 12 shows the three output voltages of the five-level converter with reference to the point 0 (see Fig. 1). Since phase B is not involved in the fault, the DVR injects a lower voltage value in this phase than in the other two phases. Therefore, the voltage V_{bo} has several unused, unlike V_{ao},V_{co} the voltages and , which all use five levels.

The scenario in the time interval 1.3 s is similar to the one depicted in Figs. 8 and 9, but with only the rectifier and sensitive equipment connected to the PCC.

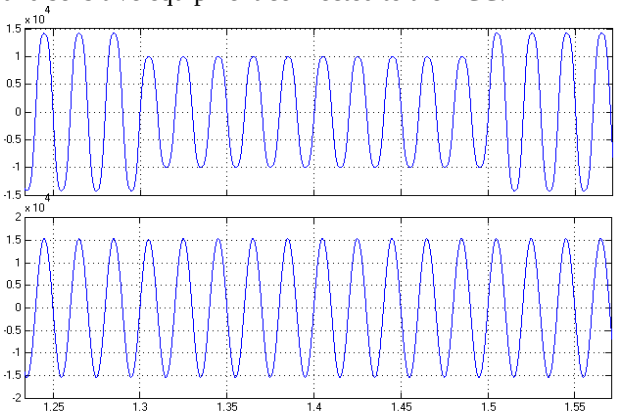


Fig. 13. Line-to-line voltage (1.26s < t < 1.54 s) (a) at the PCC and (b) across the sensitive equipment

At 1.3 s, the nonlinear load is disconnected from the PCC. Simultaneously, the three-phase-to-ground fault is applied via a resistance of 1.8 Ω. Fig. 13(a) and (b) shows the line-to-line voltage at the PCC and across the sensitive load. Since the fault is symmetrical, only one of the line-to-line voltages has been plotted for each case. The rms value of the line-to-line voltage at the PCC is 7.7 kV (70% of its rated value) with no voltage distortion. The transient response of the sensitive-load voltage can be seen in Fig. 13(b): the DVR cancels out the voltage sag caused by the fault with fast performance. The Fourier analysis shows that the fundamental-frequency component of the line-to line voltage is 11 kV and that the waveform has a voltage total harmonic distortion 0.91%.

V. CONCLUSION

Nowadays, reliability and quality of electric power is one of the most discuss topics in power industry, there are numerous types of power quality issues and power problems Among them, two power quality problems have been identified to be of major concern to the customers are voltage sags and harmonics, but this project is focusing on voltage sags. Voltage sags are huge problems for many industries, and it is probably the most pressing power quality problem today.

In this paper DVR based on a five level flying-capacitor converter operated by a repetitive-control scheme. This control structure simultaneously cancels out voltage sags, voltage imbalances, and voltage harmonics other than high-frequency switching harmonics. The control system is split into three subsystems: the first one works to eliminate the resonance peak of the filter used in the converter output voltage; while the second one is the repetitive control, which ensures a fast transient response and zero-tracking error in steady-state for any sinusoidal reference and for any sinusoidal disturbance whose frequencies are an integer multiple of the fundamental frequency. Finally, the third subsystem maintains constant, balanced voltages in the flying capacitors.

The control system, together with the DVR, has been implemented in MATLAB Comprehensive simulation results using an MV test system show the DVR's excellent performance and the control system in order to protect sensitive equipment from PQ disturbances.

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