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Design and Implementation of a Backtracking Wormhole Switch using MARX units for Mesh Topology

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Abstract: ***Network-on-Chip (NoC) is supposed to be adopted by the designers as a substitute for buses and dedicated wire interconnection schemes in future complex SoCs. Compact and power efficient design of basic routing element (router or switch) is an important part of the NoC design. Several switch implementations for different topologies of NoCs are proposed. This project presents the design of Backtracking Wormhole Switch. The switching mechanism used is circuit-switching approach. The proposed circuit-switched router, based on a Backtracking probing path setup, operates with new MARX units, and allows for efficient low latency Wormhole switch implementation. The switch can support a dead- and live-lock free dynamic path-setup scheme. The backtracked routing Network-on-Chip provides guaranteed and energy-efficient data transfer. The backtracking wormhole switch architecture is considered for use under a mesh/torus topology because of its good path diversity.***

Keywords: Network-on-chip, Backtracking, Wormhole switch, MARX.

1. Introduction

As the complexity of SoCs increases, the network-on-chip is being adopted as a solution for integrating numerous on-chip components. NoC is a new method for on chip communication to solve the problem that challenges the system on chip. One of the most difficult tasks in NoC design is guaranteeing throughput or providing a quality-of-service mechanism of the traffic offered by the on-chip components, particularly with the very limited budget of the on-chip resources. The parameters such as data loss, data rate and delay decide the performance metrics of on-chip networks.

The circuit-switching path set up scheme provides guaranteed throughput by eliminating the risk of data dropping. On establishing a desired path from source to destination, data is forwarded with the maximum utilization of the bandwidth along the dedicated links with low delay, no data jitter, and in a lossless manner i.e., without data dropping due to there being no collisions among the data streams.

The NoC switches should be reliable, cost-effective providing high speed and requires appropriate contention solving schemes when same destination port is requested by multiple packets from different sources. A pipeline circuit-switched router design is proposed, which is termed as backtracking wormhole router or BW switch, to meet the guaranteed throughput requirements.

2. Motivation

The switches are the basic building blocks of such interconnection networks and their design critically affects the performance of the whole system. So far, innovation in switch design relied only on the characteristics of the main building blocks of the switch, such as the buffers, the arbiters and the crossbar's without any further modifications.

In this proposed switch design technique an attempt is made to re-organize them in a more efficient way, by explicitly targeting the design that can handle concurrently arbitration and multiplexing and can be parameterized with the number of inputs, the data width, and the priority selection policy. With the proposed switch architecture, switch allocation, employs standard round-robin policy with significant network-throughput benefits, and switch traversal can be performed simultaneously in the same cycle, offering delay efficient implementation of the wormhole switch.

To extract the combined operation of arbitration and multiplexing, irrespective of the complexity of the priority

selection policy, aiming at the design of efficient high-throughput and low-latency switches, a new structure called Merged ARbiter and multipleXer called MARX that merges efficiently the functionality of the arbiter and the multiplexer is utilized.

In this way, the tasks of SA and ST of the original WH switch are merged to a new stage called switch allocation and traversal, which is directly implemented by the new MARX units and allows for efficient low latency WH switch implementation.

In the proposed pipelined circuit-switched router, flits do not immediately follow the header into the network. It is first observed that whether the setup header can flexibly backtrack under backtracking routing standards to search for an available alternative path rather than wait or queue until the blocking channels become available. Such a backtracking-based path-setup scheme can be implemented easily without the need of additional control network.

The above observations are the motivations for using both backtracking and MARX based wormhole switches for the proposed BW circuit-switched router, to meet on-chip hard guaranteed throughput.

3. MARX based WH Switches

The design of wormhole (WH) switches that employ the proposed dynamic priority MARX units is as depicted below.

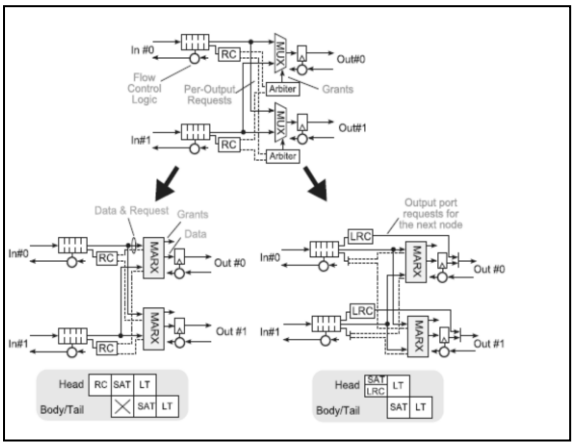

Figure 1: MARX Based Switch Architecture

The output stage of WH switch that uses separate arbiters and multiplexers can evolve to a MARX-based switch, with routing computation (RC) either preceding (left subfigure), or performed in parallel to MARX (by employing LRC - right subfigure).

The arbiter multiplexer pairs at each output are directly replaced by the corresponding dynamic priority MARX units. In this way, the tasks of SA and ST of the original WH switch are merged to a new stage called switch allocation and traversal (SAT), which is directly implemented by the new MARX units and allows for efficient low latency WH switch implementation.

3.1 MARX for Round Robin Arbitration

The basic idea of merging arbitration and multiplexing in a new combined sorting-based operation can be naturally extended to round-robin and more complex weight-based selection policies.

3.1.1 MARX with Static Priority

Round-robin arbitration logic scans the input requests in a cyclic manner beginning from the position that has the highest priority. The priority vector P that indexes the request with the highest priority, consists of N bits. For example, in the case of an 8-port round-robin arbiter, if position 3 has the highest priority, vector P is equal to 11111000 (LSB-to-MSB).

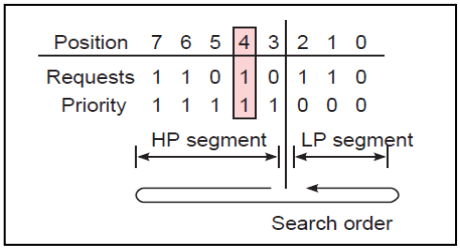

Figure 2: The priority vector separates the input requests to an HP and an LP segment.

The priority is diminishing in a cyclic manner to positions 4, 5, 6, 7, 0, 1, 2, giving to input 2 the lowest priority to win a grant. If after scanning all inputs the circuit does not find an active request, it de-asserts the AG (Any Grant) signal.

As shown in the example of Figure 2 the priority vector splits the input requests in two segments. The high-priority (HP) segment consists of the requests that belong to high priority positions, where Pi=1, while the requests, which are placed in positions with Pi=0, belong to the low-priority (LP) segment. The operation of the round-robin arbiter is to give a grant to the first active request (scanning right to left) of the HP segment and, if not finding any, to close the cycle by giving a grant to the first active request of the LP segment.

But the main drawback is the requests with lowest priorities (LP segment) have to wait for grant until all the requests in the HP segment are served. This leads to starvation of the lower priority requests. Therefore in order to overcome this drawback the cyclic search of the round robin arbiter is avoided and the input requests and the priority vector are treated in a completely different way which serves as the baseline for the implementation of the MARX units supporting dynamic priorities.

3.1.2 MARX with Dynamic Priority

In the static priority MARX the first request of the HP segment wins in a round-robin order, while in the dynamic priority MARX, the first request of the LP segment, scanning from right to left according to round robin policy, wins. At each node of the tree, the L and R flags denote if the winning symbol belongs to the left or the right sub tree, respectively.

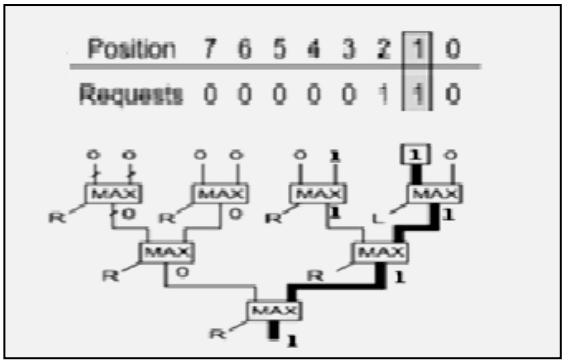

Figure 3: The round-robin arbiter selects the rightmost maximum symbol without any cyclic-priority transfer, the first request of the LP segment is granted.

The new dynamic priority MARX units employ a fair, simple and hence highly efficient round robin arbitration scheme. A binary tree can be utilized for selecting the maximum symbol. Therefore, the introduction of the dynamic priority round robin arbiter practically transforms the cyclic round-robin arbitration to an acyclic sorting operation, as in the case of a fixed priority arbiter. Figure 4 represents the sorting based binary tree with N-1 comparison nodes.

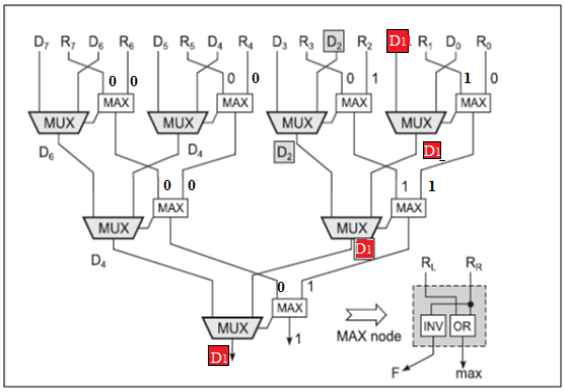

Figure 4: The round-robin arbiter selects the rightmost maximum symbol.

It employs round robin arbiter with dynamic priority similar in operation to the static priority MARX architecture but with the main difference being the removal of the cyclic search arbitration and adopting the acyclic sorting based technique.

3.3 Wormhole Switching

3.3.1 Flitization and Deflitization

Wormhole switching is by far an efficient and reliable flow control mechanism that allocates buffers and i/o links to flits instead of packets. A packet is fragmented into one or more flits. This process is called as decomposition or flitization.

A flit is the smallest unit, on which flow control is performed. It advances to the next switch only when buffering in the next switch is available to hold the flit. This results in the pipelined flow of flits in a packet as shown below.

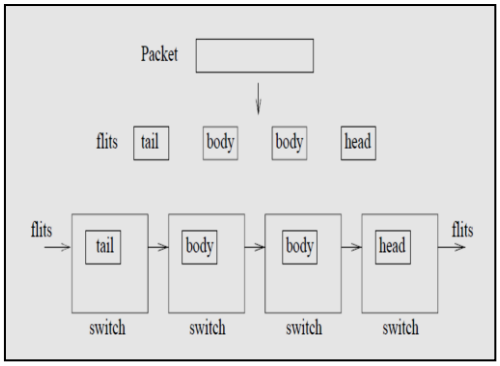

Figure 5: Flits delivered in a pipeline

As illustrated in Figure 5 a packet is segmented into four flits, with one head flit with source and destination address, leading two body flits which carry the original data and one tail flit, all transmitted in pipeline via switches, providing greater throughput.

If a packet is blocked, other packets can still traverse the i/o link via other links by finding an alternate path under suitable backtracking routing standards, leading to higher throughput. This provides better performance, smaller buffering requirement and greater throughput. Because of these unique features wormhole switching is being advocated for on-chip networks.

3.4 FSM Implementation

As for the backtracking feature of the path-setup scheme, the Exhaustive Profitable Backtracking (EPB) protocol is used to reduce on-chip implementation complexity. Moreover, the proposed EPB-based path-setup establishes only minimum paths that result in energy-efficient data transfer.

The EPB-based probing path-setup performs a straightforward depth-first search of the network using only profitable links. It does not repeatedly search the same path, and guarantees to find a minimal path if one exists. The history information used for backtracking, can be stored either in the probe header, or distributed in the switching nodes. The former method significantly increases probe header size, and, consequently, increases the required processing time to route the probe header through the network. It is particularly a problem when the number of links traversed during the path setup becomes very high. Therefore, the latter method is selected, in which the history information is distributed throughout the switching nodes of the network, to reduce the probe header size.

Since the history information for backtracking is stored in switches, the probe header contains only the destination address.. The probe header is handled to move forward or backward according to the control signals in switch-by-switch handshake (as denoted in Table 1).

Table 1: Bit format

Request Signal: Req (1 bit)	
0: Idle (Release)	1: Circuit Request
Answer signal: Ans (2 bits)	
00: Idle	10: Network Blocked &
01: Circuit Acknowledge	Busy Destination

The Ctrl In is the key component to perform the backtracking probing task. This includes functions, such as processing history information of backtracking and constructing a table of possible output ports for probing (i.e., route-probing table).

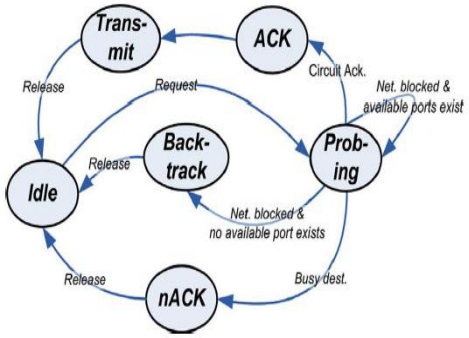

Figure 6: Simplified state diagram for FSM implementation of Ctrl In to support backtracking probing operation.

As shown in Figure 6 when a request with the incoming probe header arrives, Ctrl In goes into the Probing state, compares the current switch address and the destination address (i.e., performs address decoding) to find possible outputs for probing. Based on history information of backtracking, current availability of the output ports, and/or the feedback from the downstream switches, Ctrl In may change into the *ACK*, *nACK* or *Backtrack* states, correspondingly. These operations of Ctrl Ins consistently constitute the backtracking probing path-setup scheme supported by BW switches throughout each guaranteed throughput lane of the NoC.

4. Results and Discussion

The BW Switch implemented for use under 3X3 partial mesh topology consists of 8I/O ports corresponding to the 8 directions (North, East, West, South, NE, NW, SE, and SW) each receiving 32bits of data. The BW switch can also backtrack flexibly to search for an available alternate path during congestion thereby increasing the throughput.

The BW Switch here is simulated in Modelsim for a few request combinations and the response is shown with the help of screenshots.Figure below shows a sample screenshot depicting the route followed by the flits from source node 1 to destination node 7 via intermediate hops. A 32 bit data including an 8 bit header is given as input to the switch 1 in south direction. The destination address being node 7 the router establishes the path from node1 through intermediate hops node 2 and node 5 to node 7. As node 2 is blocked a nACK=10 is sent and the probe header decides to backtrack to find an alternate minimal path.

On backtracking the flits travel from node 1 through node 3 & 5 and finally reach node7. ACK=1 is sent from destination node7 after successfully receiving all the 4 flits.

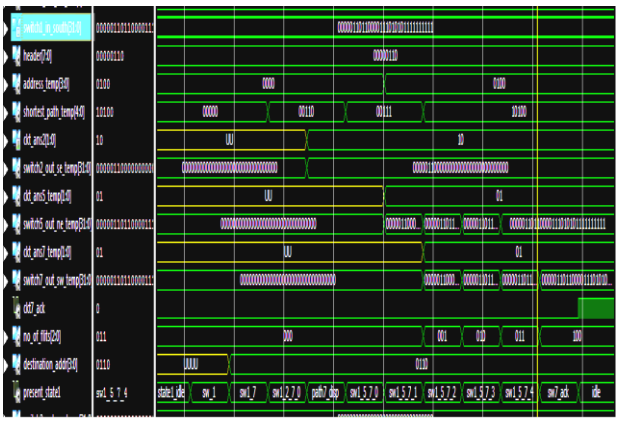

Figure 7: Routing from node 1 to 7 with backtracking

5. Conclusion and Future Work

To get the best optimization of the combined operation of arbitration and multiplexing, irrespective of the complexity of the priority selection policy, aiming at the design of efficient high-radix and low-latency switches, a new structure called Merged ARbiter and multipleXer (MARX) that merges efficiently the functionality of the arbiter and the multiplexer is designed. Later these MARX units serve as the baseline to design MARX with dynamic priority arbitration schemes. Using this dynamic priority MARX units' wormhole switch design is implemented with the concept of backtracking. The resulting wormhole switch module is designed using verilog/vhdl language and simulated in ModelSim simulator. In future the same concept can be applied to any of the network topologies to maximize the performance in terms of area, speed, power. Also security algorithm can be incorporated to make intercommunication feasible.

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