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A New Technique for Low Power Double Tail Comparator Using Parallel Mechanism

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Abstract- Comparators are the most analyzing unit in the analog to digital converters. In such situation we have to use the high speed and the low power consumption based comparators. Hence we are designing the comparators is more challenging when the supply voltage is smaller. To achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. In this paper we are presenting the low power and high speed comparators even in small supply voltages. This comparator design having the small count of transistors which is used to reduce the delay time. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors if they do not increase the circuit complexity.

***Index Terms*—Double-tail comparator, dynamic clocked comparator, high speed analog to digital converters, low power analog design.**

I.INTRODUCTION

COMPARATOR is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many highspeed ADCs, such as flash ADCs, require high-speed, low-power comparators with small chip area. In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals V+ and V- and one binary digital output V0. A comparator consists of specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs), as well as relaxation oscillators. Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to digital converter and for that reason they are mostly used in large abundance in A/D converter. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal.

II. LITERATURE SURVEY

High-speed comparators in ultra deep submicrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods [2], [3], techniques employing body-driven transistors [4], [5], current-mode design [6] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS

technologies. Body-driven technique adopted by Blalock [4], removes the threshold voltage requirement such that bodydriven MOSFET operates as a depletion-type device. Based on this approach, in [5], a 1-bit quantizer for sub-1V __ modulators is proposed. Despite the advantages, the bodydriven transistor suffers from smaller transconductance (equal to *gmb* of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. The structure of double-tail dynamic comparator first proposed in [10] is based on designing a separate input and crosscoupled stage. This separation enables fast operation over a wide common-mode and supply voltage range [10]. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [10], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

III. EXISTING SYSTEM

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and *M*tail is off, reset transistors (*M*7–*M*8) pull both output nodes Out*n* and Out*p* to *V*DD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = *V*DD, transistors *M*7 and *M*8 are off, and *M*tail is on. Output voltages (Out*p*, Out*n*), which had been pre-charged to *V*DD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where *V*INP > *V*INN, Out*p* discharges faster than Out*n*, hence when Out*p* (discharged by transistor *M*2 drain current), falls down to *V*DD–|*V*thp| before Out*n* (discharged by transistor *M*1 drain current), the corresponding pMOS transistor (*M*5) will turn on initiating the latch regeneration caused by back-to-back inverters (*M*3, *M*5 and *M*4, *M*6). Thus, Out*n* pulls to *V*DD and Out*p* discharges to ground. If *V*INP < *V*INN, the circuits works vice versa.

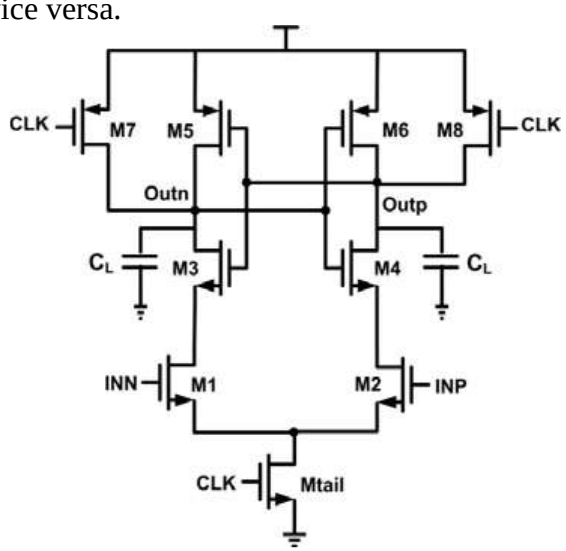

Fig:1 Schematic Diagram of Conventional dynamic comparator

B.Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig. 2 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset [10]. The operation of this comparator is as follows . During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. During decision-making phase (CLK = *V*DD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by *I*Mtail1/*C*fn(p) and on top of this, an input-dependent differential voltage _*V*fn(p) will build up. The intermediate stage formed by *M*R1 and *M*R2 passes _*V*fn(p) to the crosscoupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10]. Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, *t*0 and *t*latch. The delay *t*0 represents the capacitive charging of the load capacitance *CL*out (at the latch stage output nodes, Out*n* and Out*p*) until the first n-channel transistor (*M*9/*M*10) turns on, after which the latch regeneration starts.

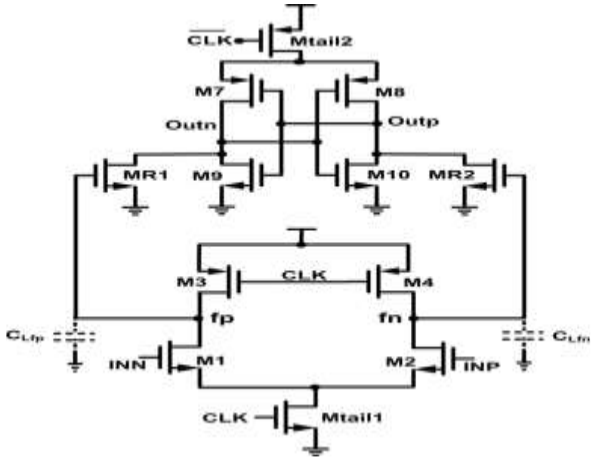

Fig:2 Schematic Diagram of Conventional Double tail Dynamic Comparator

IV. PROPOSED SYSTEM

In this paper we are going to propose the low voltage low power double tail comparator. The proposed comparator works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes low power. To overcome the static power consumption issue two NMOS switches are used below the input transistors. This could be having low power consumption compared to the conventional comparator. Then also the delay could be reduced in this comparator. Boosting and boot strapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock, removes the threshold voltage requirement such that body driven MOSFET operates as a depletion-type device. Based on this approach, in, a 1-bit quantizer for sub-1V modulators is proposed. Despite the advantages, the body driven transistor suffers from smaller transconductance (equal to *gmb* of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In the, additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages.

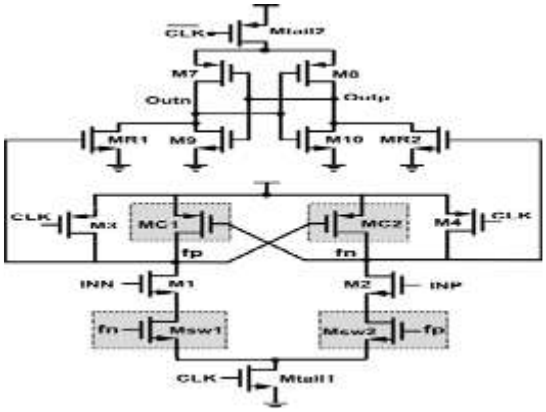

Fig:3

Shematic Diagram of Proposed Dynamic Comparator

The proposed comparator of works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 μW. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed is based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range.

V.SIMULATION RESULTS

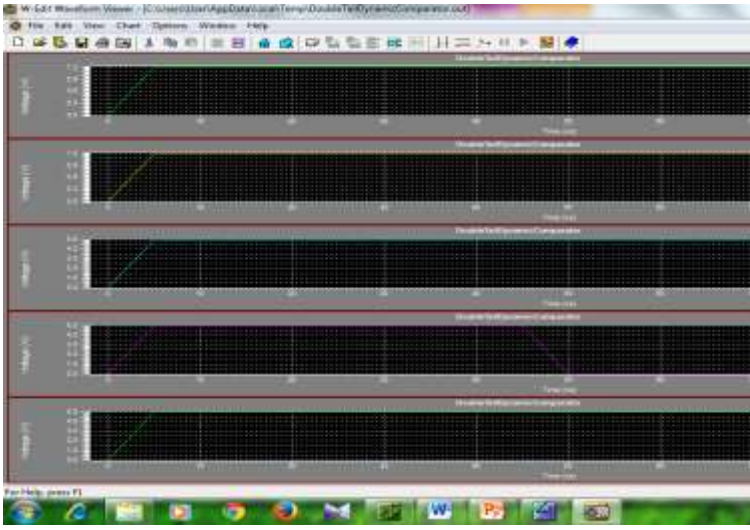

Fig:4 Output Waveform for Proposed Structure

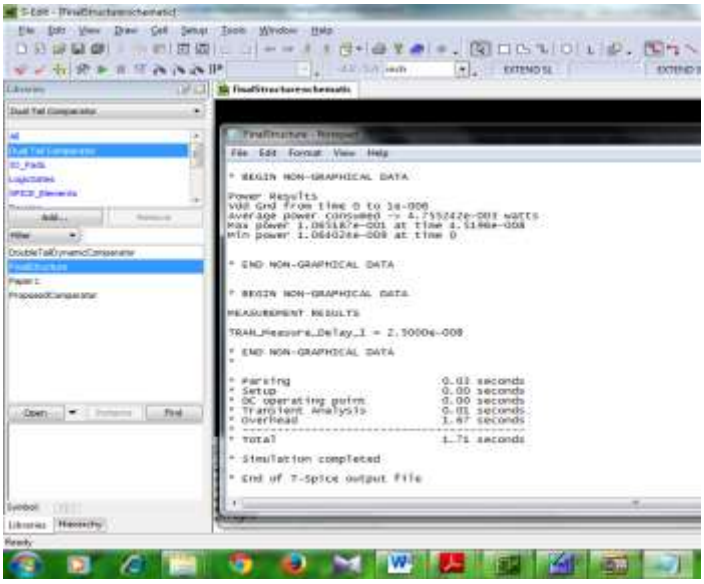

Fig:5 Power and Delay Analysis

TABLE 1
SUMMARY OF THE COMPARATORS PERFORMANCE

Comparator structure	Conventional dynamic Comparator	Conventional Double-tail Comparator	Proposed Comparator
Power	**9.182e-004W**	**8.366e-004W**	**4.75e-006W**
Delay	**7.8475 ns**	**2.5008 ns**	**2.500 ns**

VI.CONCLUSION

In this paper, we presented a comprehensive delay and power analysis for clocked dynamic comparators . Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Delay as well as power is reduced to a great extent compared to conventional structures.

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