

# A GDI Approach to Various Combinational Logic Circuits in CMOS Nano Technology

Shashank Gupta<sup>1</sup>, Subodh Wairya<sup>2</sup>

<sup>1,2</sup>Electronics Engineering Department, Institute of Engineering & Technology, Dr. A.P.J Abdul Kalam Technical University, Lucknow-226021, U.P, India

<sup>1</sup>Shashankgupta435@email.com

<sup>2</sup>swairya@ietlucknow.edu

**Abstract:** Gate Diffusion Input provides one of the effective alternatives in low power VLSI application. With the help of GDI, circuits requiring large number of transistors can be realized with the help of quite less number of transistors. This approach tends to optimize various performance parameters such as area, delay, power dissipation. In this paper GDI cell has been applied in realizing various combinational circuits. One of the novel design has been proposed (XOR circuit using only nMOS) for providing low power in digital circuit. Based on simulation results their waveforms have been analyzed and various performance parameters have been calculated. These parameters are then compared to standard CMOS logic. The schematic and layout are drawn on 120nm technology file on a Dsch tool and their analysis is done on a Microwind 3.1 tool and BSIM simulator.

**Keywords:** GDI, Half Adder, Full Adder, MUX, Comparator, Parity Checker

## 1. Introduction

With the scaling of technology to submicron process, power consumption becomes a critical parameter in the design CMOS VLSI circuits. With advancement in technology along with the rapid development of portable digital application the demand for high, speed, compact implementation and low power dissipation has triggered numerous research efforts [1], [2]. Therefore various design methodologies such as CMOS and PTL are suggested to optimize various parameters. A comprehensive comparison between the Pass Transistor Logic (PTL) and static CMOS approach was presented by Zimmermann et. al. [3]. For improvement in power dissipation several design techniques are proposed [4]-[6]. One such technique is GDI and modified GDI. With the help of GDI the circuits can be realized using lesser number of transistors which result in reduction in area, delay and hence power consumption also gets reduced.

In any circuit power dissipation depends on two basic components. First is static power dissipation which mainly occurs due to leakage current or because of the current drawn continuously from power supply and second is called dynamic power dissipation which occurs due to charging and discharging of the load capacitances i.e. because of switching transients. There are various ways to reduce leakage power. They are sleep mode approach, stack approach, Leakage feedback approach, sleepy stack approach, sleepy keeper approach [7]. There are various parameters by which we can optimize the power in digital circuits. The power can be reduced by reducing switching voltage, capacitance, switching frequency and leakage current [8].

In this paper section 2 deals with the overview of GDI cell. In section 3 various combinational circuits along with their waveforms are presented. Section 4 provides a novel design for XOR gate using nMOS only and its associated waveforms. Since nMOS has better mobility the circuit in turn results in better current driving capacity.

## 2. GDI overview

GDI approach makes use of a GDI cell as shown in fig.1 [9]. This cell resembles a CMOS inverter with some alterations. A GDI cell has four terminals – G (common gate of pMOS and nMOS transistors), N (input to the source and drain of the nMOS), P (outer diffusion node of pMOS transistor) and Out node which acts as a common diffusion node for both the transistors.

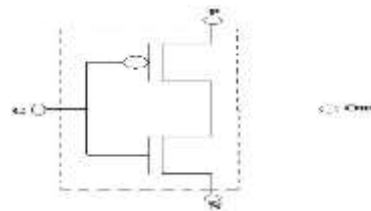


Figure 1: Basic GDI cell

Table I shows various functions and logical expressions that can be implemented using GDI cell [10]. These functions may require 6-12 transistors with the use of CMOS technology but with GDI, implementations of these function is very simple and require only two transistors. This in turn reduces the area, delay and hence the power consumed by the circuitry.

With the help of GDI Multiple input gates can also be implemented. This can be done by combining several GDI cells.

Table 1: Basic GDI Functions

N	P	G	Out	Function
'0'	B	A	$\overline{AB}$	F1
B	'1'	A	$\overline{A} + B$	F2
'1'	B	A	$A + \overline{B}$	OR
B	'0'	A	$AB$	AND
C	B	A	$\overline{AB} + AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

### 3. Implementation of basic combinational circuits using GDI Cell

This section deals with realization of various combinational circuits which forms a basic building block in designing several complex circuits.

#### 3.1 Half Adder

The GDI implementation of half adder is shown in fig. It employs a GDI cell based XOR gate and an AND gate to realize sum and carry outputs as shown in fig. 2.

$$SUM = A \oplus B$$

$$CARRY = AB$$

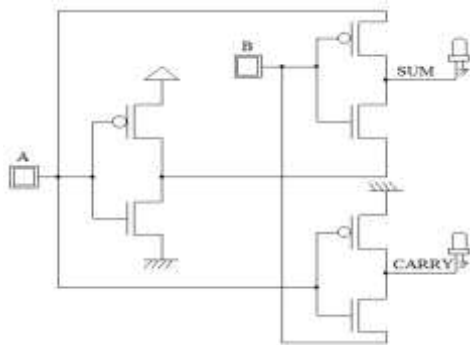


Figure 2: Half adder using GDI

The waveform of Half adder depicting sum and carry output is shown in fig. 3.

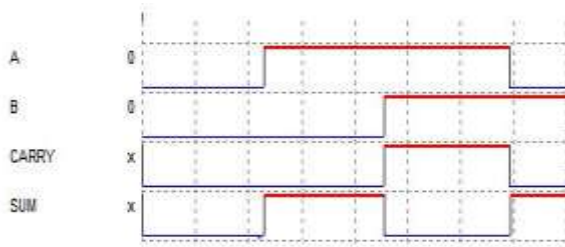


Figure 3: Half Adder waveform

#### 3.2 Full adder

In both GDI Half and Full adder XOR gate forms the basic block to generate the sum. With GDI XOR the number of transistors to realize the adder gets reduced to great extent. This in turn reduces the surface area and also the power dissipation. Fig. 4 represent GDI Full adder.

$$SUM = A \oplus B \oplus C$$

$$CARRY = AB + (A \oplus B)C$$

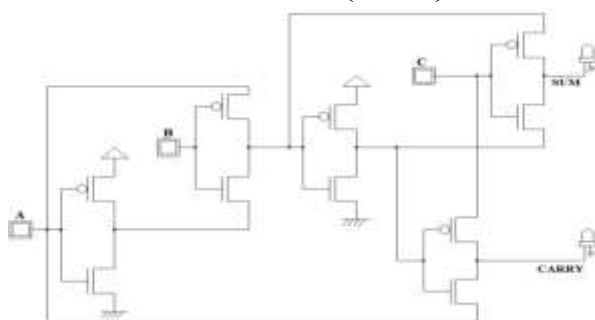


Figure 4: Full Adder using GDI

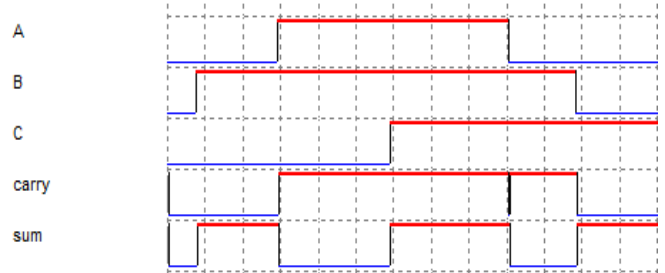


Figure 5: Full Adder waveform

#### 3.3 Half Subtractor

A half subtractor has two inputs A (Minuend) and B (Subtrahend) and output as Diff (Difference) and Bout (Borrow). Fig. 6. depicts GDI realization of half subtractor.

$$Diff = A \oplus B$$

$$Bout = \bar{A}B$$

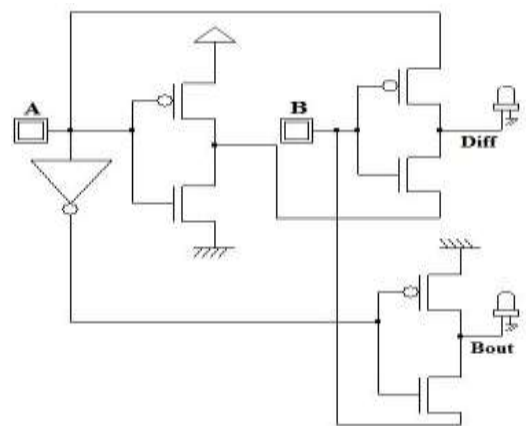


Figure 6: Half Subtractor using GDI

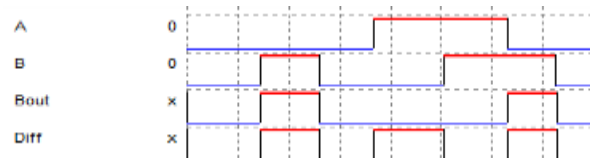


Figure 7: Half Subtractor waveform

#### 3.4 Parity Checker

It is the most common method employed in detecting errors particularly in storage devices. Three 2 input XOR gates are required for parity detection of a 4 bit number. Hence when the number of 1's in the input is even produces the output 0 and produces output as 1 for odd number of 1's in the input. A GDI based parity checker circuit is shown in fig.8.

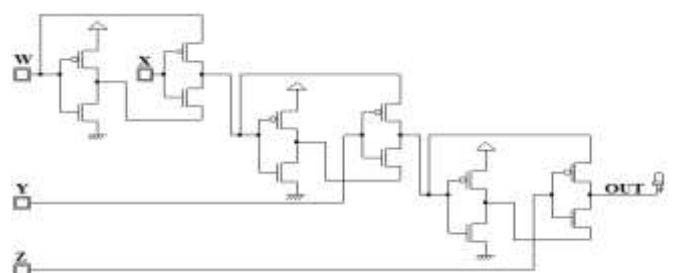


Figure 8: Parity Checker using GDI

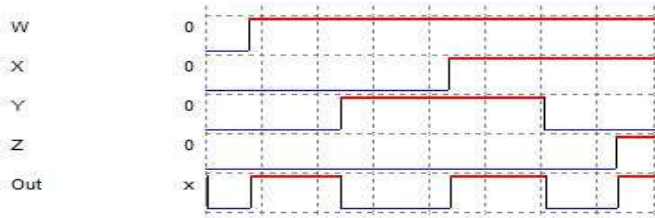


Figure 9: Parity checker waveform

### 3.5 1 Bit Magnitude Comparator

To realize 1 Bit magnitude comparator EXOR and AND mainly used. It consists of two inputs for allowing two single bit numbers and three outputs to generate less than, equal and greater than comparison outputs. Since XNOR produces output 1 for same bits of input, this property is used to find if the two bits are equal. An AND gate is used to check first bit is greater or lesser than the second. GDI cell based 1 Bit magnitude comparator is shown in fig. 10. The same principle can be further extended to n-bit comparator.

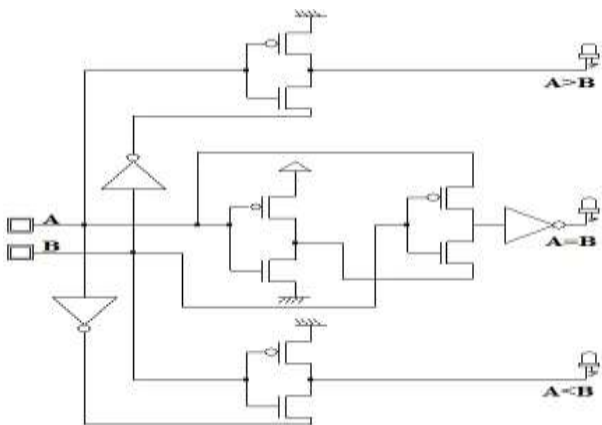


Figure 10: 1 Bit magnitude comparator

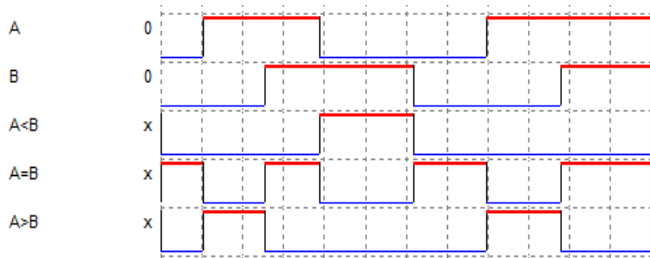


Figure 11: 1 Bit magnitude comparator waveform

### 4. Proposed XOR using nMOS

In this section a novel design for XOR gate is put forward. The XOR gate is implemented with nMOS only as shown in the fig. Since the mobility of electron is high compared to holes, so the XOR gate schematic with only nMOS result in better switching and current driving capacity. Also because of higher speed it is therefore mostly used in switching. The circuit of nMOS XOR gate is shown in fig. 12. It basically has 3 stages cascaded to produce XOR output. The first and third stages are identical which gives the invert of inputs A and B respectively. The second stage is used to combine them to produce the desired result.

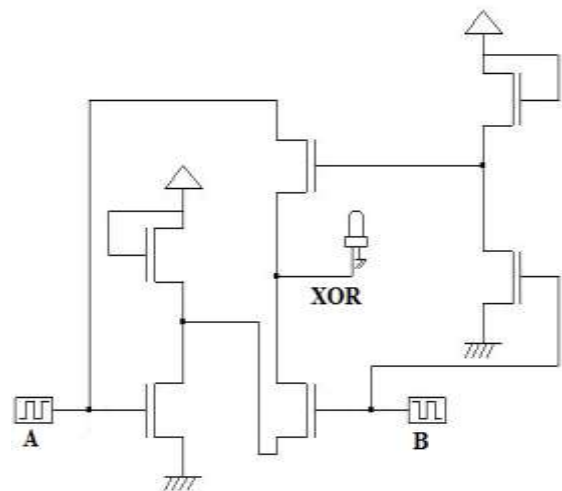


Figure 12: nMOS based XOR Gate

The waveform of the XOR circuit using nMOS is shown in fig. 13 and its associated layout is shown in fig.14. The area obtained in the layout is 63.0  $\mu\text{m}^2$ .

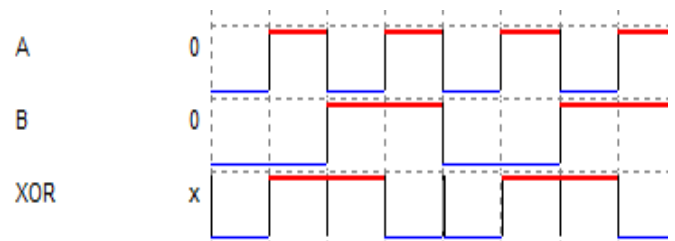


Figure 13: XOR waveform for the proposed circuit

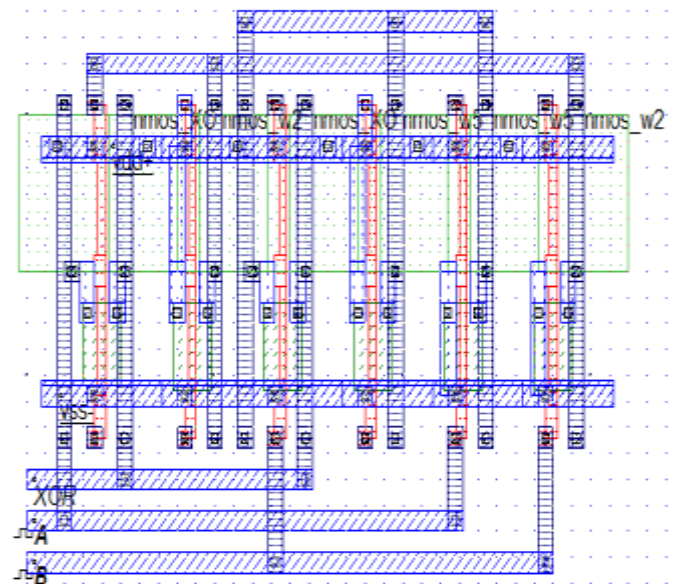


Figure14: Layout of the proposed nMOS XOR Gate

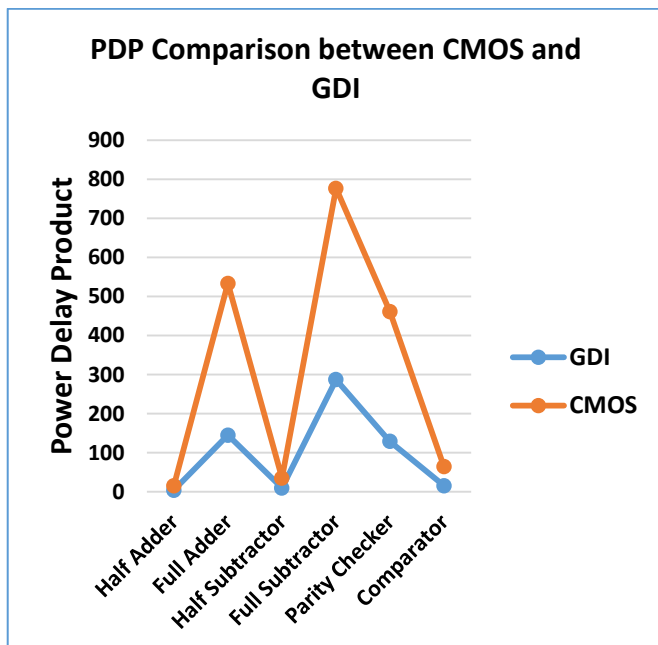
The comparison between CMOS and GDI is shown in Table II. Various performance parameters such as power, area, delay and also the number of transistors need to implement a particular circuit are evaluated. Based on this the Power delay product (PDP) is evaluated which denotes the energy per switching event. Smaller the PDP better will be the circuit.

**Table II:** Parameter Comparison between CMOS and GDI

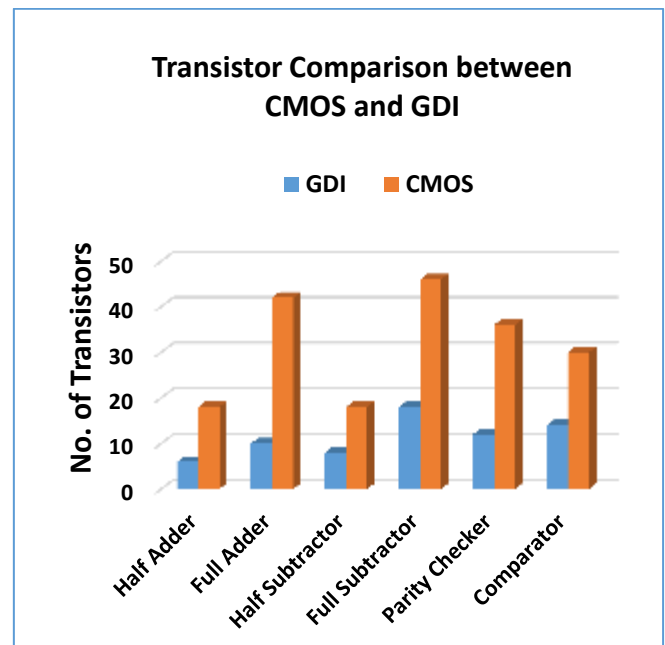
Circuit Design	GDI				CMOS			
	Power ( $\mu\text{W}$ )	Area ( $\mu\text{m}^2$ )	Delay (ns)	No. of Transistors	Power ( $\mu\text{W}$ )	Area ( $\mu\text{m}^2$ )	Delay (ns)	No. of Transistors
Half Adder	1.435	97.70	1.49	6	4.194	131.40	3.45	18
Full Adder	29.738	179.60	4.86	10	48.546	285.70	10.98	42
Half Subtractor	5.811	111.60	1.97	8	7.529	161.30	4.64	18
Full Subtractor	49.204	261.10	5.83	18	62.802	367.40	12.37	46
Parity Checker	28.183	226.8.80	4.57	12	46.937	289.60	9.82	36
1 Bit magnitude Comparator	7.371	168.60	2.36	14	11.823	217.70	5.39	30

The power Delay Product represents the figure of merit in relation with energy efficiency of logic families or logic gate. It is also called switching energy. Fig.15 depicts the PDP comparison between CMOS and GDI. PDP is the product of average power consumption and delay in a digital logic circuit.

Fig.16 gives an account of the number of transistor used in CMOS and GDI techniques. The graph clearly depicts the huge reduction in the transistor count. With the constant increase in number of transistors, current processors are demanding a considerable amount of energy in a very small area.

**Figure 15:** PDP comparison between CMOS and GDI

The transistor count is one of the important parameter which governs parameters like delay and power consumption. It is one of the most common measure of the complexity of the semiconductor IC. In case of CMOS large number of transistor are used which in turn increases delay and significantly affect the power consumption in circuit.

**Figure 16:** Comparison of transistor count between CMOS and GDI

This results in high power dissipation. And it is not only the number of transistors. There are other factors such as High operating frequencies which do have a serious impact on power consumption. So a tradeoff must exist among the performance parameters.

## 5. Conclusion

The GDI approach was broadly presented which tends to optimize the performance parameters of digital circuits. Various combinational circuits are presented which forms the core in digital applications. Their parameters are analyzed on 120nm CMOS Technology. Along with this a novel design for XOR gate by using nMOS only was presented which tends to improve the current driving capacity of the circuits. Future research may include some other GDI cell applications and their analysis.

## References

- [1] N. Weste and K. Eshraghian, Principles of CMOS VLSI design: A System Perspective Reading Education, Addison-Wesley, 2002
- [2] A.P. Chandrakasan, R.W. Brdersen, "Minimizing Power Consumption in Digital Circuits", In Proceeding of the IEEE, vol. 83, no. 4, pp. 498-523, April 1995
- [3] R. Zimmermann and W. Fitcher, "Low Power Logic Styles: CMOS Versus Pass Transistor Logic", IEEE J. Solid-State Circuits, vol. 32, pp. 1079-1090, June 1997.
- [4] Sung-Mo Kang, Yusuf Lablebici, CMOS Digital Integrated Circuits: Analysis and Design, TATA Mc GRAW-HILL, 3<sup>rd</sup> ed. 2003.
- [5] Estinne Sicard, Sonia Delmas Bendhian, Basic CMOS Cell Design, Tata Mc-Graw Hill.
- [6] R. J. Baker, Harry W. Li and David E. Boyce, CMOS Circuit Design. Layout and Simulation, IEEE Press Series.
- [7] Ajay Kumar Dadoria and Kavita Khare , "A Novel Approach For Leakage Power Reduction Techniques in 65NM Technologies", International Journal of VLSI design and Communication System (VLSICS), vol. 5, No. 3, June 2014
- [8] G. Saranya, R. S. Kiruthika, "Optimized Design of an ALU Block using Architectural Level Power Optimization Techniques", in proceeding of IEEE conference in Recent Advances in Intelligent Computational System (RAICS), pp. 168-172, 2011
- [9] Arkadiy Morgenshtein, Viacheslav Yuzhaninov, Alexey Kovshilovsky and Alexander Fish, "Full-Swing Gate Diffusion Input Logic- Case Study of Low Power CLA adder Design", Integration, the VLSI Journal 47, 62-70, 2014.
- [10] Arkadiy Morgenshtein, Idan Schwartz and Alexander Fish, "Gate Diffusion Input (GDI) Logic in a Standard CMOS Nanoscale Process", IEEE 26<sup>th</sup> Convention of Electrical and Electronics Engineers in Israel, 2010.

## Author Profile



**Shashank Gupta** received the B.Tech degree in Electronics and Communication Engineering from IEC College of Engineering and Technology, Uttar Pradesh Technology University, Greater Noida, India and is currently working towards his M. Tech degree in Microelectronics with the research interest in Low Power VLSI and enhancing the performance of digital circuits from Institute of Engineering and Technology, Lucknow, Uttar Pradesh.