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Performance Analysis of Mesh, Torus and Folded Torus under Broadcasting, using Distance Vector Algorithm

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Abstract: ***In this technological world of communication architecture, network on chip (NoC) is extensively used as communication architecture. Network on chip (NoC) topologies are becoming a backbone of communication architectures. It provides a good integration of enormous amount of storage on chip blocks as well as computational also. Network on chip handled the unfavorable conditions and it provides the scalability to the architecture. Mesh, Torus and folded torus architectures are most commonly used architecture for network on chip communication. Here, we compare the performance of Mesh, Tours and Folded torus network architecture on chip, on the basis of different parameters under broadcasting with the help of distance vector routing algorithm. To evaluate the performance of Mesh, Torus and folded torus network on chip in the simulation environment, we simulate the topology using Network Simulator (NS-2).***

Keywords: Torus, Folded Torus, Performance, NoC, Network on Chip, latency, throughput

1. INTRODUCTION

In the increasing complexity of communication architecture and rising the demand of integration of computational and storage blocks on a single chip, the attention of researchers in this area, developed globally. Since it is a great challenge to increase the system performance with limited area and power limitations. Moreover the design specific routing, exchange the information over routing the packets in the network based on new age technology of networks, the issues which are scalability as well as reuse of design make NoC (Network on Chip) more favorable as compare to outdated technology architecture.

Many researchers are developing the research area as part concepts from the area of parallel computing and networks to sphere domain of VLSI. It is seems like imagination due to Network on chip and traditional networks are two different circumstances with conflicts in reference of requirements. Traditional networks are distinct from storage on chip due to non-determinism and closeness. The design methodology of network on chip is found in [4, 5 and 6]. A crucial factor of chip, in on chip network topology, in term of some quality parameters which are energy consumptions, whole performance as well as cost. After analysis of the different network topologies we find that there are grid based arrangement and match the VLSI design. Since Network on

Chip is commonly used mesh, torus and folded torus topologies to establish a

network on chip architecture for communication [7, 8 and 9]. There are different network on chip topologies has been proposed such as Mesh, Torus, Star, Octagon, SPIN, Folded Torus [10, 9, 11, 12, 13 and 14]. Folded Torus topology is reduced the latency of Torus and Torus topology reduced the latency of mesh. The problem of excessive delay in mesh and torus topology is avoided in folded torus topology. From the literature, mesh, torus and folded torus topologies has given more attention of researchers for network on chip. In this paper, we compare the performance of torus and folded torus topologies under broadcasting using distance vector routing algorithm in orientation of different crucial parameters.

2. RELATED WORK

Improving the performance of interconnection network is essential to success to increase the number of processing cores on a single chip. We have requires to rise the processing of data and communication. Although high communication performance requirements of many core processor can meet through asymmetrical topologies and it is suited for different variety of traffic patterns. Two topologies like torus named as xxtorus and xtorus, estimate the performance on the basis of link entropy, theoretical analysis, and path diversity and heterogeneous link design also as well as take the advantages of higher level of VLSI process [16]. A torus based hierarchical hybrid optical-electronic network on chip (THOE)

and different techniques as optimization of floor plan, power control mechanism, low latency control protocols and hybrid optical-electrical routers and interconnects, hierarchical in nature is described and compare THOE with torus based optical network on chip as well as torus based electronic network on chip [17]. On chip networks faults, degrade their performance in communication and other parameters of works. A Markov model based analysis for terminal reliability of mesh and 2D torus is proposed in [18].

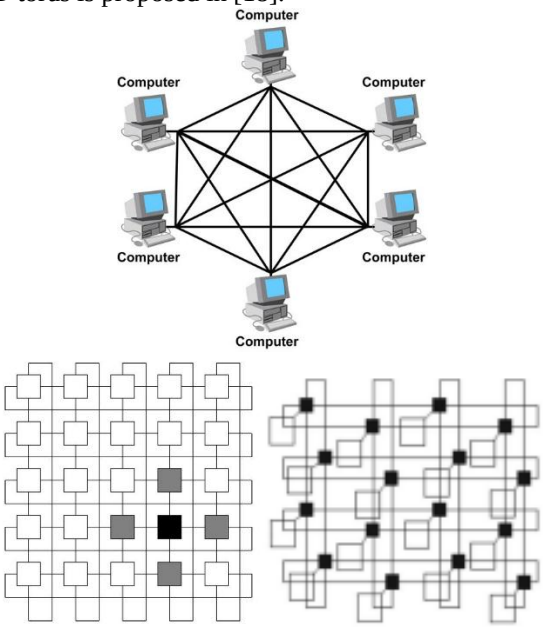

Figure 1: Mesh (Top),

Torus (left) & Folded Torus (right) Topology

Torus Topology is the most popular inter-processor communication networks which is used in current parallel supercomputers. Numerous methodologies to optimize the power efficiency by reducing the number of waveguide crossing point of optical network on chip in the floor plan. The floor plans of optical network on chip for torus and folded torus topology and design metrics for torus as well as folded torus based optical network on chip is given in [20]. A highly scalable with fault tolerant interconnection networks of 6-D mesh/folded torus topology for large scale supercomputers architectures is discussed in [21]. Zigzag and simple mapping function of embedding mesh and torus topology on to degree four chordal rings is discussed and topological properties are also investigated in [22]. But the comparison of torus and folded torus topology can be evaluated by the network simulator.

Torus and folded torus network architectures are the most commonly used for network on chip topologies. So the performance of 3D torus and 3D folded torus topology is analysed. The comparison of hierarchical torus network (HTN) by H3D mesh, torus and mesh network is given and also evaluate the performance of HTN under common traffic pattern [24]. The single routing node architecture, including packet format, routing and arbitration, routing algorithm and node routing direction, the programming and simulation of proposed architecture are designed [25]. The performance is compared on the basis of packet loss with source routing using different traffic generation mechanism with handshaking for parallel transmission concepts [26].

3. SYSTEM MODEL

We compare the performance of Mesh3x3, Torus 3×3 and folded torus 3×3 network architectures or topologies on the basis of different parameters. To perform this task, we use the network simulator (NS-2). The network animator (nam) files of Mesh, Tours 3×3 and folded torus 3×3 topologies is given in figure 2 ,3 & 4.

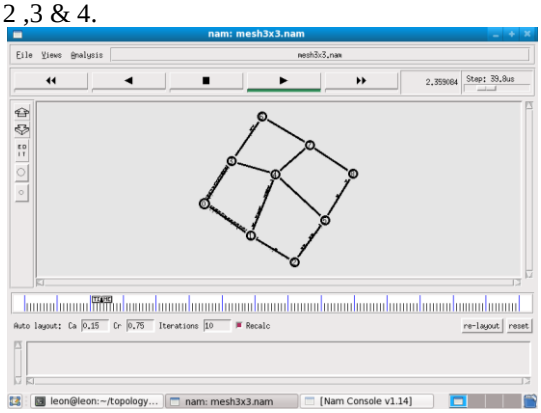

Figure 2: Network Animator of Mesh 3x3

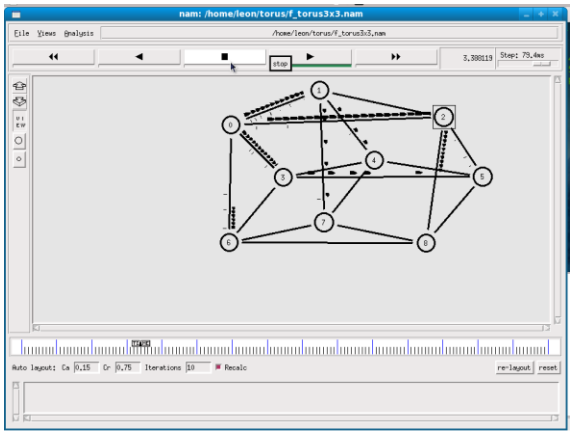

Figure 3: Network Animator of Torus 3x3

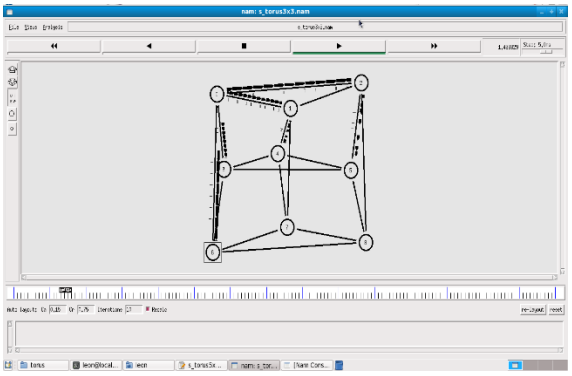

Figure 3: Network Animator of Folded Torus 3x3

4. RESULTS AND DISCUSSION

We compute the results of the nodes of 9, 16, and 25 in torus and folded torus topologies under distance vector routing algorithm. To compare the performance of three topologies named as mesh 3x3, tours 3×3 and folded torus 3×3 on basis of some important parameters such as Throughput, Latency, Dropping Probability, Packet received on the end nodes under broadcasting using NS-2 Simulator.

4.1. Throughput

Throughput can be defined in the different ways, it depends on the basis of implementation. In the present scenario, the throughput can be defined as follows [15]

$$Throughput = \frac{Total\ Completed\ Message * Length\ of\ Message}{Number\ of\ blocks\ of\ IP * Total\ Time}$$

In the above formula, the number of messages arrived at their destination is called total completed message. The number of function IP blocks which in involved in the communication is known as number of block of IP. Length of message is taken in flits. Time is taken in between the occurrences of the first message generation and last message reception. These things have been taken in the program of NS-2 simulator. After execution of program, the simulation results show the comparison of mesh3x3, torus 3×3 and folded torus 3×3 topologies. The simulation result is in figure 5

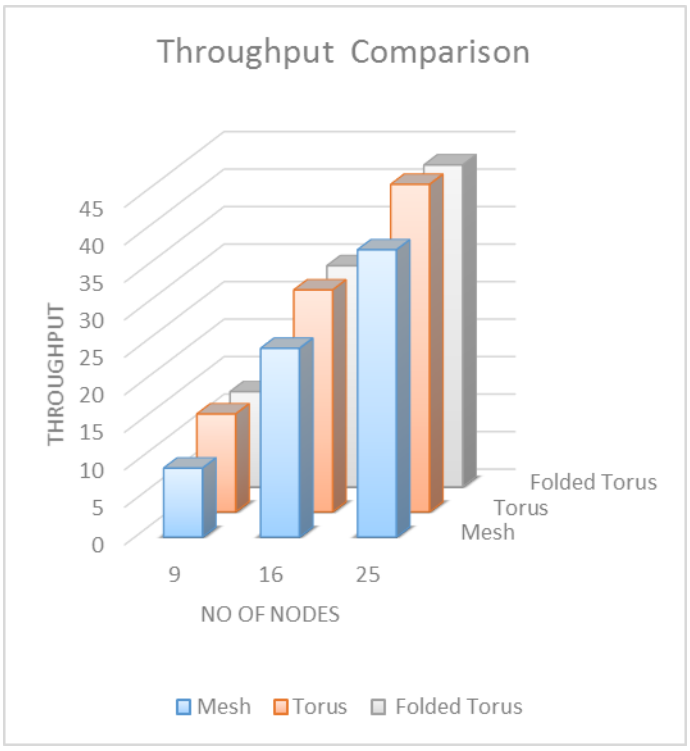

Figure 5: Comparison of throughput of Mesh, Torus and Folded torus topologies

4.2. Latency

The time that elapses between the occurrence of a message header injection into the network at the source node, that include the queuing time in source, and the occurrence of the corresponding tail flit reception at the destination node [29] is known as latency. Since we take the transport of nodes in one place to another place, here we called this as transport latency. Simulation results are given in figure 6.

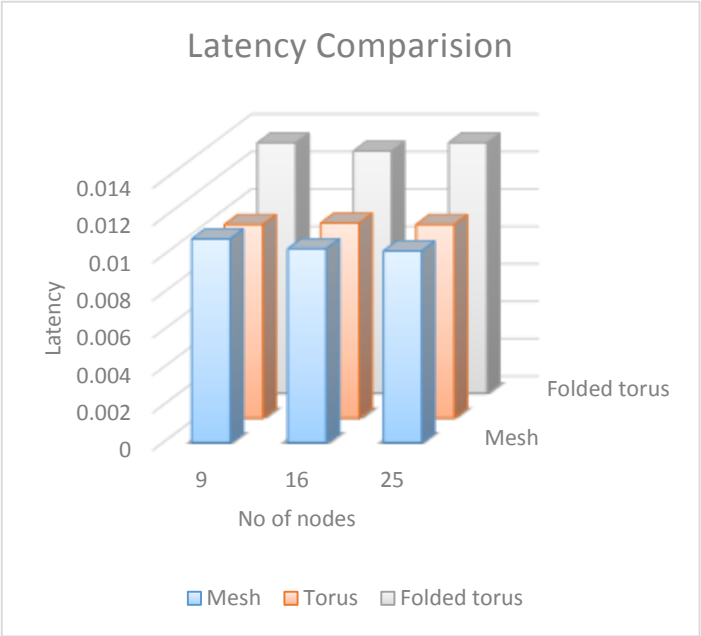

Figure 6: Comparison of latency of Mesh, torus and Folded torus topologies

4.3. Drop Probability

According to probability theory, we find the dropping probability of packets as total no of packet drop which is divided by total number of dropped packets and total number of received packets at the destination nodes [27]. This may be as follows:

$$Drop\ Probability = \frac{Tot.\ No.\ of\ drop\ packets}{Tot.\ No.\ of\ (sended + recieved)\ packet}$$

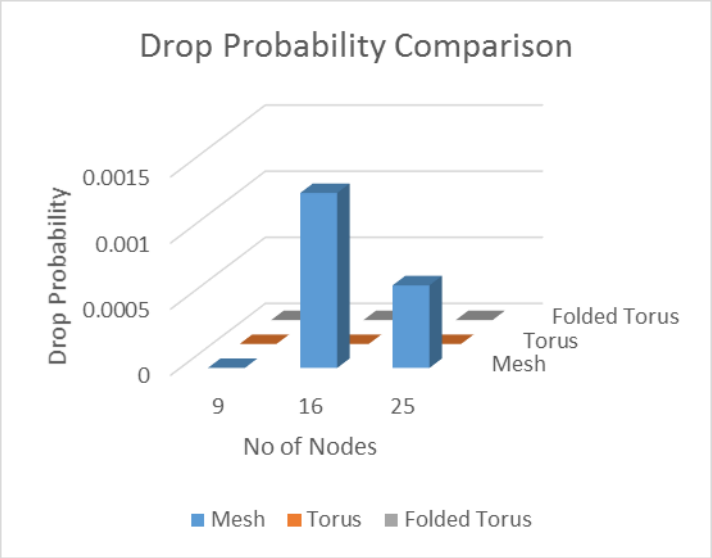

Figure 7: Comparison of drop probability of Mesh, torus and Folded torus topologies

4.4. Total Packet Receive on the end-node

Now, we calculate how many packets are received on the destination nodes in mesh, torus and folded torus topology.

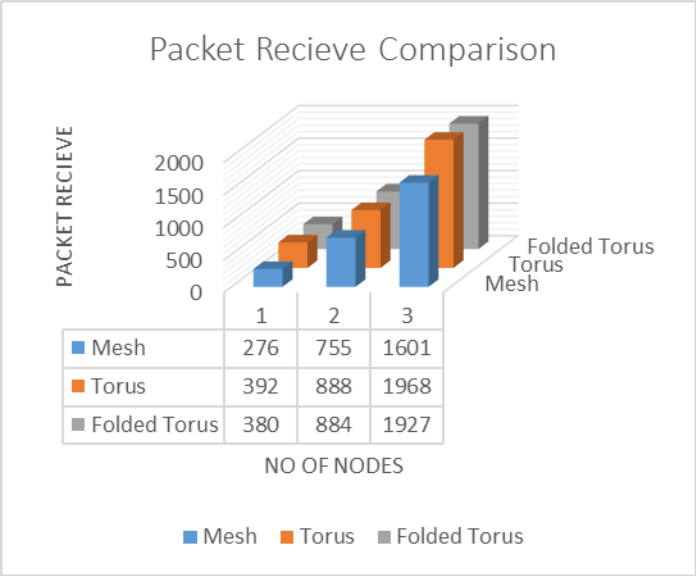

Figure 8: Comparison of Total Packet Receive of Mesh, torus and Folded torus topologies

5. CONCLUSION

Finally we conclude that NoC have overcome the disadvantages of Storage on chip. Mesh, Torus and folded torus are three well-known and widely used topologies among many offered Network on chip topologies. We carried out widespread comparisons of mesh, torus and folded torus networks by distance vector routing algorithm using broadcasting for different statistics of merit such as latency, throughput, drop probability and packet receive.

We get that folded torus has always better latency than torus and mesh. Still the cost we pay for this enhancement is higher power consumption in the case of torus and mesh topology. Routing algorithms, number of nodes and number of links in a network have a direct effect on power Consumption and latency. So we applied folded torus topology which has less power consumption because we used less no of links in folded torus as compared to torus and mesh. Folded torus has less latency than torus and mesh.

In conclusion, we designated the folded torus topology which has more throughputs, less latency, less drop probability and its packet receive ratio as compared to torus and mesh. Therefore we conclude that folded torus is better than torus and mesh topology using distance vector algorithm under broadcasting model. For future work, the comparison between mesh, torus and folded torus under different type of casting like broadcasting, multicasting, and unicasting in different scenario using AODV, DSR and OLSR algorithm can be implemented.

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