www.ijecs.in
International Journal Of Engineering And Computer Science ISSN:2319-7242
Volume 2 Issue 4 April, 2013 Page No. 1156-1161

Carry Bypass & Carry Select Adder Using Reversible Logic Gates

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Date of Submission: 24th April, 2013

Abstract
In the recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology, and optical computing. The basic gates such as AND, OR, and EXOR are not reversible. This paper presents various designs of reversible logic gates used for reversible operation & the applications as carry bypass and select adder Block. This paper also includes simulation result of forward & backward computation of reversible TSG, Fredkin & Toffoli gate. These gates are then used to design four bit Carry bypass and select Adder blocks. Methodology used for designing reversible gate is Tanner Tool Version-14.1 & technology file 0.25 micron. It is shown that the adder architecture designed using TSG Fredkin & Toffoli gate are much better & optimized as compared to existing four bit Carry bypass and select Adder in terms of low power dissipation .The four new reversible gates are also proposed in this paper.

Keyword - Reversible Logic, TSG, Fredkin, Reversible adders.

I. INTRODUCTION

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Modern digital circuits offer a great deal of computation. As technology evolves and many more transistors can fit in a given area, the concern for power dissipation as heat arises. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where K=1.3806505*10-23m2kg-2K-1 (joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. Also, according to Moore's law, the number of transistor elements doubles roughly every two years and if this trend continues to hold, in the near future more and more energy will be lost due to bit erasures and cooling than doing computations. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. Reversible circuits are those circuits that do not lose information.

Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design, optical computing, nanotechnology and quantum computing. The most prominent application of reversible logic lies in quantum computers. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as

AND or OR are clearly irreversible).Thus, Quantum Arithmetic must be built from reversible logical components [3]. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa. In the reversible circuits, there is a one-to-one mapping between input and output vectors.

In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2]. Since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Furthermore, voltage-coded logic signals have energy of Esig = ½CV^2, and this energy gets dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology. It has been shown that reversible logic helps in saving this energy using charge recovery process [4].

Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless. Thus, an NXN reversible gate can be represented as

Iv= (I1, I2, I3, I4,…….……IN)
Ov= (O1, O2, O3,……..…….ON).

Where Iv and Ov represent the input and output vectors respectively.

II. REVERSIBLE FREDKIN, TOFFOLI & TSG GATES

The reversible TSG, Fredkin & Toffoli gates are used for implementation of carry select and bypass adders. In this paper first the TSG, Fredkin & Toffoli gates are simulated using Tanner tool and then these blocks are used for designing adders**.**

A. FREDKIN gate

Fig 1 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is defined by P=A, Q=A'B ⊕AC and R=A'C ⊕AB. Quantum cost of a Fredkin gate is 5.

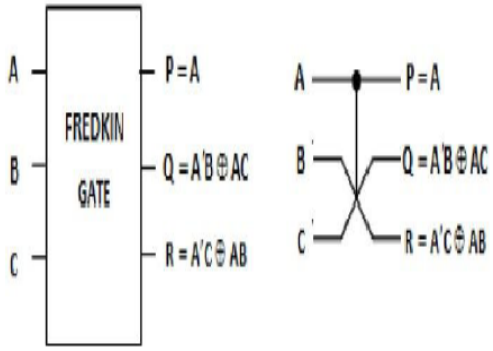

Fig 1 Fredkin gate[6]

B. TOFFOLI gate

Fig 2 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O (P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

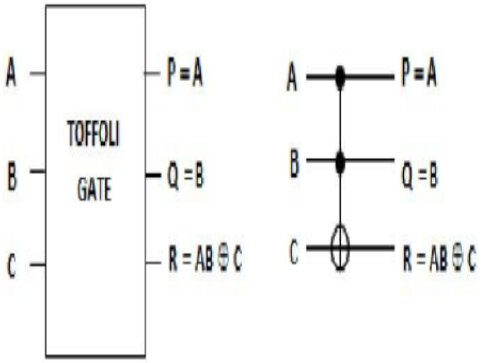

Fig 2 Toffoli gate [6]

C. TSG gate

The reversible 4*4 TSG gate block diagram is shown in Fig. 1.The input vector I (A, B,0,Cin) and the output vector is O (A, A⊕B**,** Sum, Cout).

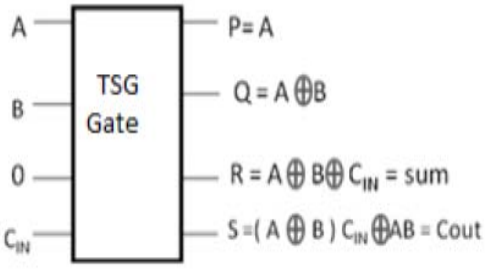

Fig 3 TSG Gate as Reversible Full Adder [5]

III. CARRY BYPASS ADDER

The block diagram of carry bypass adder is as shown in fig.4.In 4 bit carry bypass adder four full adders and one multiplexer is used. The selection line for

multiplexer is obtained from product of propagation constants of the inputs. Propagation constant is nothing but the ex-or operation of the inputs. If the product of all propagation constants are is 1 then the carry output is directly selects from input carry. If the product of all propagation constants are is 0 then the carry output selected by multiplexer is from the output of last full adder. So here is multiplexer is used for bypass the carry. The hardware cost of bypass adder is less. The area occupied is given as $O(n^2)$ and delay is $O(n\wedge\frac{l}{l+1})$ and the product of area and delay is given as $O(n\wedge\frac{l+2}{l+1})$.

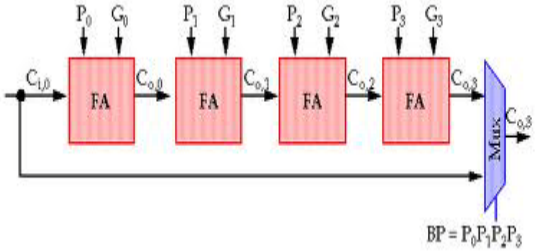

Fig. 4 Carry bypass adder structure

IV. CARRY SELECT ADDER

The block diagram of carry select adder is as shown in fig.5.In 4 bit carry select adder four full adders and five multiplexers are used. The reason for going to carry select adder is to reduce delay. The input carry is given as common selection line for all multiplexers. In this two ripple carry adders are used. For first RCA input carry taken as 0 and for second RCA input carry taken as 1. The area of carry select adder is more because of two RCAs are used. The sum output selected by the multiplexer is depending on carry of input data. If Cin is 0 the sum output selected by multiplexer is from first RCA and if Cin is 1 the sum output selected by multiplexer is from second RCA. The area occupied is given as O(n log n) and delay is O(log n) and the product of area and delay is given as $O(n \log n^2)$.

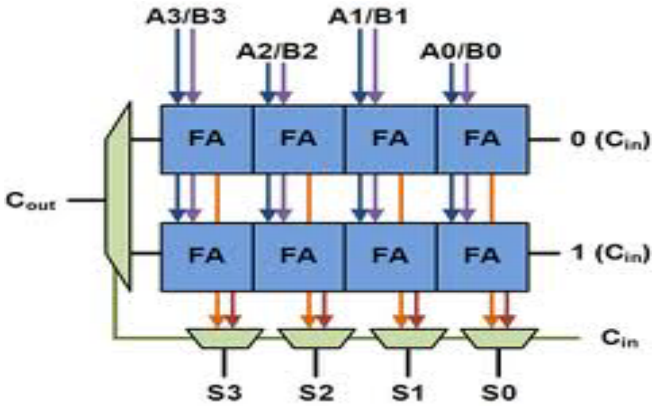

Fig 5 carry select adder structure

V. SIMULATION RESULTS USING REVERSIBLE LOGIC

A. *TSG gate*

TSG gate work as a reversible full adder with two garbage outputs. When implementing TSG as a reversible full adder, zero is passed to its third input which reduces the computation complexity at the output of TSG, to make it work as a full adder. Thus, directly implementing TSG as a reversible full adder will lead to transistor overhead. This overhead can be reduced by carefully examining the transistor implementation of TSG gate, and removing those transistors which are not involved in the computation, when TSG is working as reversible full adder. The optimized structure of TSG gate working singly as a reversible full adder is shown in Fig. 6 which is implemented with only 18 transistors thus avoiding the transistor overhead. This technique will also significantly reduce the transistor overhead when realizing the reversible circuits.

B. *Carry bypass adder*

The carry bypass adder using reversible gates is obtained with four TSG gates, three TOFFOLI gates and one FRDKIN gate. The propagation constants are directly obtained from second output of TSG gate. To multiply these propagation constants three TOFFOLI gates are needed. Each three input TOFFOLI gate serves as AND operation of two inputs by making third input as '0' with two garbage outputs. The three input FREDKIN gate serves as multiplexer with two garbage outputs. The simulation setup for carry bypass adder using transistor realization is as shown in fig.7

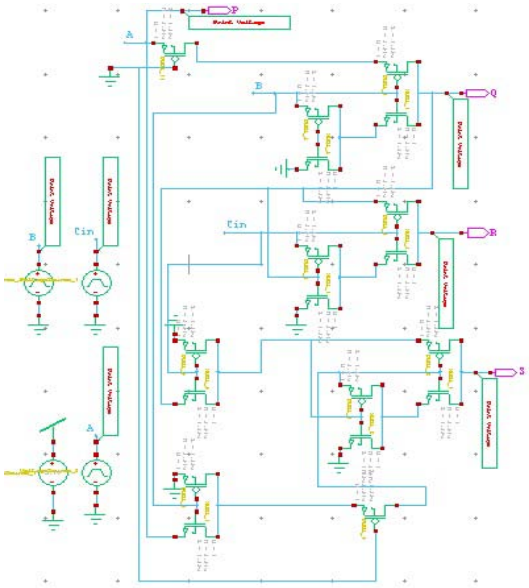

Fig.6 Simulation setup for TSG gate

Table 1 simulation parameters of full adder

GATE	Delay(ns)	Raise time(ns)	Fall time (ns)	Power (mw)
TSG	0.3216	0.01462	0.08742	3.98

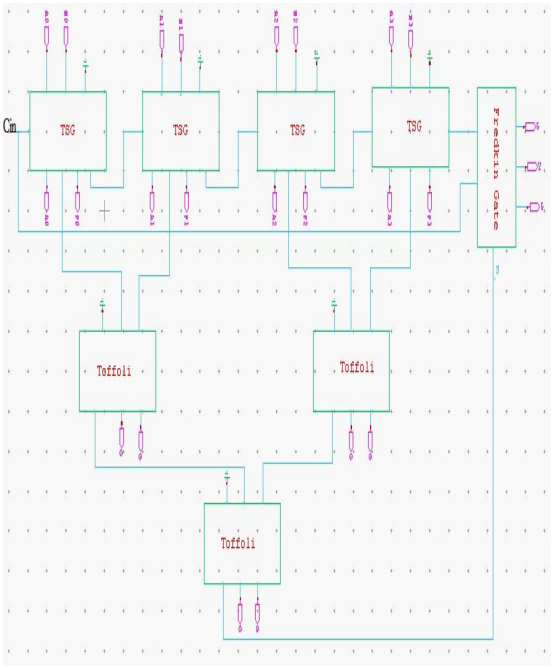

Fig.7 Simulation setup for carry bypass adder

Table 2 simulation parameters of carry bypass adder

GATE	Delay(ns)	Raise time(ns)	Fall time (ns)	Power (mw)
4TSG+3 Toffoli+1 Fredkin	41.265	0.15785	0.13421	4.01

C. Carry select adder

The carry select adder using reversible gates is obtained with eight TSG gates and five FRDKIN gates. The three input FREDKIN gate serves as multiplexer with two garbage outputs. The simulation setup for carry select adder using transistor realization is as shown in fig.8

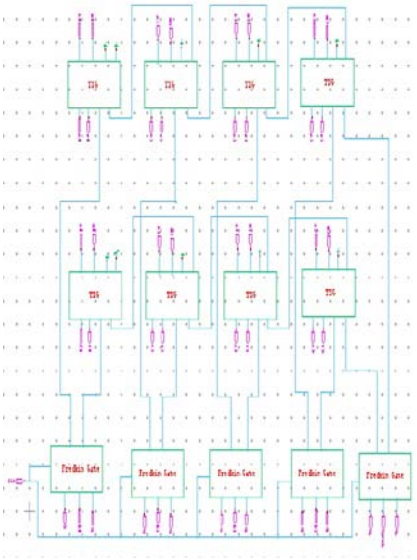

Fig.8 Simulation setup for carry bypass adder

Table 3 simulation parameters of carry select adder

GATE	Delay(ns)	Raise time(ns)	Fall time (ns)	Power (mw)
8TSG+5Fredkin	40.856	0.125621	0.10514	4.25

VI. NEW REVERSIBLE GATES

In this paper four new reversible gates are proposed and named as (New Reversible Gate) NRG1, NRG2, NRG3, and NRG4. The functionality description and truth table are described below. 'g' represents the GARBAGE at the output.

A. NRG1 gate

The reversible 4*4 NRG1 gate block diagram is shown in Fig. 9.The input vector I (A, 0, C, D) and the output vector is O (A,$\overline{C+D}$, $\overline{C \oplus D}$,$\overline{D}$). In this make the input B to 0 then we will get at the output as one NOR, EX-NOR and NOT gate operations of the input bits.

Table 4 Truth table for NRG1 gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	1	1	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	1	1	0	1

0	1	1	1	0	1	1	0
1	0	0	0	1	1	1	1
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	1
1	0	1	1	1	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	0

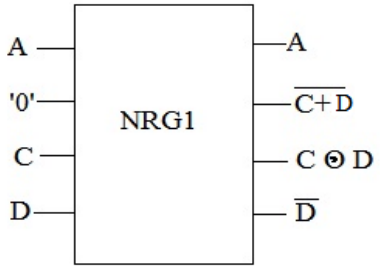

Fig.9 Proposed NSG1 gate

B. NRG2 gate

The reversible 4*4 NRG2 gate block diagram is shown in Fig. 10.The input vector I (A, B, C, D) and the output vector is O (g, g, $\bar{A}(\overline{C \oplus D}) + A(C \oplus D)$, g).In this gate the third output of reversible gate can be used as output of 2*1 MUX .Where the input A acts as selection line and the two inputs are EX-OR and EX-NOR operations.

Table 5 Truth table for NRG2 gate

A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**
0	0	0	0	0	1	1	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	0
1	0	0	0	1	1	0	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	1
1	1	1	1	1	1	0	0

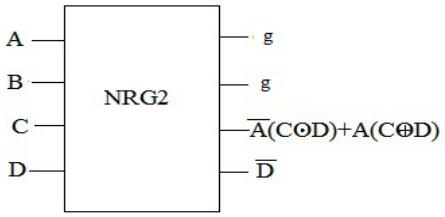

Fig.10 Proposed NSG2 gate

C. NRG3gate

The reversible 4*4 NRG3 gate block diagram is shown in Fig. 11.The input vector I (A, 1, C, D) and the output vector is O (A, CD**,** $C \oplus D$, $\bar{D}$). In this gate the second input B always connects to V_{dd} (logic 1). Then the outputs of gate are obtained as SUM and CARRY of half adder and one NOT operation.

Table 6 Truth table for NRG3 gate

A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**
0	0	0	0	0	1	0	1
0	0	0	1	0	1	1	0
0	0	1	0	0	1	1	1
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	1
1	1	1	1	1	1	0	0

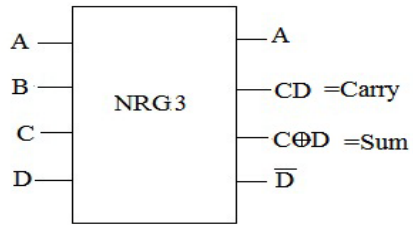

Fig.11 Proposed NSG3 gate

D. NRG4 gate

The reversible 4*4 NRG4 gate block diagram is shown in Fig. 12.The input vector I (A, B, C, D) and the output vector is O (g, g, g, $\overline{A \oplus B \oplus C \oplus D}$).In this the fourth output can be used as the parity error check. The remaining three outputs are garbage outputs.

Table 7 Truth table for NRG4 gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0
1	1	0	0	1	1	0	1
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1	1	1	1	1	1	1	1

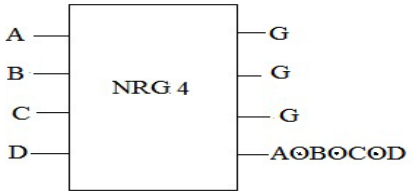

Fig.12 Proposed NSG4 gate

VII. CONCLUSION

The focus of this paper is on transistor Implementation of reversible 4*4 TSG & Fredkin gate, Toffoli gate to design the Four bit Carry bypass Adder and carry select adder. Adder architectures using the proposed TSG, Fredkin gate, Toffoli gate is consuming less power. And also four new reversible gates are proposed to perform various functions.

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