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Design and Analysis of Integrated Electronic Ballast for HID Lamps Featuring HPF

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***Abstract:** This paper proposes high-power-factor electronic ballast for metal-halide (MH) lamps. In the proposed circuit, two buck–boost converters and a buck converter are integrated with a full-bridge inverter by sharing the four active switches of the full-bridge inverter. Two active switches are switched at high frequencies, while the other two are switched at lower frequencies. The buck converter is used to step down the DC-link voltage of the full-bridge inverter and filter out the high-frequency components to drive lamps with a low-frequency square-wave (LFSW) current. The buck–boost converters are operated at discontinuous-conduction mode to perform the function of power-factor correction (PFC) to ensure almost unity power factor at the input line. By tactful arrangement of diodes, the DC-link capacitors are discharged in parallel; this helps to operate the high-frequency active switches at a high duty ratio, achieving a small peak value of the PFC-converter current and correspondingly smaller conduction losses. Detailed operation modes and the design equations are provided. Prototype electronic ballast for a 70 W MH lamp is built and tested. Experimental measurements have proven that the proposed electronic ballast has the advantages of high-power factor and being free of acoustic resonance. By integrating the active switches of the converters and the inverter, the proposed electronic ballast is advantageous in terms of cost-effectiveness and high energy-conversion efficiency.*

1 INTRODUCTION

Owing to the benefit of high luminous efficacy, high-intensity-discharge (HID) lamps have become an attractive lighting source. Although metal-halide (MH) lamps have the shortest life among various kinds of HID lamps, they are widely used in industrial and outdoor applications because of their advantages of compact size, high luminous efficacy (>85 l m/W) and good colour rendition (colour rendering index Ra > 85) [1–3]. Since the MH lamp presents the characteristics of negative incremental reactance, it requires a ballast to stabilize the lamp current. Conventionally, electromagnetic ballasts, which use line-frequency inductors to limit the lamp current, have been utilized because of the advantages of low cost, simplicity and high reliability. However, the electromagnetic ballasts have several drawbacks, such as bulky size, heavy weight, low-efficiency, poor power regulation, and high sensitivity to changes in supply voltage. Recently, traditional electromagnetic ballasts have gradually been replaced by electronic ballasts that are operated at high frequencies and so have the advantage of small size, light weight and high energy-conversion efficiency over their electromagnetic counterparts.

However, MH lamps driven by high-frequency voltage may suffer from problematic acoustic resonance. Acoustic resonance is a physical phenomenon that is related to pressure-wave propagation in the discharging tube of the lamp. This phenomenon can result in an unstable arc, flickers, extinguishment, or even worse, lamp damage and sometimes lamp explosion [4–6]. Many approaches have been proposed to eliminate acoustic resonance; among them, driving MH lamps with a low-frequency square-wave (LFSW) current has been considered the most effective [7–10].

On the other hand, in order to comply with the more stringent regulations on current harmonics, such as the IEC61000-3-2 class C standards, electronic ballasts require an additional power-conversion stage, referred to as the power-factor-correction (PFC) stage. Hence, electronic ballasts for driving MH lamps may consist of three stages, which are: (1) PFC stage; (2) DC-to-DC conversion stage; and (3) full-bridge inverter stage. The PFC stage is used to shape the input current to be sinusoidal and in phase with the input-line voltage to achieve high-power factor (HPF) and to reduce the total harmonic distortion (THD_i) of current at the input line. It also provides a constant DC-link voltage to the second stage. A boost or buck–boost converter usually serves as the PFC stage in which the output voltage is always higher than the rated value of lamp voltage. Therefore, the second stage is usually a DC-to-DC buck converter used to step down the DC-link voltage in order to comply with lamp voltage standards and to regulate the lamp power. The final stage is a full-bridge inverter, the active switches of which operate at low switching frequencies to drive the MH lamp with LFSW current. Such three-stage electronic ballasts can ensure HPF and drive the MH lamps with LFSW current to avoid acoustic resonance. However, each stage incurs losses in the energy-conversion process and this limits the overall circuit efficiency. Moreover, each stage requires independent active switch (es) and corresponding control circuits.

To reduce the product cost of the electronic ballast, some two-stage and single-stage approaches have been developed [9–16]. Among them, some single-stage electronic ballasts drive MH lamps at high switching frequency. In order to prevent the acoustic resonance, additional real-time detection and frequency-shift circuits are required [13, 14]. References [15] and [16] successfully integrated all three stages and proposed a single-stage solution, in which a buck converter or a boost converter is adopted as the PFC stage. For a buck converter, HPF can be achieved only when its DC output voltage is much smaller than the amplitude of the AC input voltage. Generally, HPF and low THDi can be easily achieved by operating a boost-PFC stage at transition mode (TM). However, in the integrated circuits, operating the PFC stages at TM is unfeasible since the active switches are integrated and should be operated at constant frequencies. A boost converter operating at a constant frequency and in discontinuous-conduction mode (DCM) can obtain unity power factor, provided that its DC output voltage is much higher than the amplitude of the AC-input voltage.

To lower the product cost and improve the circuit efficiency, this paper proposes novel electronic ballast that integrates two buck–boost converters, a buck converter and a full-bridge inverter into a single power-conversion stage. A prototype circuit designed for a 70 W MH lamp was built and tested to verify the analytical predictions.

II CIRCUIT CONFIGURATION AND OPERATION

Fig. 1 shows the proposed electronic ballast that originates from a full-bridge inverter. MOSFETs S1–S4 is active switches of the full-bridge inverter. Diodes D1–D4 represents their intrinsic body diodes. There are two buck–boost converters to perform the function of PFC. PFC1 consists of D5, D7, S1, inductor L1 and DC-link capacitor C1. PFC2 consists of D6, D8, S4, inductor L2 and DC-link capacitor C2. PFC1 operates in the positive half-cycle of the input line voltage, while PFC2 operates in the negative half-cycle. Since PFC1 and PFC2 never simultaneously conduct current, L1 and L2 have the same inductance and can exist as two windings in one magnetic core. The buck converter consists of inductor Lb, capacitor Cb and switches S1–S4. Actually, it complies with the operation of the full-bridge inverter to perform as a bidirectional buck converter.

The arrangement of diodes D9, D10 and D11 makes C1 and C2 be discharged in parallel. In this way, the input voltage of the buck converter is only half of the DC-link voltage. At a constant output voltage, the duty ratio of the active switch of the buck converter is high at a low-input voltage and vice versa. It is noted that the active switches are shared. For a constant level of output power, operating PFC1 and PFC2 at a high duty ratio results in a small peak value of the inductor current and is advantageous as far as yielding smaller conduction losses. An igniter and the transformer T1 generate high-voltage to start up the lamp. The small low-pass filter, Lm and Cm, is used to remove the high-frequency current harmonics that occur at the input line.

MOSFETs S1–S4 are controlled by four gated voltages, vgs1–vgs4, respectively. Fig. 2 illustrates their time sequence. As shown, vgs2

and vgs3 are synchronous with the AC-input voltage and are low-frequency rectangular waveforms. In the vicinity of the zero-crossing of the AC-input voltage, there is a short dead time between vgs2 and vgs3, which prevents S2 and S3 from simultaneously conducting current. On the contrary, vgs1 and vgs4 are high-frequency rectangular-wave voltages when vgs3 and vgs2 are at highvoltage levels, respectively.

Although the active switches are shared by the PFC converters and the bidirectional buck converter, the characteristics of buck–boost converter and buck converter should be retained. In other words, the PFC-converter currents (ip1 and ip2) should charge the DC-link capacitors. They cannot directly enter the buck converter. Therefore, ip1 and ip2 should be designed to decrease to zero before the buck-converter current ib does during the time when S1 or
S4 is off. The circuit parameters should be well designed to meet this requirement. Otherwise, as soon as ib reaches zero, ip1 will flow through L1, C1, D10, C2, D3, Cb, Lb, vin and D5, or ip2 will flow through L2, D6, vin, Lb, Cb, D2, C1,

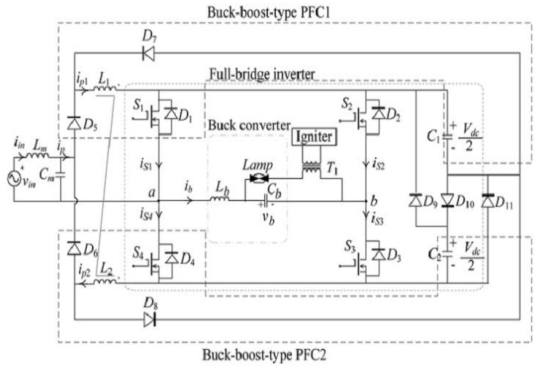

Fig. 1 Proposed electronic ballast for MD lamp

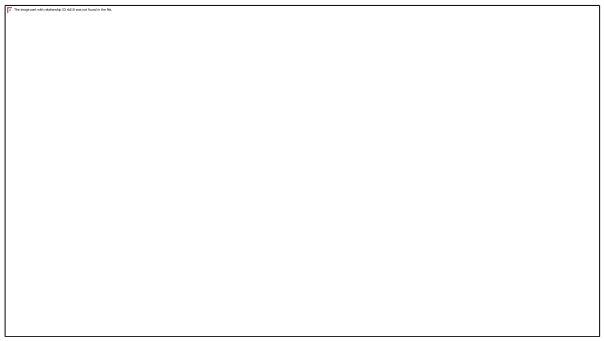

Fig. 2 Time sequence of gated voltages

D10 and C2. If these undesired current loops exist, PFC1 and PFC2 no longer perform as buck–boost converters, which will hinder the circuit from achieving HPF. Another design constraint is that the voltages across C1 and C2 (Vdc/2) should be higher than the amplitude of the input voltage to make PFC1 and PFC2 perform as buck–boost converters. If not, when S1 (S4) is turned off, the input voltage will keep supplying ip1 (ip2) to charge C1 and C2 via D10, D4 (D1) and D5 (D6), which means that PFC1 and PFC2 perform as boost converters. Besides, in order to achieve HPF and output LFSW voltage to drive an MH lamp, the PFC converters and the bidirectional buck converter are designed to operate at DCM.

The proposed electronic ballast has a symmetrical circuit topology. At steady state, the circuit operation can be divided into four modes in each high-frequency cycle. For simplifying the circuit analysis, the lamp igniter and transformer T1 are omitted, and the MH lamp is represented by its equivalent resistance, Rlamp. The operation modes in the positive half-cycle of the input line voltage and those in the negative half-cycle are similar, except that the reactive components and the active switches of the PFC1 and PFC2 converters are interchanged. Thus, only the operation modes in the positive half-cycle of the line voltage are discussed. Fig. 3 shows the operation modes, and Fig. 4 illustrates the theoretical waveforms for each mode. The circuit operation is described as follows.

2.1 Mode I (t0 < t < t1)

Mode I begins at the instant of turning on switch S1. In this mode, S3 is also ON. There are two current loops. One is the PFC-converter current ip1 flowing through vin, Lm, Cm, D5, L1 and S1. The other is the buck-converter current ib, which is supplied by C1 and C2 and then flows through S1, Lb, Cb, S3, D9 and/or D11. The voltage across L1 is equal to the rectified input voltage. Since the PFC converter is designed to operate at DCM, ip1 increases linearly from zero with a rising slope that is proportional to the rectified

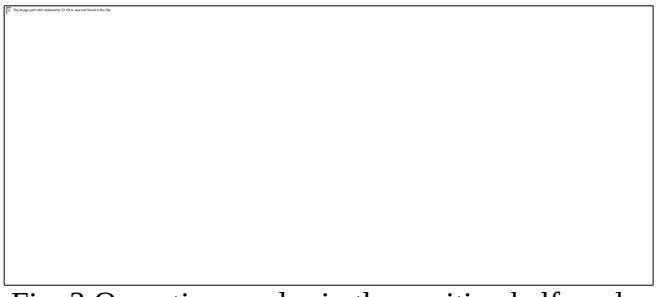

Fig. 3 Operation modes in the positive half-cycle of the line voltage

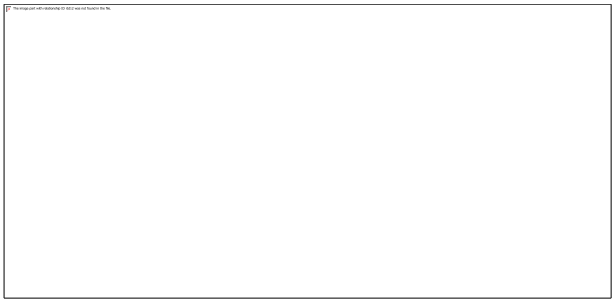

Fig. 4 Theoretical waveforms

input voltage. As shown in Fig. 1, the current from the low-pass filter ip is equal to ip1 in this mode. Concerning the buck-converter current, the voltage across Lb is equal to Vdc/2 minus vb. The buck converter also operates at DCM, thereby, ib rises from zero.

Mode I end when S1 is turned off. There could be two different operation modes following Mode I, depending on the state of S3. When S3 is kept ON, the circuit operation enters Mode II-A. Contrarily, in the dead time between vgs2 and vgs3, both S1 and S3 are OFF and the circuit operation will enter Mode II-B.

2.2 Mode II-A (t1 < t < t2)

Mode II-A begins as soon as S1 is turned off. In order to maintain the flux balance in L1, current ip1 freewheels through D7 to charge C1. Since Vdc/2 is designed to be higher than the amplitude of the input voltage, D5 is reverse-biased. Current ip is zero. On the other hand, current ib keeps flowing through Lb, Cb, S3 and D4. The voltages across L1 and Lb are equal to − Vdc/2 and − vb, respectively. Therefore both currents decrease linearly.

2.3 Mode II-B (t1 < t < t2)

Both S1 and S3 are OFF. The current loop of ip1 is as same as that in Mode II-A. The only difference between Mode II-B and Mode II-A is the current loop of ib. In this mode, ib freewheels through Lb, Cb, D2, D4 and D10 to charge capacitors C1 and C2. The voltage across Lb is equal to − Vdc − vb. Hence, ib decreases faster than it does in Mode II A.

2.4 Mode III-A (t2 < t < t3)

As stated above, ip1 is designed to decrease to zero before ib does. The circuit operation enters this mode after Mode II-A as soon as ip1 become zero. Only ib and the lamp current keep flowing. When ib becomes zero, the circuit operation enters Mode IV.

2.5 Mode III-B (t2 < t < t3)

The circuit operation enters this mode after Mode II-B as soon as ip1 becomes zero. Only ib and the lamp current keep flowing. When ib becomes zero, the circuit operation enters Mode IV.

2.6 Mode IV (t3 < t < t4)

During this mode, only the lamp current supplied from Cb exists. When vgs1 goes back to a high level to turn on S1 again, the circuit operation returns to Mode I of the next high-frequency cycle.

III CIRCUIT ANALYSES

For simplifying the circuit analysis, the following assumptions are made:

1. All the circuit components are ideal.
2. Since the capacitances of C1 and C2 are large enough, the DC-link voltage Vdc can be regarded as a constant voltage source.
3. The capacitance Cb is large enough that the voltage vb remains constant during the high-frequency switching cycle.
4. The lamp is regarded as an open circuit before ignition and a pure resistor at the steady state.

Based on the circuit operation described in Section 2, the currents flowing in the PFC converter and the bidirectional buck converter do not interfere with each other even though some active switches are shared. The features of the buck– boost converter and the buck converter can be retained. Therefore, the PFC converter and the buck converter can be analysed separately.

3.1 PFC Converter

Based on the discussion of operationmodes, the PFC converters perform as buck–boost converters. The PFC converters are supplied by the AC line voltage source given by

$$v_{in}(t) = V_m \sin(2\pi f_L t) \quad (1)$$

where fL and Vm are frequency and amplitude of the input voltage, respectively. In practice, fL is much lower than the high switching frequency, fs, of S1 and S4. It is reasonable to consider the rectified input voltage as a constant over a high-frequency cycle. Since the buck–boost converters are operated at DCM over an entire line-frequency cycle, ip1 rises from zero at the beginning of Mode I and reaches its peak at the end of Mode I. The waveform of ip, ip1 and ip2 are conceptually shown in Fig. 4. The expanded waveform of ip1 in high-frequency cycles are illustrated in Fig. 5. The

peak values of ip1 form the positive half-cycle of a sinusoidal waveform, and can be expressed as

$$i_{p1,peak}(t) = \begin{cases} \dfrac{V_m \sin(2\pi f_L t) DT_s}{L_1} & 0 \le 2\pi f_L t < \pi \\ [redacted] & \end{cases} \quad (2)$$

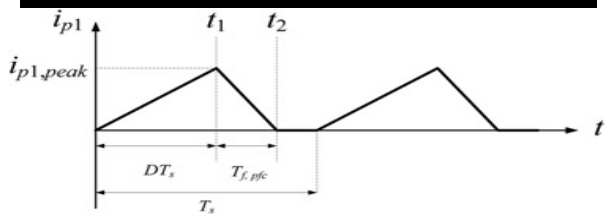

Fig. 5 Theoretical waveforms of ip1 in high-frequency cycles

where Ts and D are the switching period and duty ratio of S1 and S4, respectively. When S1 is OFF, the voltage across L1 is −Vdc/2. The duration of the interval during which ip1 decreases from the peak value to zero is

[redacted]

From the theoretical waveforms shown in Fig. 4, ip is equal to ip1 when S1 is ON and ip is zero when S1 is OFF in the positive half-cycle of the input voltage. In contrast, ip is equal to ip2 when S4 is ON and ip is zero when S4 is OFF in the negative half-cycle. Therefore the peak values of ip form a sinusoidal envelope

$$i_{p,peak}(t) = \frac{V_m \sin(2\pi f_L t) DT_s}{L_1} \quad (4)$$

The high-frequency contents of ip can be removed by Lm and Cm. Then, the input current iin will be equal to the average of ip over a high-frequency cycle, as follows

[redacted]

Equation (5) reveals that the input current is sinusoidal and in phase with the input line voltage if the duty ratio remains constant over an entire line cycle. As a result, HPF can be achieved. The input power can be determined by taking an average of its instantaneous value over one line-frequency cycle, as follows

[redacted]

Then, the lamp power can be calculated

[redacted]

where η represents the circuit conversion efficiency.

To operate the buck–boost converter at DCM, the following inequality equation should be met

[redacted]

From (8), Vdc should be designed to be high enough to ensure DCM operation over an entire input line-frequency cycle, as follows

[redacted]

3.2 Bidirectional buck converter

According to the discussion of circuit operation in Section 2, S1–S4, Lb and Cb form a bidirectional buck converter. The inductor Lb and capacitor Cb are used to filter out the high-frequency components of the inverter voltage vab. Then, the voltage across Cb is an LFSW waveform. During the positive half-cycle of the input line voltage, S2 and S4 are OFF; S3 is kept ON and S1 is turned on and off at higher frequencies. In contrast, during the negative half-cycle of the line voltage, S1 and S3 are OFF; S2 is kept ON and S4 is turned on and off at higher frequencies. The operations during the positive half-cycle and the negative half-cycle of the input line voltage are similar except that the polarities of ib and vb are reversed. Here, only the circuit operation during the positive half-cycle is discussed.

Neglecting the winding resistance of transformer T1, vb is equal to the lamp voltage, Vlamp. When S1 and S3 are ON, the voltage across inductor Lb is

[redacted]

Current ib rises from zero and will reach a peak value at the instant of turning off S1. Its peak value is equal to

[redacted]

When S1 is turned off, ib freewheels through diode D4. The voltage across Lb is

[redacted]

This negative voltage causes ib to decrease. The duration of the interval during which ib decreases from the peak value to zero is given by

$$T_{f,buck} = \frac{\left((V_{dc}/2) - V_{lamp}\right) DT_S}{V_{lamp}} \quad (13)$$

As can be seen in Fig. 4, ib is a triangular waveform in the high-frequency cycle. Its average is expressed as

$$\overline{i_b} = \frac{\left(V_{dc} - 2V_{lamp}\right)V_{dc}D^2T_S}{8L_bV_{lamp}} \quad (14)$$

At steady-state operation, the average value of ib is equal to lamp current, as follows

$$\overline{i_b} = \frac{V_{lamp}}{R_{lamp}} \quad (15)$$

Combining (14) and (15), Lb can be calculated as

$$L_b = \frac{\left(V_{dc} - 2V_{lamp}\right)V_{dc}D^2T_SR_{lamp}}{8V_{lamp}^2} \quad (16)$$

For fulfilling DCM operation, Tf,buck is expressed in (13) and should be shorter than (1 − D)Ts. This leads to

$$V_{dc} \le \frac{2V_{lamp}}{D} \quad (17)$$

IV PARAMETERS DESIGN

An electronic ballast for a 70-W MH lamp is illustrated as a design example. Table 1 lists the circuit specifications. The input voltage is 110Vrms ± 10%. In the proposed electronic ballast, the active switches cannot operate at zero-voltage switching (ZVS). For reducing the switching losses, the switching frequency of S1 and S4 cannot be too high. In this illustrative example, the switching frequency of S1 and S4 is 40 kHz while that of S2 and S3 is 60 Hz. The lamp voltage and current at the rated power are 90 V and 0.78 A, respectively.

The design considerations are detailed as follows.

Table 1 Circuit specifications

Input line voltage, v_{in}	$110V_{rms}$ ± 10%, 60 Hz
high switching frequency, f_{S1} and f_{S4}	40 kHz
low-switching frequency, f_{S2} and f_{S3}	60 Hz
lamp power, P_{lamp}	70 W
lamp voltage, V_{lamp}	90 V
lamp current, I_{lamp}	0.78 A
lamp equivalent resistance, R_{lamp}	115.7 Ω

4.1 Determine DC-link voltage Vdc and duty ratio D

As stated above, in order to design the PFC converter to operate as a buck–boost converter, the voltage across each of the DC-link capacitors should be higher than the amplitude of the input voltage, as follows

$$\frac{V_{dc}}{2} \ge V_m \quad (18)$$

Also, the PFC-converter current should decrease to zero before the buck-converter current does, that is

$$T_{f,pfc} \le T_{f,buck} \quad (19)$$

From (3), (13) and (19), the following inequality is derived

$$V_{dc} > V_{lamp} + \sqrt{V_{lamp}^2 + 4V_mV_{lamp}} \quad (20)$$

The circuit parameters are designed for an input voltage of 110 Vrms ± 10%; that is, the range of the amplitude is 140–171 V. Using (9), (17), (18) and (20), the boundary curves of Vdc with respect to duty ratio are obtained. The boundary curves at the highest level of the input voltage (Vm = 171 V) are shown in Fig. 6a, whereas those at the lowest level (Vm = 140 V) are shown in Fig. 6b. The slash regions can meet the design requirement. From Fig. 6a, the duty ratio should be less than 0.51 and Vdc should be higher than 354 V. It is noted that Vdc should be chosen to be as low as possible to reduce the voltage stresses and switching losses on the active switches. In this design example, Vdc is chosen to be

Vdc= 360(V)

The PFC converters operate at DCM. A small duty ratio always results in high peak current as well as higher conduction losses. Thus, it is better to operate the active switches at a higher duty ratio. Nevertheless, designing the duty ratio at the rated input voltage and the rated lamp power should consider both variations of the input voltage and the lamp power. The PFC converters and the buck converter share the active switches S1, and S4, of which the duty ratio is used to control the input power and thereby control the lamp power. It loses the freedom of independently regulating the DC-link voltage and the lamp current. In the proposed circuit, there is a feedback loop for obtaining a fixed value of Vdc, but not a lamp-current feedback loop. From (7), the duty ratio is inversely

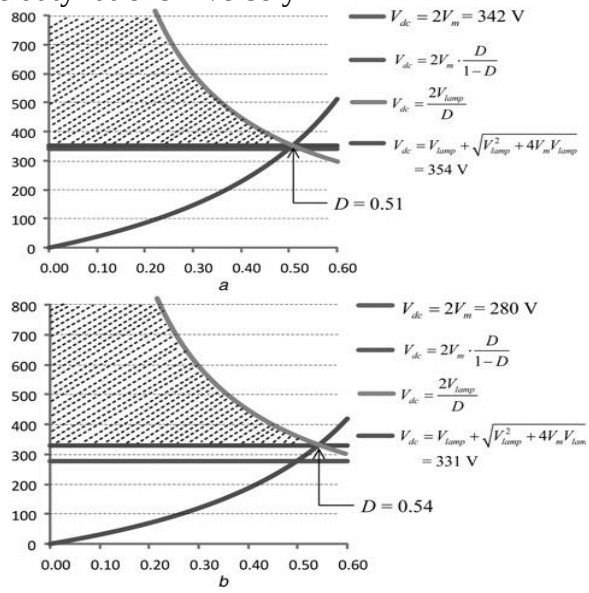

Fig. 6 Boundary curves of Vdc versus duty ratio a Vm = 171 V, Vlamp = 90 V and b Vm = 140 V, Vlamp = 90 V

proportional to the input voltage at a constant lamp power. The lower the input voltage, the

higher the duty ratio. From Fig. 6a, the applicable duty ratio is 0.51 maximum. Considering the input voltage variation of 10%, the duty ratio for operating the circuit at rated input voltage (110Vrms) and the rated lamp power (70 W) is designed to be D = 0.45

4.2 Calculate L1, L2 and Lb

Using (7) and (16) and assuming 85% circuit efficiency, L1, L2 and Lb are calculated to be

L1 = L2 = 0.37(mH), Lb = 0.59(mH)

4.3 Calculate Cb

To prevent the occurrence of acoustic resonance, the energy caused by the lamp's current ripple should be small. This means Cb must be large enough to reduce the lamp's voltage ripple, and hence, reduce the current ripple. The ripple of the lamp voltage is expressed as [17]

$$\frac{\Delta V_{\text{lamp}}}{V_{\text{lamp}}} = \frac{(1-D)T_S^2}{8L_bC_b} \times 100\% \qquad (21)$$

For designing a voltage ripple of 10%, Cb is calculated to be 0.73 uF. The larger the value of Cb, the lower the voltage ripple. However, the lamp voltage changes polarity during every low-frequency cycle. In the transient time for Cb tochange polarity, a high-value Cb would induce higher transient current and longer transient time for charging Cb to a stable value. High transient current results in the use of active switches of high-current rate as well as more conduction loss. There should be a compromise between having a low-voltage ripple and a low transient current. Here, Cb is chosen to be Cb = 0.8 (mF)

4.4 Determine Lm and Cm

Lm and Cm are used to filter out the high-frequency components of ib. By rule of thumb, Lm and Cm are designed as a low-pass filter with a natural frequency about one eighth of the switching frequency. Lm and Cm are determined to be Lm = 1.6 (mH), Cm = 0.5 (mF)

V Experimental results

A prototype of the proposed electronic ballast was built and tested. Table 2 lists the circuit parameters. The control

Table 2 Circuit parameters

Filter inductor L_m	1.6 mH
filter capacitor C_m	0.5 μF
buck-boost inductor L_1, L_2	0.37 mH
DC-link capacitors C_1, C_2	330 μF/400 V
buck inductor L_b	0.59 mH
buck capacitor C_b	0.8 μF
active switches S_1 –S_4	IRFP460
diodes D_5 –D_{11}	MUR460
igniter	
resistor R_{ign}	8 kΩ/10 W
capacitor C_{ign}	330 nF/630 V
sidac	K2000 G
transformer T_1	turns ratio 1:30
—	secondary inductance 0.51 mH

circuit is shown in Fig. 7. It mainly consists of a microcontroller DSPIC30F4011, an igniter, a zero-crossing detector, a DC-link voltage detector and four MOSFET drivers TLP250. A square waveform in phase with the ac input voltage is generated by the zero-crossing detector and fed into the microcontroller from which four gated voltages are generated and then amplified by the gate driver. The amplified gated voltages vgs1–vgs4 are used to control the four active switches S1–S4, respectively. Also, the microcontroller monitors and regulates the DC-link voltage Vdc to control the lamp power by adjusting the duty ratio of the high-frequency gated voltages vgs1 and vgs4.

The DC-link capacitor C1 supplies the igniter, which consists of a resistor Rign, a capacitor Cign, a sidac and a step-up transformer T1, as shown in the electronic-ballast circuit. The secondary winding of T1 is connected in series with the MH lamp. Before breakdown, the lamp is nearly open-circuited. Since the PFC converters unceasingly supply energy to the DC-link capacitors, their voltages will increase up until the voltage across Cign becomes sufficiently high to trigger the sidac. Thereafter, the sidac conducts an impulse current flowing through the primary winding of T1, which results in a high voltage to ignite the lamp. After successfully igniting the lamp, the DC-link voltage drops toward a steady-state value. For preventing reignition of the lamp, the DC-link voltage for operating the lamp at the rated power level should be designed to be lower than the breakover voltage of the sidac.

Fig. 8 shows the lamp voltage and current during the starting transient. After igniting the lamp, it takes about 50 s to initiate the thermal equilibrium and to finally reach the steady-state operation with a rated lamp power. Fig. 9 shows the waveforms for the input voltage and input current. The input current is sinusoidal and in phase with the input voltage. The measured power factor is greater than 0.99 and the total current

harmonic distortion (THD) is 5.5%. The measured input power and lamp power is 80.0 and 69.6 W, respectively, and the circuit efficiency is 87%.

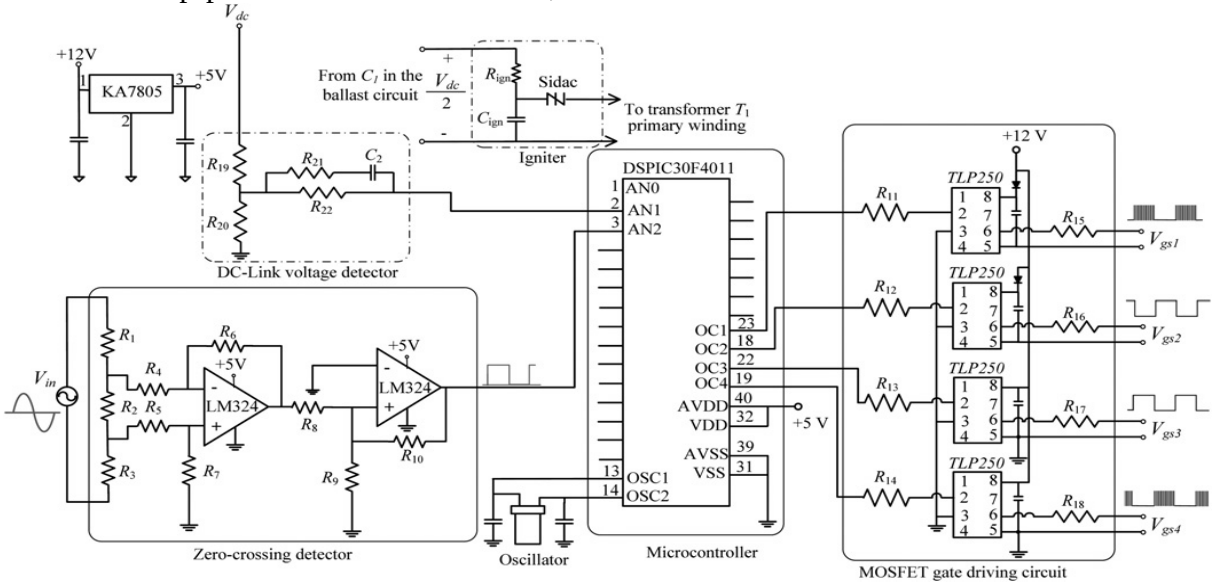

Fig. 7 Control circuit

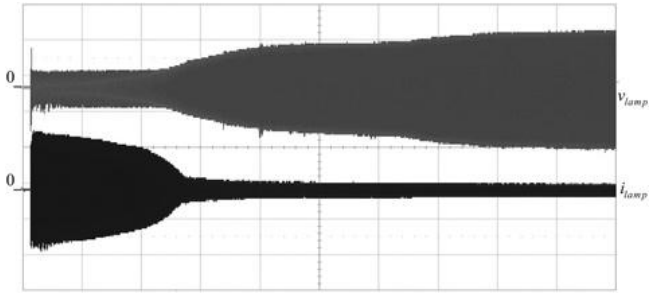

Fig. 8 Waveforms of vlamp and ilamp during starting transient (vlamp: 50 V/div, ilamp: 5 A/div, time: 5 s/div)

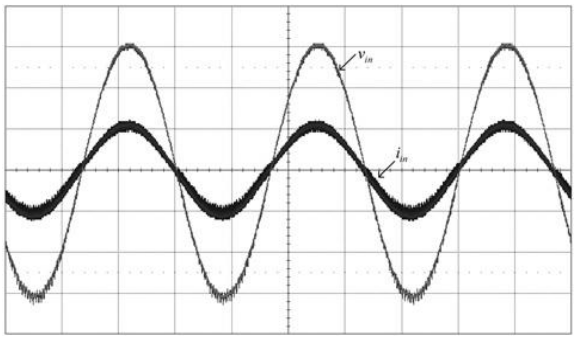

Fig. 9 Waveforms of vin and iin (vin: 50 V/div, iin: 1 A/div, time: 5 ms/div)

Figs. 10 and 11 show the inductor currents of the PFC-converter and the buck-converter, respectively. As illustrated, they all operate at DCM over the entire cycle of the line voltage. The comparison between the PFC-converter current and the buck-converter current are shown in Fig. 12. As expected, the PFC-converter current

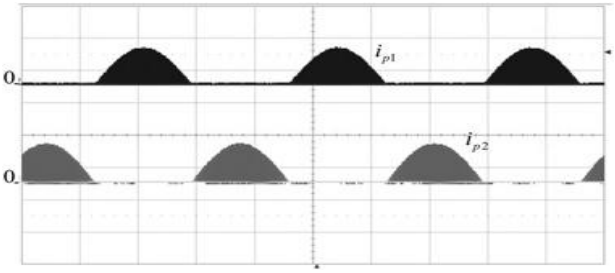

Fig. 10 Waveforms of ip1 and ip2 (current: 5 A/div, time: 5 ms/div)

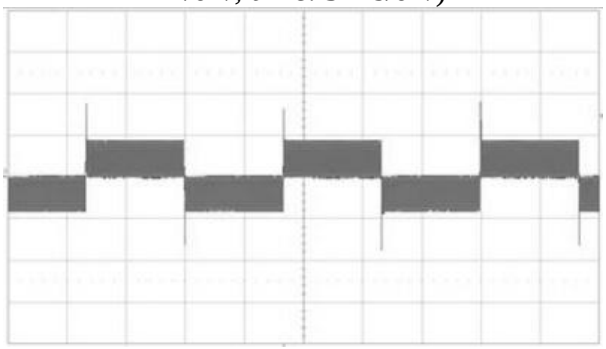

Fig. 11 Waveforms of ib (current: 2 A/div, time: 5 ms/div)

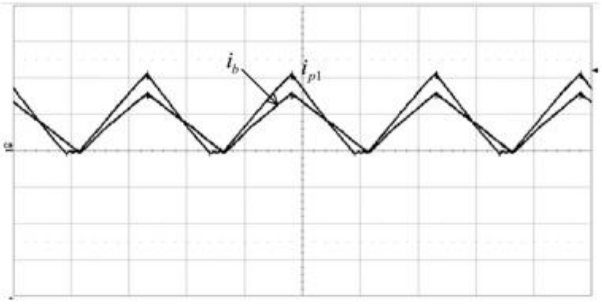

Fig. 12 Comparison of ip1 and ib (ip1: 2 A/div, ib: 1 A/div, time: 10 μs/div)

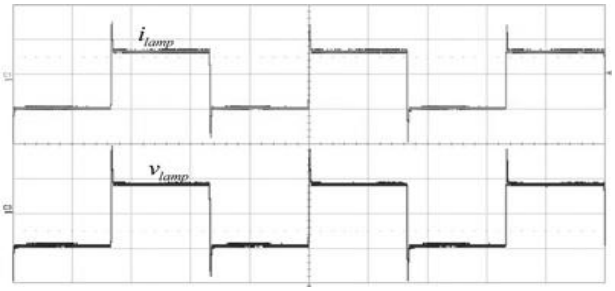

Fig. 13 Waveforms of vlamp and ilamp (voltage: 100 V/div, current: 1 A/div, time: 5 ms/div)

decreases to zero before the buck-converter current. The waveforms for lamp voltage and current, shown in Fig. 13, are 60-Hz square waveforms. The lamp current ripple is 5.7%. The lamp can operate stably, and no acoustic resonance is observed.

VI CONCLUSIONS

A novel electronic ballast for driving an MH lamp with a LFSW current is presented. The ballast has symmetrical circuit topology, and is derived by integrating two buck– boost converters, a buck converter and a full-bridge inverter. The buck–boost converters, which perform as PFC converters, are operated at DCM to achieve HPF and low current THD. The buck converter filters out high-frequency components of the output voltage of the full-bridge inverter and provides LFSW voltage to drive the MH lamp. By tactfully adding three diodes, the input voltage of the buck converter can be reduced to half of the DC-link voltage. It helps to operate the high-frequency switches at a higher duty ratio and thereby to have a PFC-converter current of smaller peak value and lower conduction losses. As compared with the three-stage electronic ballast that can achieve HPF and drive MH lamps with LFSW voltage, two active switches and two control circuits are saved. Consequently, the proposed electronic ballast is potential cost-effective product.

The circuit operations are described and the design equations are derived. A prototype circuit designed for a 70W MH lamp was built and measured to verify the theoretical analyses. Experimental results show that the electronic ballast performs satisfactorily. A nearly unity power factor (>0.99) and low THD (5.5%) can be achieved. The lamp is driven by a low-frequency (60 Hz) square-wave current to avoid the occurrence of acoustic resonance.

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