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Design of Low Power Variable Latency adder and Its Implementation in Decimation Filter

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Abstract*—In this paper, we have designed a new variable latency adder and its implementation of decimation filter. There are multiple ways to implement a decimationfilter. This filter design combination of CIC (cascaded-integrator-comb) filter and HB (half band) filter as the decimator filter to reduce the frequency sample rate conversion and detail of the implementation step to realize this design in hardware. Low power design approach for CIC filter and half band filter will be designed adder section..This adder allows works at lower power by maintaining the same throughput as well as compare the performance analysis of conventional adder. The VL-adder designed can be modified to overcome the effects of negative bias temperature instability (NBTI) on circuit delay operations..The filter is designed VHDL coding and verified using a FPGA (field programmable gate array) board and Mentor Graphics tool.*

***Keywords*—digital design, CIC filter, half-band filter, Carry select adder.**

I. INTRODUCTION

Effective Power can reduced on both dynamic and leakage power of a VLSI circuit. The critical timing pathof a VLSI circuit is rarely activated or sensitized.The VL-adder predicts the operation latency on the fly. When a long-latency operation occurs, the data capturing clock edge are shifted by one more clock cycle so that the adder output can be latched on correctly.Compared to a conventional adder design, a VL-adder can work at a much lower VDD such that the majority of operations can be processed within one clock cycle. VL-adder design for the negative bias temperature instability (NBTI) tolerance: when a chip is aging, the detection threshold of long-latency operation is automatically adjusted.

In VL-Adder is implemented in the decimation filter. Decimation filter has wide application in both the analog and digital system for data rate conversion as well as filtering. One of the most popular applications of the decimation filter is sigma-delta ADC (analog-to-digital converter) [9]. Sigma-delta ADC is widely used in audio application for very high resolution, such as CD (compact disc) player.

Conventionally sigma-delta modulator is sampled at significantly higher frequency compare to the actual frequency band where the interested signal located in. In most of the communication device, we will implement a decimator filter to reduce the data rate in order to reduce the dynamic power consumption. There are many approaches in the decimation filter implementation. i.e cascade CIC – FIR (finite impulse response) filter,multiple stage HB filter and cascade CIC – HB filter [10].In this paper, a cascade CIC – HB filter implementation is adder section to change the performance analysis between VL-Adder and Conventional Adder.

II. VL ADDER CONCEPT

There are multiple critical carry propagation paths in CSA, each of which starts from the first bit adder of every CSS, crosses the MUXes of the sequential stages, and ends at the sum generation block of the last stage. The delay of a CSA heavily depends on the input vectors.

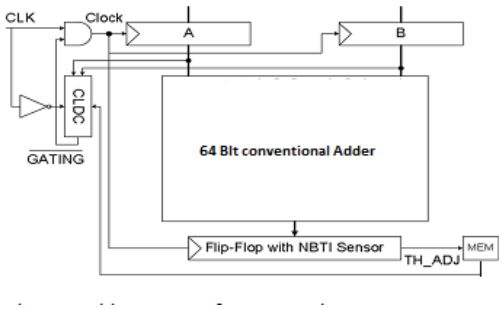

Fig 1.VL-Adder Block diagram

When long-latency operation occurs only when LONG_OP = 1. The corresponding circuit, called carry length detection circuit (CLDC), is shown in Fig. 2. When an LONG OP signal is pulled up ‘‘high,’’ a gating signal is triggered to disable the clock (Gen CLK) switching in the following clock cycle, as shown in Fig. 3. Here, signal TH ADJ is fixed at ‘‘low.’’

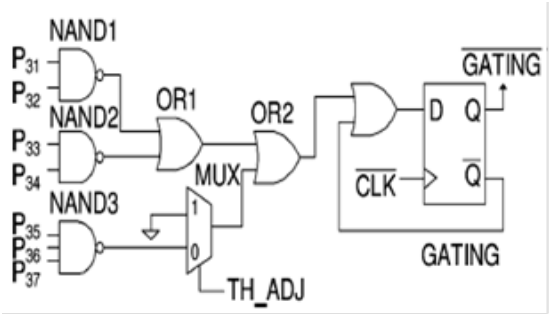

Fig.2. CLDC Design for VL-CSA

In our 64-bit VL-CSA design, the input bits of are used to detect the long-latency operations. The detection logic can be expressed as follows:

$$LONG\_OP = (A31 \oplus A31)(A32 \oplus A32)\ldots(A37 \oplus A37)$$

Due to the NBTI effect, the circuit delay continuously increases with the degradation of PMOS threshold voltage [5]. VL-adder in which the detection threshold of long/short-latency operations can be adaptively adjusted to account for NBTI-degraded delay: operations with an NBTI-degraded delay that is longer than one clock cycle are automatically categorized as long-latency operations and executed within two clock cycles.When the circuit performance is degraded by NBTI effect, a guard band violation may occur as an output switch within the guard band.When delay will be increased at that time input of the data is captured one clock or more clock period during matching the input and output.

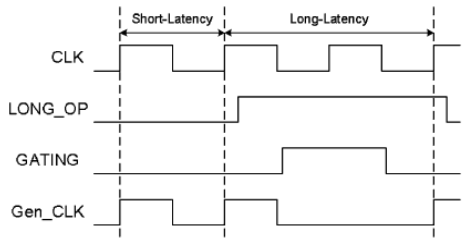

Fig.3. Timing diagram of VL-adder operation

III.IMPLEMENTATION OF DECIMATION FILTER

Implementation of decimation filter building block as shown in fig.4

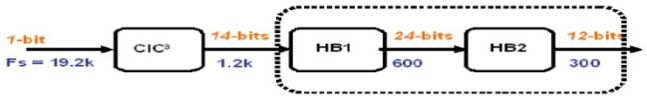

Fig.4 Building blocks of a decimator filter

In this design, a F_s = 19.2 kHz input sampling frequency is first reduce to 1.2 kHz (F_s/16) with a third orderCIC filter, followed by further reduction to 300 Hz using two HB filters. This decimation filter is designed for sigma-delta ADC in ECG (electrocardiograph) application, which has a signal band from 0.05 to 150 Hz.The CIC filter supporting theory and detail digital circuit and results are summarized in Section IV. The HB supporting theory and detail digital circuit and results are summarized in Section V. Conclusion is drawn in Section VI.

A. CIC FILTER

A 3rd orderCIC(Cascade Integrator Comb) filter is selected for a better attenuation. The CIC filter will reduce the sampling frequency by a factor of 16 and differential delay used is 1. The frequency of the input signal is 19.2 kHz and the frequency of the output signal is 1.2 kHz. Two CIC filter design approaches were implemented to estimate their area and power performances.

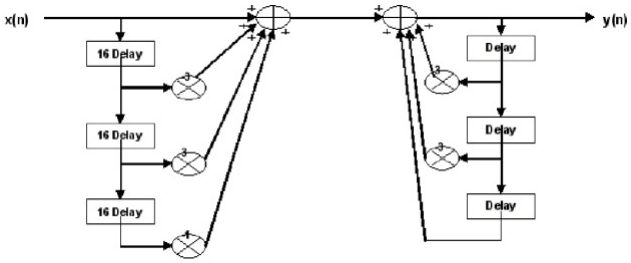

Fig. 5 Building blocks of a CIC filter

Fig. 5 shows the block diagram of the polynomial CIC filter. The output for each time sample is determined by the current input, previous input, and previous output. The structures presented here are cascades of CIC decimation and simple polynomial-based filter finite-impulse response FIR)filter[12].The CIC filter is used as an anti-aliasing filter when the data rate is high since the operation in the CIC filter only consists of addition operation. The transfer function of the CIC filter can be written in equation is.

$$H(z) = \left(\frac{1-z^{-R}}{1-z^{-1}}\right)^{N}$$

where, R and N are the decimation rate and order of the IC filter CIC decimation filter make the circuit to work at low frequencies as well as low power dissipationOne benefit of running the compensation filter at the low rate is to achieve a more efficient hardware solution, that is, more time sharing in the compensation FIR filter

In CIC filters, the comb section can precede, or follow, the integrator section. It'ssensible, however, to put the comb section on the side of the filter operating at the lower sample rate to reduce the storage requirements in the delay [9].Swapping the comb filters with the rate-change operations results in the most commonimplementation of CIC filters. Notice the

decimation filter's comb section now has a delay length (differential delay) of N = D/R. That's because an Nsample delay after decimation by R is equivalent to a Dsample delay before decimation by R. Likewise for the interpolation filter; an N-sample delay before interpolation by R is equivalent to a D-sample delay after interpolation by R which yields two major benefits: first, the comb section's new differential delay is decreased to N = D/Rreducing data storage requirements; second, the combeffects reduce hardware power consumption[10]section now operates at a reduced clock rate.

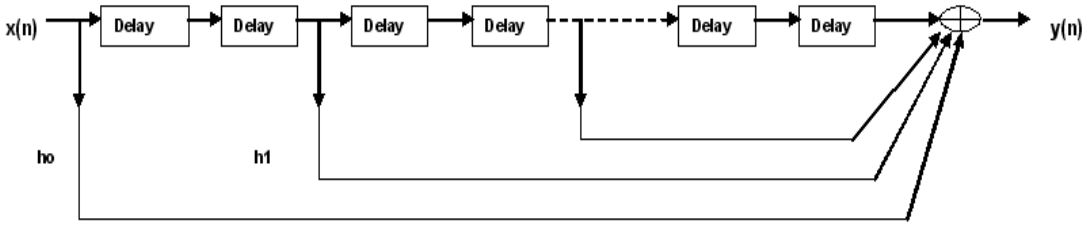

Fig. 6 Building blocks of a Half band filter

The second HB filter is a higher order filter to improve the attenuation. In this design, the second HB filter is a 45 tapfilter with 23 non-zero coefficients and it reduces the sampling frequency from 600 Hz to 300 Hz.
FIR filters offer control over filter shaping and linear phase performance. Due to its linear phase response, they are used in audio application, but at the cost of the high filter order.[2] A linear phase FIR filter requires large number of coefficients, we have implemented half-band FIR filter to reduce the number of coefficients.[4] In half-band filters, the number of taps is reduced considerably since the odd coefficients are zeros, which reduces the hardware and also power consumption.

IV.RESULTS AND ANALYSIS

The presented method has been validated by designing the Decimation filter stage using VHDL. The filter has been synthesized in a 0.18 micro secondCMOS technology.Both behavioural and timing simulations conformedthat the circuit is functional and meets specification. This chapter contains performance analysis of implement conventional Adder and VL-Adder in the decimation filter. The input to a comb filter is 19.2kHz which is the output of oversampling converter. In this filter decimation factor 16 is used, there output of comb filter is 1.2KHz..This is the input frequency of 2-stage half band filters in which each half band filter is decimates individually by a factor of 2.All results are obtaining using mentor graphics tools also verified the same for low power and compactness in are using synthesis tool in Xilinx. Also functionality is verified modelsim through observing the down sampling rate.

A.SIMULATION RESULT

The Fig.7 shows the simulation results of implement the conventional adder in the decimation filter.

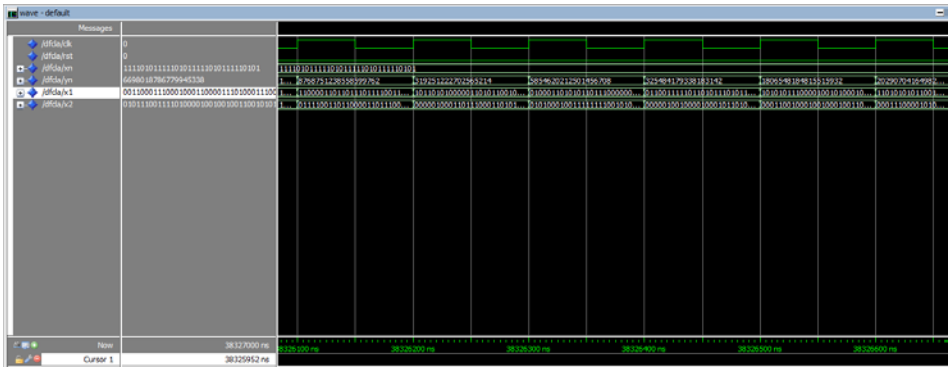

Fig.7 simulation results for decimation filter using conventional adder

The simulation results of decimation filter using conventional adder is obtained using mentor graphics tool shown in Fig 7 and the figure has input and clk, The clk is used to represent the clk signals and the input signal is the givien to filter and output taken after sometimes because due to operation delay.

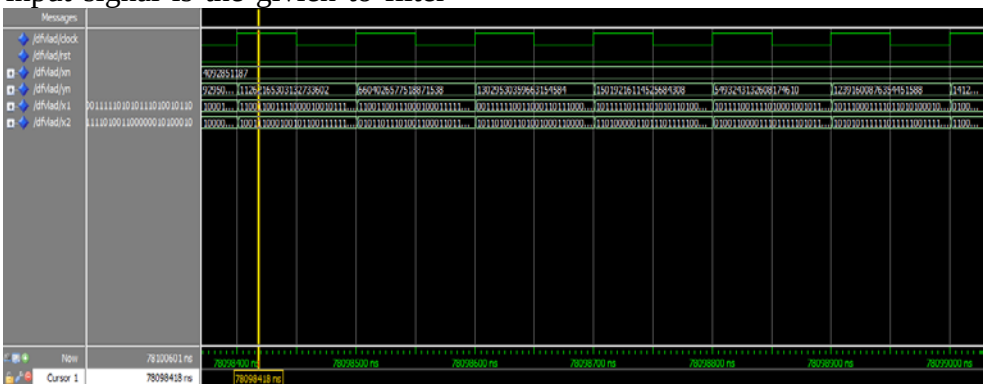

Fig.8 simulation results for decimation filter using VL-adder

The Fig.8 shows the simulation results of implement the VL- adder in the decimation filter.The simulation results of decimation filter using VL- adder is obtained using mentor graphics tool shown in Fig.8 and the figure has input and clk, The clk is used to represent the clk signals and the input signal is the givien to filter and output taken after sometimes because due to operation delay.

B.SYNTHESIS ANALYSIS

Decimation filter is implemented to details such as the type of filter used, the decimationfactors, and the number of filter coefficients for eachstage of two standards.The performance can be inferred from the obtained synthesized reports that by using conventional and VL-Adder, since number of non-zero bits gets reduced to half there by amount of hardware(adders) required gets reduced, which results in reduction power dissipation but at the cost of area.From the table 1, we can realize the decimation filter output that using VL-CSA and CONV.CSA. The significant amount of power,delay and area is reduced VL-CSA implement of decimation filter using mentor graphics tool.

Filter	ADDER	DELAY (ns)	AREA (gate count)	POWER (mw)
Decimation Filter	Conventional CSA	10.447	66339	1957
	VL-CSA	6.728	62535	1127

Table.1 Comparison of Decimation Filter using CONV.CSA and VL- CSA

V. CONCLUSION

In conclusion, different design approaches were implemented to realize a low power decimator filter. The performances in term of power consumption, delay and gate count were also compared with using VL-CSA and conventional CSA. In order to achieve low power consumption,

the operating Sample rate frequency and hardware reduction concept were implemented using mentor graphics tool.In audio applications, need for efficient digital filter has been increasing at high rate because of high speed and low power requirements. In this paper, we discussed design of a decimation filter used for high performance audio applications.This decimation filter is designed for sigma-delta ADC in ECG (electrocardiograph) application, which has a signal band from 0.05 to 150 Hz.

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REFERENCES

[1] J. Pouwelse, K. Langendoen, and H. Sips, "Dynamic voltage scaling on a low-power microprocessor," in *Proc. 7th Int. Conf. Mobile Comput.Netw.*, Jul. 2001, pp. 251–259.

[2] H. Suzuki, W. Jeong, and K. Roy, "Low power adder with adaptive supply voltage," in *Proc. 21st Int. Conf. Comput. Des.*, Oct. 2003, pp. 103–106.

[3] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective*. Englewood Cliffs, NJ: Prentice-Hall, 1996.

[4] T.-Y. Chang and M.-J. Hsiao, "Carry-select adder using single ripple-carry adder," *Inst. Electr. Eng. Electron. Lett.*, vol. 34–22, pp. 2101–2103, Oct. 1998.

[5] N. Kimizuka, T. Yamamoto, T. Mogami, K. Yamaguchi, K. Imai, and T. Horiuchi, "The impact of bias temperature instability for direct-tunneling ultra-thin gate oxide on MOSFET scaling," in *Proc. Very LargeScale Integr. Symp. Techol.*, 1999, pp. 73–74.

[6] M. Agarwal, B. C. Paul, M. Zhang, and S. Mitra, "Circuit failure prediction and its application to transistor aging," in *Proc. 25th IEEE VeryLarge Scale Integr. Test Symp. (VTS)*, May 2007, pp. 277–286.

[6] S. R. Norsworthy, R. Schreier, and G. C. Themes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, 1997.

[7] E. B. Hogenauer, "An economical class of digital filters for decimation and interpoloaton," *IEEE Transactions on Acoustics, Speech and SignalProcessing*, vol. ASSP-29, no. 2, pp. 155-162, 1981.

[8] Y. C. Lim, and B. R. Parker, "FIR filter design over a discrete powersof-two coefficients space," *IEEE Transaction on Acoustics, Speech andSignal Processing*, vol. ASSP-31 pp. 583-591, 1983 ,World Academy of Science, Engineering and Technology 42 2008523

[9]. Crochiere RE and Rabiner LR (1983) Multirate digital signal processing. Englewood Cliffs, NJ: Prentice`-Hall.

[10].Vesma J and Doctoral Thesis "Optimization and applications of polynomial based interpolation filters"., Tampere University of Technology,1999, Publ. pp: 254.

[11].Richa R. K. Singh"Polynomial based Design of CIC Compensation Filter used in Software Defined Radio for Multirate Signal Processing"Deptt. of Electronics and Communication Deptt. of Electrical EngineeringUIET CSJM University Kanpur MNNIT Allahabad.

[12] K.Shunhagavalli andDr.P.Vanaiaranian, "An area optimization of decimation filter using csd representation for hearing aid application"Irish signals and systems conference,2006,IET publication 2006,page:303-307.

[13].] Guo-Ming Sung and Hsiang-Yuan Hsieh "An ASIC design for decimation filter with canonic signed–digit representation"Intelligent signal processing and communication systems, 2008. ISPACS 2008.page:1-4

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