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High Gain and Reduced Switch Stress DC-DC Converter Topology for PV System

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Abstract:
This paper presents a new high step-up isolated DC-DC converter topology for photovoltaic system. The suggested configuration provides a converter with high voltage gain and reduced switch stress by using three coupled inductor with two hybrid voltage multiplier cell. The operation of the proposed converter is based on a charging capacitor with a single switch in its structure. A passive clamp circuit composed of capacitors and diodes is employed in the converter structure for lowering the voltage stress on the power switch as well as increasing the voltage gain of the converter. Since the voltage stress is low in the provided topology, a switch with a small ON-state resistance can be used. As a result, the losses are decreased and the efficiency is increased. The design of DC-DC boost converter is also discussed in detail. Simulation of DC-DC converter is performed in MATLAB/Simulink and the result are verified.

Keywords: IBC-Interleaved Boost Converter, CI-Coupled Inductor, VMC-Voltage Multiplier Cell SC-Switched Capacitor

1. Introduction

The renewable energy technology has undergone a substantial development in the last three decades. Photovoltaic (PV) system is promising and one of the fastest growing renewable energy sources. The proposal uses a voltage boosting cell associated with a coupled-inductor in order to achieve the high step-up voltage gain [1]. Differently from the high gain converters frequently proposed in the literature, this one presents inherent characteristic of current source at the output. The values suggested could be used to modify the function parameters for the scenarios considered, and DC converter is used between the PV module and inverter to minimize size of the transformer connected at the AC grid side [2]. The overall performance of such a system depends mainly on the efficiency of power conversion stages. Hence, selecting an appropriate high gain DC-DC converter is critical

In conventional boost DC-DC converter, diode reverse recovery problem and switch stress at extreme duty ratios restrict the practical voltage gain. Though a cascaded boost converter offers higher conversion ratio, presence of more components limits its operating efficiency [3]. The Magnetically coupled converters like fly back, push pull and full bridge converter can provide the required voltage gain by properly choosing turns ratio of transformer. Unfortunately, the leakage inductance of the magnetic element causes additional voltage stress and incremental losses on the switch. Without using a transformer, several methods to enhance the voltage gain include using voltage multiplier cell (VMC), coupled inductor (CI) and switched capacitor (SC) networks [4].

The step up converters provide the required voltage gain but their power handling capability is limited by their component count. Three phase interleaved boost converter (IBC) based on coupled inductors and VMC is proposed. The three switches present in the operated with a uniform phase shift between them. This helps to reduce the input current ripple [5]. Two simple inductors are replaced by coupled inductors to increase the voltage gain and handle higher power. The main features of this converter are high voltage gain, low voltage and current stress on the switches, low input current high power handling capability. Recently the use of step-

up DC-DC converters with high voltage ratio has been increased. That is due to the growing usage of this type of converters in a wide range of applications such as fuel cell stacks (FC), photovoltaic (PV) cells, uninterruptable power supplies (UPS), etc. In these sorts of applications high step-up converters are used to convert the low level varying primary voltage to the desired regulated high voltage output [6]-[8].

The conventional boost converter is not applicable in power sector for high voltage gain due to high switching losses. The duty cycle of an isolation transformer, which is connected in open-loop condition of the controlled isolated dc–dc converter, is fixed. In the resultant of soft switching of all the power semiconductor switches can be always achieved by utilizing the leakage inductance [9]-[11]. This paper proposed a dc-dc boost converter topology based on three winding coupled inductor and diode-capacitor technology for high step-up, high power density and high efficiency conversion, which adopts a single switch and two series hybrid voltage multiplier cells. Moreover, two identical passive regenerative snubbers are used for absorbing the energy of stray inductance, clamping the voltage spike of the main switch [12]-[14].
you submit your paper print it in two-column format, including figures and tables. In addition, designate one author as the "corresponding author". This is the author to whom proofs of the paper will be sent. Proofs are sent to the corresponding author only [15]-[17].

2. Operating Principle of the Proposed Converter

The equivalent circuit of the proposed converter topology is shown in Figure 1, in which a three winding coupled inductor (T) can be modeled by a magnetizing inductor Lm, a leakage inductance L_k, and an ideal transformer with primary winding N_1 and two secondary windings N_2 and N_3.

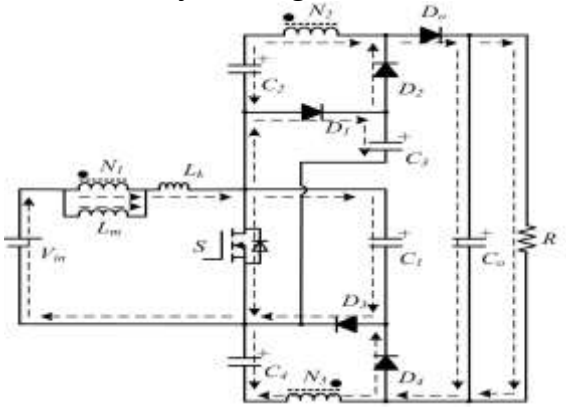

Figure 1: Circuit Diagram of the Proposed Converter

The two parallel passive regenerative snubbers are composed of the diode D_1 and capacitor C_3, the diode D_3 and capacitor C_1, through which the energy stored in the leakage inductor, can be recycled effectively. Also, the voltage across the main switch S is clamped to a lower level. Thus, the efficiency can be improved greatly. In addition, two hybrid voltage multiplier cells are respectively composed of secondary side windings N_2 and C_2, N_3 and C_4. When the main switch is on, the magnetizing inductor and two capacitors in voltage multiplier cells are charged, and the capacitor C_o provides energy to the load. When the main switch is off, the primary side and secondary sides of the coupled inductor, two capacitors C_2 and C_4, and input dc source are connected in series for transferring energy to the load. Therefore, the proposed converter can achieve high-voltage gain in appropriate duty cycles and low turns ratios.
The operating principles of the proposed converter for continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are presented as follows [18]-[20].

2.1. CCM Operation

This section presents the operation principle of CCM, and explains the power flow state of each mode. The operation process is divided into six modes during one switching period. The Figure 2 shows the waveforms of the proposed converter at CCM. To simplify the circuit analysis of the proposed converter, the following conditions are assumed [21]-[23]:

1. The capacitors C_1, C_2, C_3, C_4 and C_o are large enough to reasonably neglect the voltage ripples.
2. The power switch and diodes are ideal, except for D_o, D_2 and D_4. Because the reverse-recovery problems of diodes D_o, D_2 and D_4 will be discussed, and all forward voltage drops on them are ignored.
3. The coupling coefficient of the coupled inductor k is equal to $L_m/(L_m+L_k)$, and the turns ratio $n = N_2/N_1 = N_3/N_1$.

Mode I [t_0-t_1]: At $t=t_0$, the switch S is turned on nearly zero-current-switching (ZCS) due to the role of leakage inductance, which is helpful for alleviating the switching loss. During this short time interval, D_1, D_2, D_3, and D_4 are turned off, and D_o still remains on state. The current flow path is shown in Figure 3 (a). The magnetizing inductor L_m along with C_2 winding N_2 and N_3, the leakage inductance L_k is charged by and C_4 continues to release energy to the output through the source Vin. Therefore, magnetizing inductor current i_{Lm}, the secondary

winding currents i_{N2} and i_{N3} are decreased linearly, and the leakage inductance current i_{Lk} is increased linearly. The current ids through the main switch S is increased linearly [24]. This mode ends when the current flowing through winding N_2 and winding N_3 falls to zero at $t=t_1$.

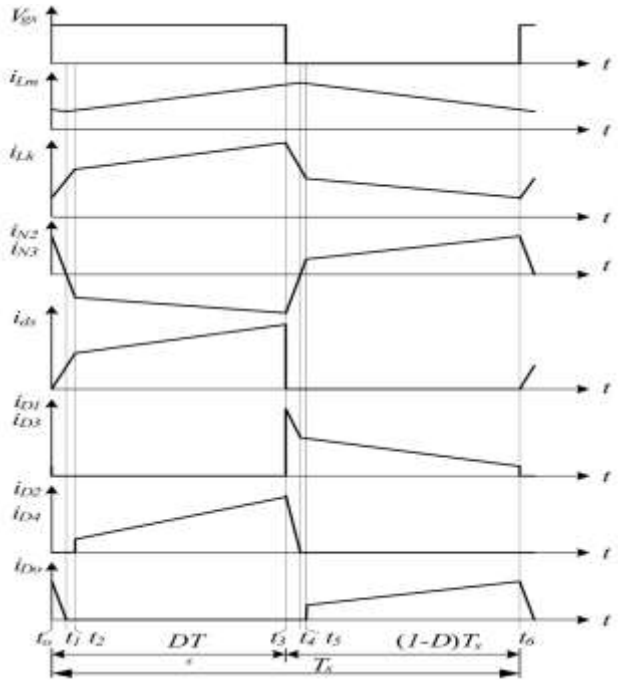

Figure 2: Waveforms of the Proposed Converter at CCM

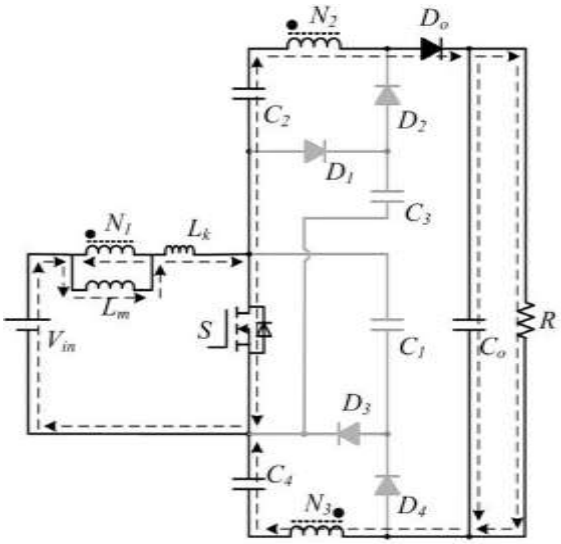

Figure 3 (a): CCM Mode I

Mode II $[t_1\text{-}t_2]$: From the time $t=t_1$, the equivalent junction capacitor C_o of the output diode D_o begins to release the stored charge to the leakage inductance of secondary winding and capacitors C_2 and C_4, and the reverse recovery energy of the output diode D_o is recycled [25]. The current flowing through winding N_2 and winding N_3 is increased inversely, and the current flow path is shown in Figure 3 (b). This time interval is extremely short, and the diodes D_2 and D_4 start to conduct at $t=t_2$.

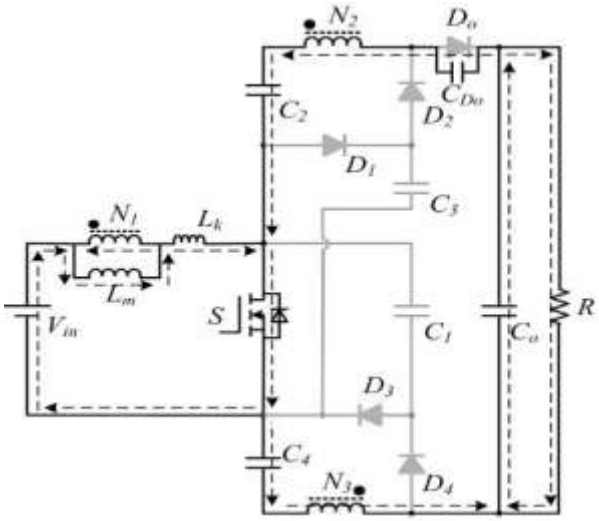

Figure 3 (b): CCM Mode II

Mode III $[t_2\text{-}t_3]$: During this interval, the secondary voltage VN_2 and the clamped capacitor voltage VC_3 are connected in series to charge the double-voltage capacitor C_2 through the switch and the rectifier diode D_2. Simultaneously, the secondary voltage VN_3 and the clamped capacitor voltage VC_1 are connected in series to charge the double-voltage capacitor C_4 through the switch and the rectifier diode D_4. The magnetizing inductor L_m and leakage inductor L_k are charged by the source V_{in}. Therefore, the current i_{Lm} and the leakage inductance current i_{Lk} are increased linearly. Meanwhile, the output capacitor C_o provides its energy to the load [26]. The current flow path is shown in Figure 3(c).

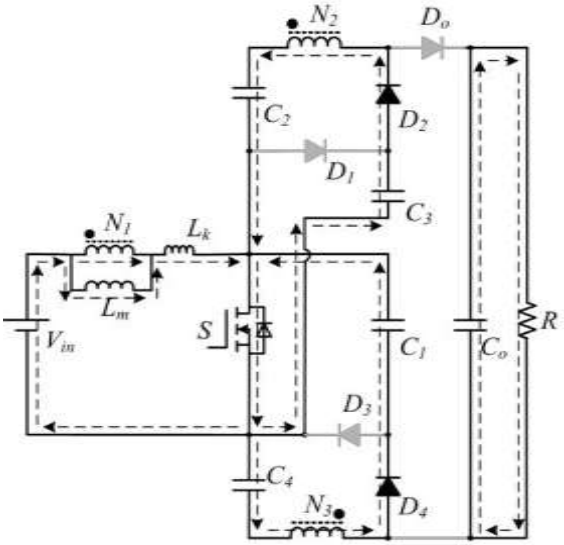

Figure 3 (c): CCM Mode III

Mode IV $[t_3\text{-}t_4]$: At the time $t=t_3$, the switch S is turned off. On the one hand, the input source V_{in} is series connected with N_1 and L_K to charge clamped capacitors C_1 and C_3 through diodes D_1 and D_3. The energy of leakage inductance is recycled and the current i_{Lk} is decreased linearly [27]. On the other hand, the secondary winding current i_{N2} (i_{N3}) are decreased rapidly since the opposite direction of the voltage of the winding N_2 and N_3. At the time $t=t_4$,

the winding current i_{N2} (i_{N3}) decays to zero. The current flow path is shown in Figure 3(d).

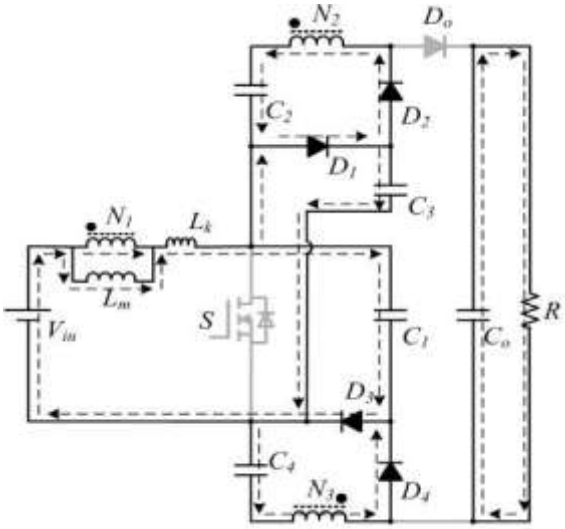

Figure 3 (d): CCM Mode IV

Mode V [t_4-t_5]: During this extremely short period, the equivalent junction capacitor CD_2 of the output diode D_2 and the equivalent junction capacitor CD_4 of the output diode D4 release energy, this is recycled [28]. The magnetizing inductor Lm begins to be discharged to capacitors C_1 and C_3, and the current flow path is shown in Figure 3 (e). Meanwhile, the output capacitor Co provides its energy to load R.

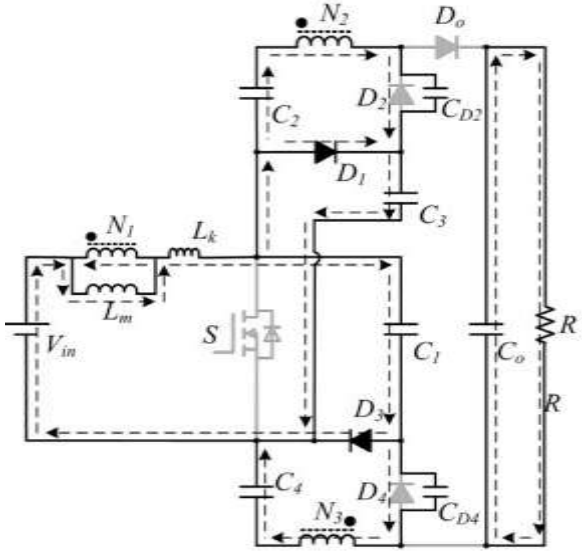

Figure 3 (e): CCM Mode V

Mode VI [t_5-t_6]: At t=t_5, the diode D_o is conducted. The current flow path is shown in Figure 3 (f). The leakage inductor, two capacitors C_2 and C_4, the magnetizing inductor and input source V_{in} are series discharged to the output. The clamped capacitors C_1 and C_3 are parallel charged by leakage inductance L_k and the DC source V_{in}. The voltage stress across the switch S is clamped to low voltage level. The magnetizing inductor current i_{Lm}, leakage inductance current i_{Lk}, diodes current i_{D1} and i_{D3} are decreased linearly [29]. Since the leakage inductance is smaller and the i_{Lk} current decreases faster than that of the magnetizing inductor current i_{Lm}, the secondary winding currents i_{N2} and i_{N3} are increase linearly according to the principle of idea transformer. When the switch S is turned on again, this mode is ended.

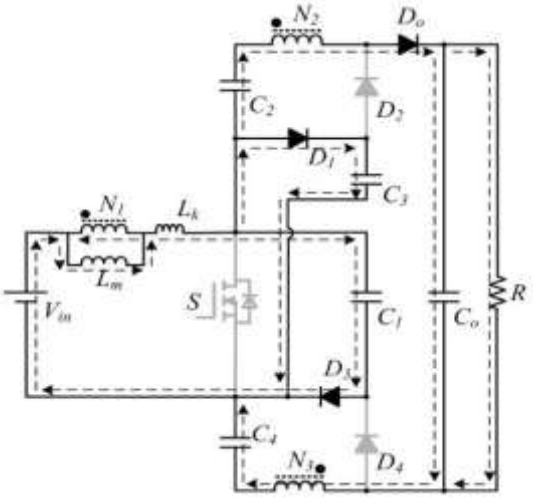

Figure 3 (f): CCM Mode VI

3. Performance Analysis

3.1 Voltage Gain

To simplify the steady-state analysis, only mode-III and mode-IV are taken into account, and other modes occupying extremely short time are ignored. When the switch *S* is turned on, the following equations can be obtained from Fig.3(c).

$$v_{N1}^{III} = \frac{L_m}{L_m + L_k} = kV_{in} \quad (1)$$

$$v_{Lk}^{III} = \frac{L_k}{L_m + L_k} V_{in} = (1-k)V_{in} \quad (2)$$

$$v_{N2}^{III} = v_{N3}^{III} = nv_{N1}^{III} = nkV_{in} \quad (3)$$

Where *k* is the coupling coefficient of the coupled inductor, and *n* is the turn's ratio of the coupled inductor. When the switch *S* is turned off, the coupled inductor and the DC source V_{in} are in series connected to discharged the outlet side as shown in Fig.3 (f). By applying voltage-second balance principle on N_1, N_2, N_3 and L_k, the voltage V_{N1}, V_{N2}, V_{N3}, and V_{Lk} are found as follows [30]:

$$v_{N1}^{VI} = \frac{Dk}{1-D} V_{in} \quad (4)$$

$$v_{N2}^{VI} = v_{N3}^{VI} = \frac{nDk}{1-D} V_{in} \quad (5)$$

$$v_{Lk}^{VI} = \frac{D(1-k)}{1-D} V_{in} \quad (6)$$

The voltage of capacitors C_1, C_2, C_3 and C_4 can be written as:

$$V_{C1} = V_{C3} = V_{in} + v_{N1}^{VI} + v_{Lk}^{VI} = \frac{1}{1-D} V_{in} \quad (7)$$

$$V_{C2} = V_{C4} = V_{C1} + v_{N3}^{III} = (nk + \frac{1}{1-D}) V_{in} \quad (8)$$

3.2 Voltage Stresses on Components

The voltage stress of the main switch S and D_1, D_3 are represented as

$$V_{ds} = V_{C1} = V_{C3} = V_{D2} = V_{D3} = \frac{1}{1-D} V_{in} = \frac{1}{2n+3} V_o \quad (9)$$

According to the aforementioned description of CCM modes, the voltage stress of diodes *D*2, *D*4, and *D*o are given as

$$V_{D2} = V_{D4} = \frac{1+n}{1-D} V_{in} = \frac{n+1}{2n+3} V_o \quad (10)$$

$$V_{Do} = \frac{2n+1}{1-D} V_{in} = \frac{2n+1}{2n+3} V_o \quad (11)$$

For demonstrating the performance of the proposed converter, the proposed converter is compared with other three winding coupled inductor converters in [25] and [30] as shown table 1. It can be found that the voltage of the proposed converter is highest and the voltage stress on switch is lowest under the same duty cycle D and the same turns ratio n designed as less than 2. Besides, the quantities of diodes and capacitors are the least as converter introduced in [25], which is conducive to reducing the cost.

Table 1 Performance Comparison of Similar Converters

High step-up converter	Converter in [25]	Converter in [30]	Proposed converter
Voltage gain	$\frac{2n+2-nD}{1-D}$	$\frac{3n+2-nD}{1-D}$	$\frac{2n+3}{1-D}$
Voltage stress on switch	$\frac{V_o}{2n+2-nD}$	$\frac{V_o}{3n+2-nD}$	$\frac{V_o}{2n+3}$
Quantities of diodes	5	6	5
Quantities of capacitors	5	6	5
Quantities of windings	3	3	3

3.3 Turns Ratio of Coupled Induction Selection

In the proposed converter, the coupled inductor is operated as both flyback and forward converters; therefore, the coupled inductor should be designed as a flyback transformer. The turn's ratio of the coupled inductor has an influence on the switch duty cycle [31]-[33], the voltage gain, and the voltage stress of power devices. The turn's ratio can be depicted by

$$n = \frac{V_o}{2V_{in}}(1-D) - \frac{3}{2} \quad (12)$$

The input voltage and the output voltage are determined by the specific application. Hence, if the duty cycle is chosen, the turn's ratio of the coupled inductor can be carried out easily, and then the voltage stress of power devices can be calculated. Generally, the duty cycle is less than 0.7 in order to decrease conduction loss. On the contrary, if the duty cycle is too small, the volume of the coupled inductor will be larger due to the bigger turn's ratio. As a result, a compromise should be made considering the duty cycle and the turns ratio under given voltage gain [34].

3.4. Coupled Inductor Design

In theory, the proposed converter will be operated in CCM (continuous conduction mode) if the *Lm* is higher than *LmB*, and it will be operated in DCM (discontinuous conduction mode) when the *Lm* is smaller than *LmB*.

$$L_{mB} = \frac{D(1-D)^2 R T_s}{2(2n+3)^2} \quad (13)$$

3.5. Main Switch and Diodes Selection

In practice, voltage spike will occur when the main switch is turned off owing to the leakage inductance of the coupled inductor and parasitic capacitor. In addition, the spike voltage also can be caused because of the stray inductance and capacitance existing in printed circuit board. Hence, considering above-mentioned factor, the voltage and current ratings of the chosen active devices are usually larger than150% of the calculated value [35].

3.6. Capacitor Selection

The voltage ripple of capacitors depends on the value of capacitors. In order to restrain the voltage ripple to an acceptable range, the minimum capacitance should be calculated. According to $\Delta Q = C\ VC = I\ C\ T$, (35) and (36) can be used to estimate the capacitance of capacitors, in which Vo is the output voltage, V_C and V_{Co} represent the maximum acceptable voltage ripple on capacitors C_1~C_4 and C_o, fs is the switching frequency, and R is the load.

$$C \geq \frac{V_o}{\Delta V_C R f_s} \quad (14)$$

$$C_o \geq \frac{D V_o}{\Delta V_{Co} R f_s} \quad (15)$$

Considering the equivalent series resistor (ESR), a fraction of power will be dissipated when the converter is in operation. The ESR of an aluminum electrolytic capacitor will be smaller as the capacitance increases. Therefore, the capacitance is usually selected to be much larger than the calculated value.

4. Result Analyzes

To reconfirm the viability and accurate performance of the proposed high step-up dc-dc converter, some simulation results through MATLAB/Simulink software and a built prototype in the laboratory to verify the performance of the proposed converter. In the MATLAB/Simulink platform, the voltage waveform for input and output of the proposed converter are shown. Figure 4 shows the simulation results of the proposed converter with an output voltage of 400V.

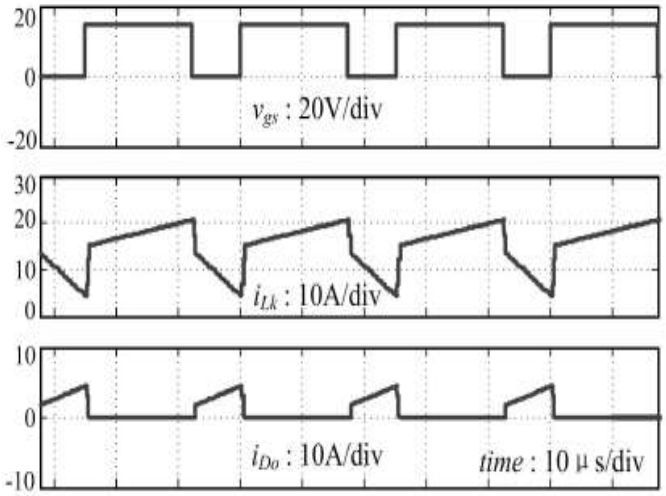

Figure 4 (a): Simulated Results of Vgs, i_{LK} and i_{Do}

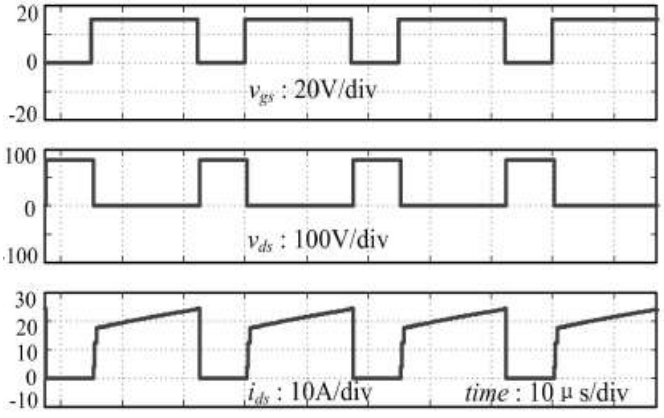

Figure 4 (b): Simulated Results of V_{gs}, V_{ds} and i_{ds}

The electric specifications and circuit components are selected as V_{in}=25V, V_O=400V, f_s=40KHz, N_1:N_2:N_3=1:1:1, C_1= C_3=100μF, C_2=C_4=220μF, Figure 4(a) gives the simulated results of driving signal of switch S and the input current $i_{Lk,}$ and the current i_{Do} through the diode D_O. It shows that the simulated results of voltage of the converter are operated in CCM and the reverse-recovery problem of output diode is alleviated. Figure 4(b) illustrates the simulated results of the voltage and current stress across switch S. One can see that the voltage stress is far lower than output voltage, and the switch S is turned on with zero current nearly due to the leakage inductor of coupled inductor. Figure 5 shows the PWM generator signal for various duty cycles.

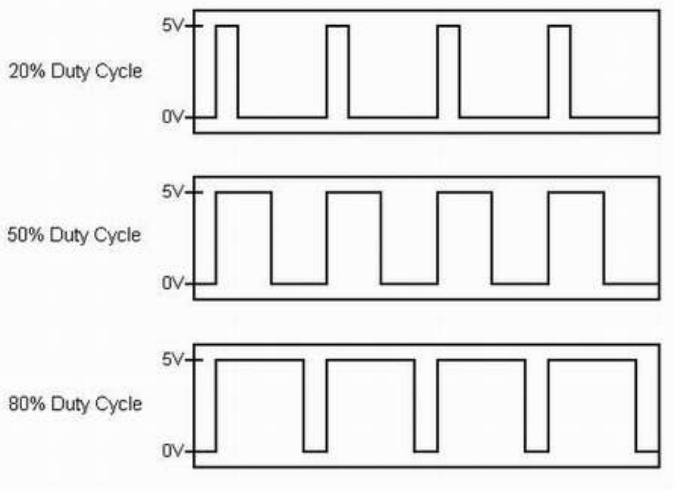

Figure 5: PWM Generator Signal for Various Duty Cycles

5. Conclusion

This paper proposes a novel DC-DC boost converter structure by using a single switch, a three- winding coupled inductor and two hybrid multiple voltage cells. The two multiple voltage cells are parallel charged and discharged series. Thus, the presented topology can provide very high voltage gain under appropriate duty cycle and turns ratio. Meantime, the operation analysis and design for the converter becomes quite simple since the two multiple voltage units are identical. Moreover, the voltage stress of the main switch *S* is clamped at a level far less than output voltage, so the power switch *S* with low *Rds*(*on*) can be selected to improve the efficiency. The steady- state analysis of the converter is discussed in detail. The simulated results verify the good performance of proposed converter.

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