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Design and Performance Analysis of LC Oscillator and VCO for ISM and WI-FI Band Applications

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Abstract:
Wireless device portability and power efficiency are the two major challenges in modern device modelling. Voltage Controlled Oscillator (VCO) is one the most essential circuit used in wireless systems. From last decade, people want to be connected all the time using wireless communication devices. In addition, the demand for high bandwidth communication channels has exploded with the advent of the internet.
Thanks to the high density available on integrated circuits, sophisticated digital modulation schemes can be employed to maximize the capacity of these channels. This has changed the design of wireless and wire line transceivers. We focus on the design of a critical sub-block: the voltage controlled oscillator (LC oscillator, VCO). We review the requirements for VCOs and evaluate the advantages and disadvantages of VCO.
A new approach is proposed work is aimed to achieve the desired operating frequency, high stability. Power has become one of the most important paradigms for microprocessor & ASIC/SOC designs. Hence to have very low power consumption, this paper work is decided to implement using VLSI technology.

Keywords
CMOS, LC oscillator,VCO ,ISM, WI-FI Band.

I. INTRODUCTION

With the growth of wireless communication for personal purposes, the demand for low-cost, low-power and minimum area, wireless systems has increased rapidly. Device portability and power consumption are the two crucial parameters for high performance wireless devices such as GSM, WLAN [1] Bluetooth and Pico-Radios Wireless Sensor Network [2]. Voltage Controlled Oscillator (VCO) is the most basic circuit required for all wireless systems. VCO is a high frequency circuit and the power consumption of the wireless communication system depends heavily on it [3].
LC oscillators are commonly used in CMOS radio-frequency integrated circuits (RF-ICs) because of their good phase noise characteristics and their ease of implementation [4, 5, 6, 7, 8]. In modern wireless communication systems, channels are placed very closely for the efficient use of the frequency spectrum[9].
We have decided to study oscillators, because we were interested in this type of Structure as it is useful in many different types of electronic equipment. Their role is to create a periodic logic or analog signal (sinusoidal or not) with a stable and predictable frequency. They are used in different fields and especially in radio-frequency transmission in order to generate the carrying signals. We also need this structure to generate the main clock of processors. Moreover, there are many different types of oscillators. We chose to study LC oscillator and Voltage controlled oscillators. Here our study particularly focuses on the frequency parameter.
The VCO core is based on an inverter-type ring oscillator supplied by a current coming from the voltage-to-current converter [10]. The VCO consists of four-stage fully differential delay cells performing full switching. Phase noise [11], tuning range, power consumption and device size are the main areas to be considered while designing any VCO circuit. Nowadays, the VCO designs are made in such a way that greater emphasis is on reducing power consumption, so it is difficult to achieve low phase noise and wide tuning range because of more emphasis on the low-power VCO designs [12].

II. DIFFERENTIAL LC OSCILLATOR:

Differential LC oscillator the operating frequency is decided by the capacitor and inductor value.
The operating frequency is given by:

$$fo = \frac{\omega 0}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$$

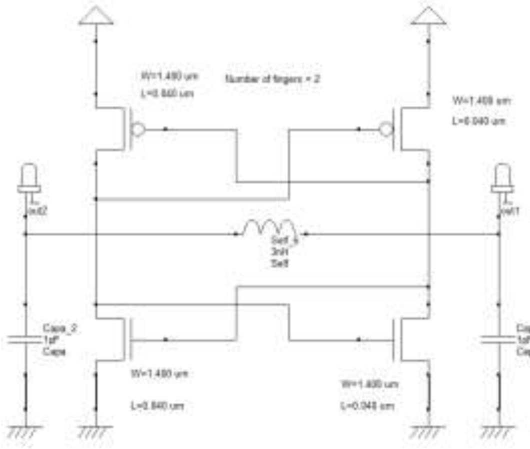

Fig I: LC Oscillator Model

Here, in our implementation layout as shown in fig. II (a), we added some virtual capacities and inductor because their values are easy to change during the simulation. Once the good values of the capacities and inductor were known, we could implement these components.

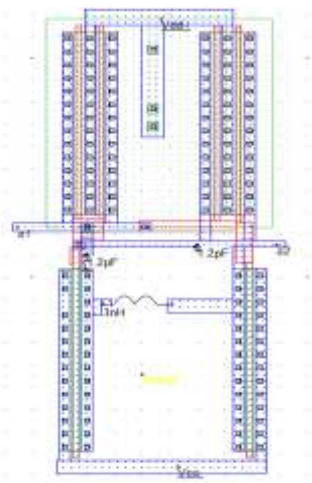

Fig.II (a): Implementation of LC Oscillator–Virtual LC

Table 1. Width and Length for PMOS & NMOS

	Width(µm)	Length(µm)	No. of Fingers.	Current (I max)
Pmos 1	1.660	0.040	2	1.746mA
Pmos 2	1.660	0.040	2	1.746mA
Nmos1	1.660	0.040	1	1.484mA
Nmos2	1.660	0.040	1	1.484 mA

In VLSI design, the actual active components are used in terms of the material layer properties and the behaviour. Fig. II (b), here we added actual designed capacitor and Inductor. The effect of the actual component is as same as the virtual components.

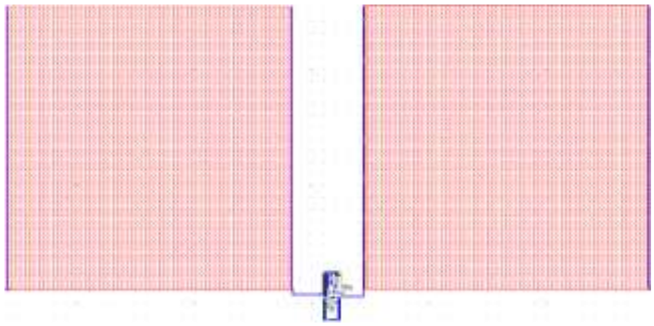

Fig. II (b): Implementation of LC Oscillator –Actual LC

The fig. III(a) shows the simulation result of LC oscillator with its voltage Variation. Here we are placing the capacitor with 1.2 pF each and inductance with 3nH. Both the outputs oscillate and a permanent regime is reached after some eight nanoseconds (8 ns). A simulation model displays as in fig. 3 (b) shows the frequency variations versus time together with the voltage variations. We can notice on Fig. 3(b) that the frequency is stable around 3.74 GHz. This is an ISM band frequency that we can use for the further application.

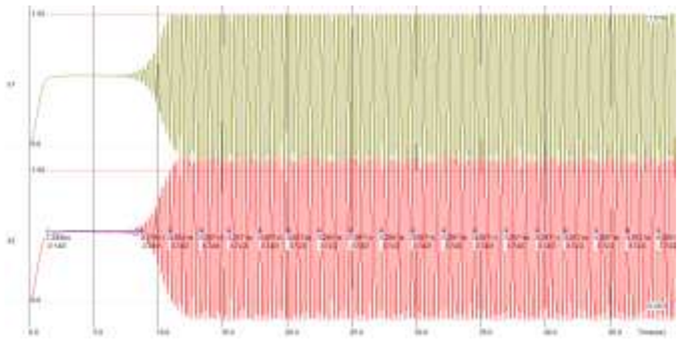

Fig.III (a): LC Oscillator Frequency and Voltage Variation

Implementation of LC Oscillator- Actual Component

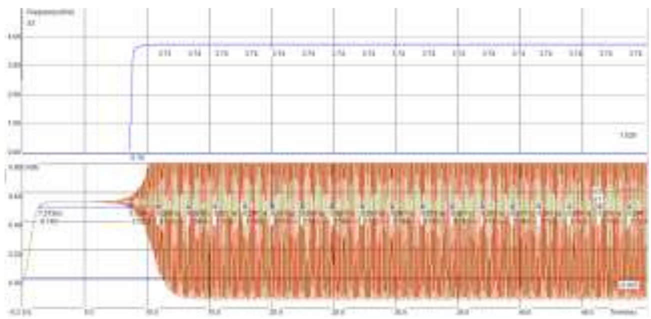

Fig.III (b): LC Oscillator operating Frequency

Fig: III (c) represents a Monte Carlo Simulation, which consists in studying frequency variation when Vdd is varying in a random way. We can easily conclude that any supply fluctuation has a significant impact on the oscillator frequency. [17][18]

In parametric analysis, we study the power dissipation on the particular node, paretic capacitance of the node. Montecarlo analysis pro window and observing variations on the frequency by changing the samples values to 20.

Montecarlo analysis is computational algorithms that rely on repeated random sampling to obtain numerical results. They are often used in physical and mathematical problems and also simulations of the effect of component variations on performance.

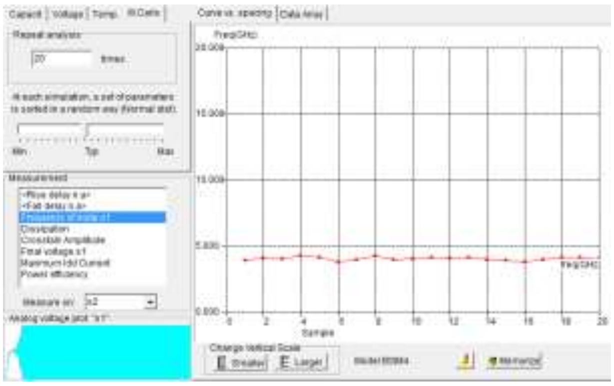

Fig. III (c): Monte Carlo analysis (effect on frequency)

Simulating the extracted SPICE net list with the help of third party simulator. Re-simulate the inverter for (W/L)n of 4λ/2λ and (W/L)p of 8λ/2λ using a capacitive load of 1pF. Measure the rise time and fall time. Estimate the value of Rp and Rn.

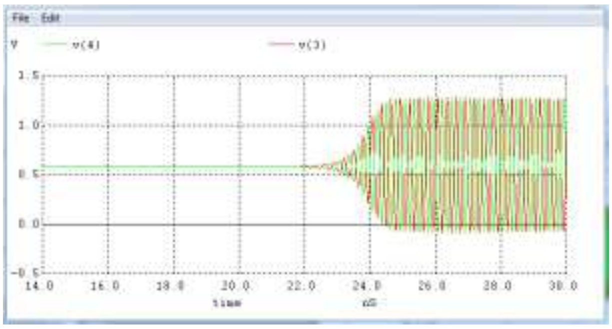

Fig. III (d) Transient Analysis-SPICE netlist

IV. VOLTAGE CONTROLLED OSCILLATOR

A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. It generates a clock with a controllable frequency from -50% to +50% of its central value. Here in Fig. IV, we studied VCO. The frequency of oscillation is varied by the applied DC voltage 'V_control' which is used to fix the current in NMOS as N1, N2, N3, N4 and PMOS as P1, P2, P3, P4. A change on V_control will modify the currents in the inverters and act directly on the delay.

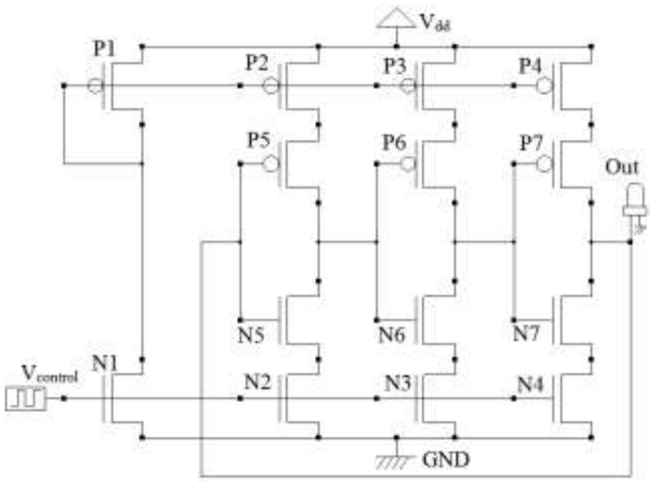

Fig IV: Voltage Controlled Oscillator Structure

Proposed VCO design shown in Fig. IV is three stage ring oscillator which is controlled by a current source. Main emphasis is laid over low power and low area consumption in proposed design.

Recently Wireless systems took over the whole communication system and portable devices are widely used.

For working on portable devices we must have low power dissipation and less area utilizing circuit.

In the proposed work, PMOSP5 and NMOS N5 forms an inverter, and similarly P6, P7, N6 and N7 construct inverter while upper PMOS P2 and lower NMOS N2 operate as current sources. The current sources (P2and N2) limit the current available to the inverter (P5-N5). The inverter chain uses a voltage control $V_{control}$ to modify the current that flows in the N1, P1 branch. The current through N1 is mirrored by N2, N3 and N4. The same current flows in P1. The current through P1 is mirrored by P2, P3 andP4. Consequently, the change in $V_{control}$ induces global change in the inverter currents, and acts directly on the delay. A higher number of stages are commonly implemented, depending on the target oscillating frequency and consumption constraints.

Here, we have three inverters in the loop but it is possible to put more, it depends on the oscillating frequency required. The voltage variations of input signal 'V_control' and output signal 'Voltage_ctr_osc' are given in Fig.6. We chose to modify V_control very slowly, in order to see the influence on the oscillations. We put Control higher than 0.5 V, because there are no any oscillations under that value.

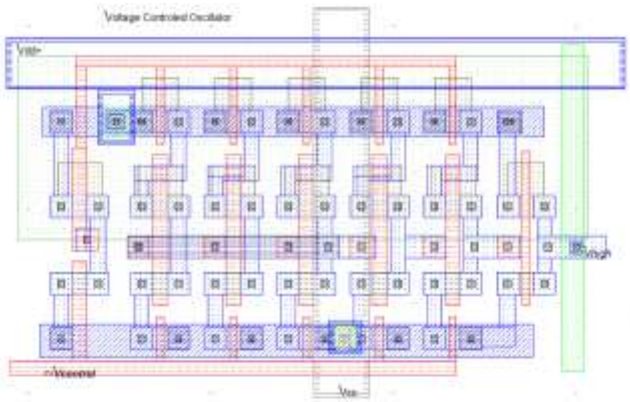

Fig V: Implementation of Voltage Controlled Oscillator–Layout

Properties for the .MSK file provided above
Width: 3.4µm (169 lambda)
Height: 2.1µm (106 lambda)
Surf: 7.2µm2 (0.0 mm2)

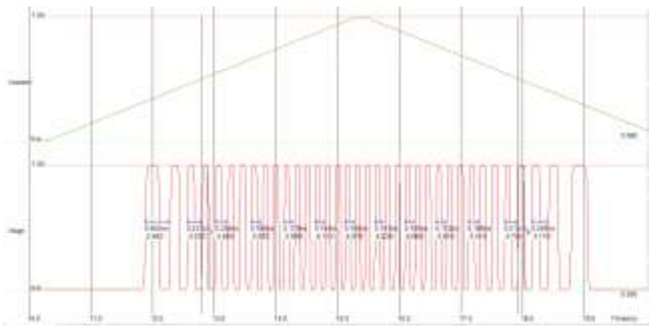

Fig.VI (a) : Voltage Variations of Input Signal 'V_control' andOutput signal 'Voltage_ctr_osc'

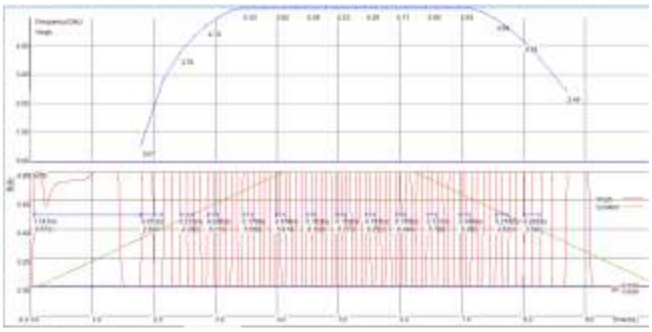

Fig.VI (b): Frequency and Voltage variation in VCO

Fig.VI (c): Frequency with constant V-Controll

Fig: VI (d) represents a Monte Carlo Simulation, which consists in studying frequency variation when Vdd is varying in a random way. We can easily conclude that any supply fluctuation has a significant impact on the oscillator frequency. [2][3]

In parametric analysis we study the power dissipation on the particular node, paretic capacitance of the node. Montecarlo analysis window and observing variations on the frequency by changing the samples values to 20.

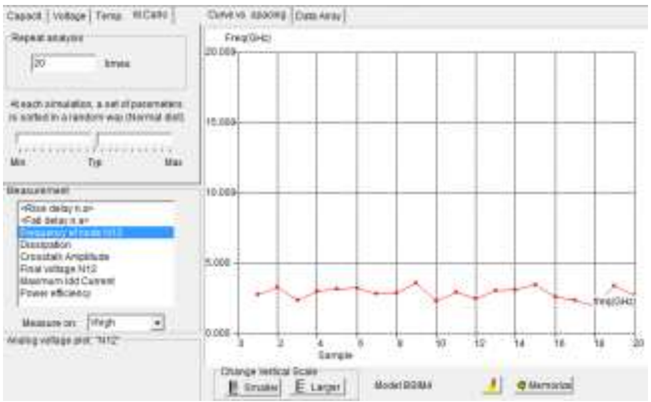

Fig.VI (d): Monte Carlo analysis (effect on frequency)

As we can notice on Fig. 8, the oscillation frequency's variation is not linear. The maximum frequency upto 6.12 GHz is obtained when V_control is maximal. It is possible to modify these values by implementing more inverters.

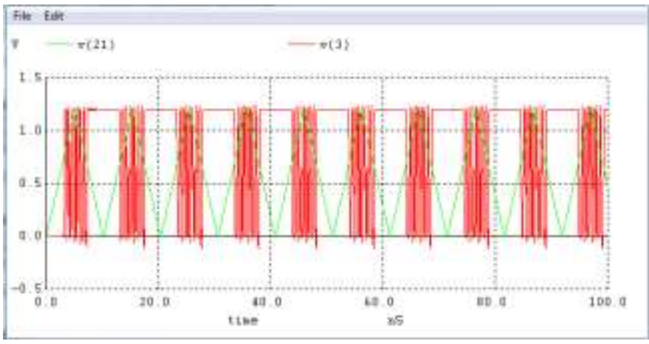

Fig. VI (e): Transient Analysis-SPICE netlist)

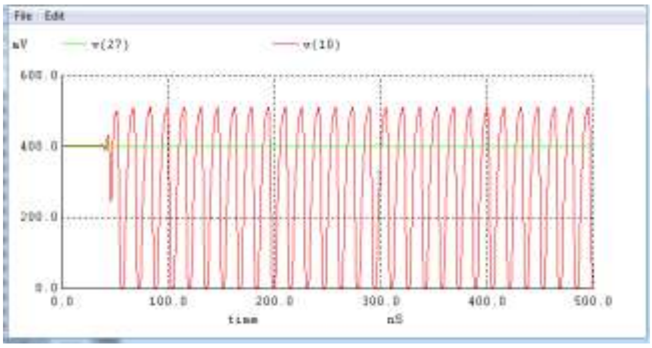

Fig. VI (f): Transient Analysis-SPICE netlist (Constant V-Controll)

Table: Parameter of MOS level implemented

Mos Level parametersTypical Value 45nm			
Parameter	**Definition**	**NMOS**	**PMOS**
VTO	Threshold Voltage	0.18V	-0.15 V
U0	Carrier Mobility	0.016 m2 /V-s	0.012 m2 /V-s
TOXE	gate oxide Thickness	3.5 nm	3.5 nm
PHI	Surface Potential	0.15 V	0.15 V
GAMMA	Bulk threshold Parameter	0.4 V^0.5	0.4 V^0.5
W	Channel Width	80 nm minimum	80 nm
L	Channel Length	40 nm minimum	40 nm

Table 2. Key Features of 45nm Technology

V. Analysis

Oscillators are the important part of many electronics designs. As in VLSI area and power plays a vital role**.** Table will extract the both values.

Table 2: Result Analysis

Parameters	**VCO**	**Differential LC**
Area	**7.2μm2**	**9.0μm2**
Power	**36.381μW**	**0.766 mW**
No. of Gates	**24**	**4**

VI. CONCLUSION

In this paper we simulated LC oscillator and voltage control oscillator using Microwind 3.5.

However, for our paper, we decided to use the ISM radio bands of frequency (Industrial, Scientific and Medical radio bands), which are not controlled by national regulations. Their use is free and we don't need any authorization for Industrial Scientific or Medical use. For example, we selected the 2.400 – 2.483 GHz band of frequency which is used by Bluetooth applications, and the 5.725 – 5.875 GHz band for WI-FI applications.

The simulation was performed using Win Spice Version 03.2006 and library model for 45 nm CMOS technology. According to the obtained simulation results we can conclude:

a)The measured tuning range of the proposed Differential LC design is 0.14 to 3.74 GHz.

b)The measured tuning range of the proposed VCO design is 0.60 to 6.12 GHz.

c)The measured tuning range of the proposed VCO design is 1.20 to 2.87 GHz for a constant V_Controll as 0.4 V.

d)Familiarizing comparison with a basic understanding of the most important types of circuit analysis available with SPICE simulators.

For digital and data applications fully integrated oscillators are being widely used. The use of fully integrated tuned oscillators is products. Performance concerns as well as large area still inhibit the widespread acceptance of integrated tuned oscillators.

With the advent of higher communication data rates and digital clock rates and the proliferation of wireless terminals the demand for integrated GHz oscillators is growing. The use of fully integrated tuned oscillators is only emerging in wireless products. Performance concerns as well as large area still inhibit the widespread acceptance of integrated tuned oscillators.

VLSI technology is the fastest growing field today. From the continuous survey it is observed that foundry of technology and supply voltage range is continuously decreases with the advancement of technology. By scaling down the technology, we can optimize the parameters like power consumption. The current technology up to 2008-2009 was 90 nm technology. Hence considering the advancement of future technology and the advantage of 45 nm technology over 65 and 90 nm technology, the selection of 45nm technology for the proposed project was the proper choice of technology.

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