

# **Ddr3 Based Lookup Circuit For High Performance Network Processing**

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## **ABSTRACT**

Double Data Rate (DDR) SDRAMs have been prevalent in the PC memory market in recent years and are widely used for networking systems. These memory devices are rapidly developing, with high density, high memory bandwidth and low device cost. However, because of the high-speed interface technology and complex instruction-based memory access control, a specific purpose memory controller is necessary for optimizing the memory access trade off. In this paper, a specific purpose DDR3 controller for high-performance table lookup is proposed and a corresponding lookup circuit based on the Hash-CAM approach is presented.

## **I. INTRODUCTION**

With the development of network systems, packet processing techniques are becoming more important to deal with the massive high-throughput packets of the internet. Accordingly, advances in memory architectures are required to meet the emerging bandwidth demands. Content Addressable Memory (CAM) based techniques are widely used in network equipment for fast table look up [1]. However, in comparison to Random Access Memory (RAM) technology, CAM technology is restricted in terms of memory density, hardware cost and power dissipation. Recently, a Hash-CAM circuit [2], which combines the merits of the hash algorithm and the CAM function, was proposed to replace pure CAM based lookup circuits with comparable performance, higher memory density and lower cost. Most importantly, off-chip high-density low-cost DDR memory technology has now become an attractive alternative for the proposed Hash-CAM based lookup circuit. However, DDR technology is optimised for burst access for cached processor platforms. As such, efficient DDR bandwidth utilization is a major challenge for lookup functions that exhibit short and random memory access patterns. The extreme low-cost and high memory density features of the DDR technology allow a trade-off between memory utilisation and memory-bandwidth utilisation by customising the memory access. This, however, requires a custom-purpose DDR memory controller that is optimised to achieve the best read efficiency and highest memory bandwidth [3]. The objective of this work was to investigate advanced DDR3 SDRAM controller architectures and derive a customised architecture for the abovementioned problem.

This paper proposes an advanced DDR3 memory controller architecture optimised for a DDR3 based high-performance table lookup circuit and presents its

implementation using Altera Stratix III FPGA technology.

## **II. RELATED WORK**

Owing to the multi-bank architecture and burst write/read mode, concurrent operations on different banks are allowed in the SDRAMs. High memory bandwidth can be achieved by scheduling the memory access to each bank. Based upon this idea, many SDRAM users focus on bank control and data access sequences to achieve a better system performance.

In the applications of multimedia processing systems, Kim [4] presented an address-translation technique, which increases the memory bandwidth by 50%; Jaspers [5] mapped video data units into the memory in accordance with the statistics of actual data access results and interleaved access to the memory banks; Zhang [6] and Zhu [7] provided memory management solutions for H.264 applications, which increases bus efficiency by approximately one third. For general-purpose DDR memory controller implementations on FPGAs, the Xilinx DDR3 controller [8] keeps four banks open at a time and the least recently used bank will be closed for access to the unopened bank.

All these efforts abovementioned are under the assumption that successive data access patterns are predictable and thus data could be stored and retrieved at the previously known address location of the memory. However, this method is not applicable to the random data access required in networking systems. By regrouping the addresses Mladenov [9] is able to avoid excessive switching between rows, thus increasing the memory efficiency for random access. However, this method is highly dependent on the access pattern and the performance improvement is not guaranteed.

The presented research targets the above shortcomings by exploring specific purpose memory

controller architectures that permit the efficient utilisation of the DDR3 memory bandwidth.

### III. DESIGN METHODOLOGY

DDR3 SDRAM is the 3<sup>rd</sup> generation of DDR memories, featuring higher performance and lower power consumption [10]. In comparison with earlier generations, DDR1/2 SDRAM, DDR3 SDRAM is a higher density device and achieves higher bandwidth due to the further increase of the clock rate and reduction in power consumption benefiting from 1.5V power supply at 90 nm fabrication technology. With 8 individual banks, DDR3 memory is more flexible to be accessed with fewer bank conflicts.

The proposed Hash-CAM based lookup circuit is shown in Figure 1.



Figure 1: Hash-CAM lookup circuit using DDR3 SDRAMs

The original data and reference address information are stored in the DDR3 SDRAM. A lookup request (data input) for a given content is pipelined and processed by the Hash-CAM circuit to generate an address. This address value is forwarded to DDR3 SDRAM Interface where it is translated into instructions and addresses that are recognized by the DDR3 memory as an access. The stored data & addresses in the memory are read back to the Hash-CAM circuit in order to validate the match. In the case of a match, the corresponding reference address is returned.

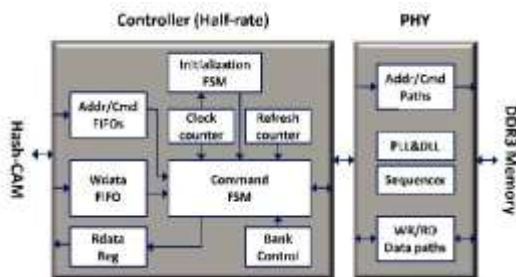


Figure 2: DDR3 SDRAM interface

As depicted in Figure 2, a complete DDR3 SDRAM interface consists of an initialization control, refresh control, command control, and a data path control circuit. The proposed DDR3 controller is responsible for generating DDR3 access commands, addresses, data and memory PHY specific control and timing order signals.

### A. DDR3 SDRAM timing & bank access control

The most important parameters of the DDR3 technology are column address strobe latency ( $t_{CAS}$ ), RAS to CAS latency ( $t_{RCD}$ ), RAS precharge time ( $t_{RP}$ ) and row active time ( $t_{RAS}$ ) [10].

The worst case row cycle time ( $t_{RC}$ ) applies for successive random accesses to different rows in a bank, where  $t_{RC} = t_{RAS} + t_{RP}$ . The DDR3  $t_{RC}$  value is usually higher than 20 clock cycles. In order to overcome the random access limitations set by  $t_{RC}$ , two successive random read accesses in a bank must therefore be avoided. To achieve this, data contents in the DDR3 memory can be duplicated into each bank and bank addresses are generated by the controller itself with respect to each active or read command. This is to guarantee that any two continuous read requests apply to different banks of the memory. In such condition, a possible data allocation scheme is illustrated in Figure 3, where  $n$  DDR3 SDRAM devices are bundled together sharing the same address inputs.



Figure 3: Data allocations in DDR3 SDRAMs

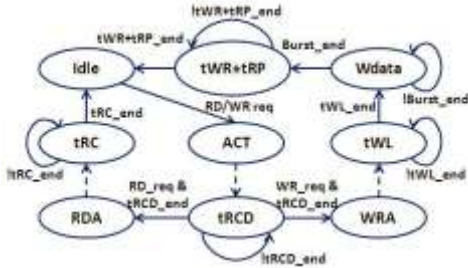
A number of burst data from each DDR3 SDRAM device is used to store the original input data as well as the reference addresses. The address of the first burst data in the DDR3 memory is calculated from the hash value of the input data. The group of the input data ( $Data[1..n]$ ) having the same hash value rest at the same address location ( $Addr(k)$ ) of different memory devices. For given table entrants, the equivalent number of memory blocks ( $k$ ) in the Hash-CAM is derived from the configuration of the DDR3 SDRAM, burst length ( $BL$ ) and the number ( $n$ ) of memory devices, which can be expressed as

$$k = n \cdot W_{DQ} \cdot BL / (W_{DATA} + W_{ADDR})$$

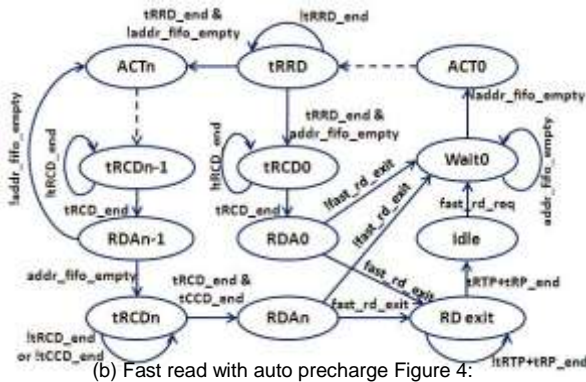
where  $W_{DQ}$  is the data width of the DDR3 SDRAM,  $W_{DATA}$  is the input data width and  $W_{ADDR}$  is the width of the reference address of the input data. After  $k$  is selected, the CAM size is then determined by calculating the percentage data collisions ( $C$ ) of the Hash-CAM

### WR/RD cycle

The command state diagram for the proposed controller is shown in Figure 4. The definitions of all timing parameters can be found in [10]. As half clock rate is applied to the controller circuit, all timing parameters of the DDR3 memory are divided by two when calculating the equivalent number of clock cycles in the state machine. Because this controller circuit is designed for table look up, write operation is not taken into the account for the lookup performance as it is only working on the table update stage.



(a) Normal write/read with auto precharge



(b) Fast read with auto precharge Figure 4: Command State Diagrams

Figure 4(a) gives the normal write/read operations with the auto precharge option. The write/read cycles must satisfy the delay parameters, such as  $tRCD$ ,  $tWL$ . With this approach, the next access must wait a certain period of time, known as  $tRC$ , until the currently opened row is closed. This results in an unnecessary delay. As discussed in Section III.A, fast read can be achieved by switching banks. Bank control logic is used to issue desired bank addresses at each cycle when a bank active command or read command is issued. The state machine for this method is given in Figure 4(b). The proposed controller provides the control interface for switching between normal write/read mode and fast read mode.

Unlike other data processing techniques, the distinct characteristic of the random data lookup is the uncertainty of the incoming data. In this work,

address FIFOs are applied to buffer the row/column addresses separately for each read request. The “empty” flag of the row address FIFO ( $addr\_fifo\_empty$ ) is checked in order to evaluate whether the next command is active ( $ACT$ ) or read ( $RDA$ ).

### C. Fast read timing

When operating in fast read mode, the input data rate is the dominant parameter that determines the command sequences. Figure 5 shows an example timing diagram of the controller commands output, with a selected DDR3 memory model.



(a) Continuous read request



(b) Discontinuous read request

Figure 5: Commands timing for fast read operation

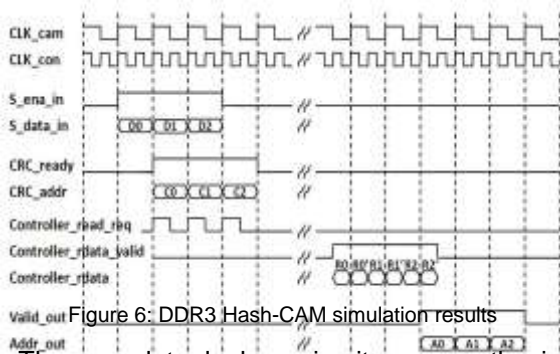
Under such conditions, this half-rate controller is ready to accept the read request at every other clock cycle. Continuous read requests apply when the input data frequency is faster than half of the controller clock frequency, as given in Figure 5(a). In this case, the controller reaches its best performance during read operations and the DDR3 data bus is fully utilised. For discontinuous read request, the memory bus efficiency is dependent on the incoming data frequency. An example is given in Figure 5(b).

Note that in this test circuit all of 8 banks from the DDR3 memory are involved in this “ACT-RDA” cycle. In other cases, fewer banks could be selected to allow more memory spaces for the data storage, as long as the time interval between two  $ACT$  commands on the same bank is less than  $tRC$ .

## IV. EXPERIMENTAL RESULTS AND ANALYSIS

In order to validate the proposed controller architecture within a data lookup application, a complete test circuit comprised of Hash-CAM block, Altera’s PHY megacore and Micron’s DDR3 memory model (MT41J128M8) are used. The prototype is designed to work at half-rate frequency of  $200MHz$  and the Hash-CAM sub-block is designed to work at quad-rate, at  $100MHz$ . The functional simulation results are shown in Figure 6. The input data ( $S\_data\_in$ ) is clocked at  $100MHz$ . For each hash value ( $CRC\_addr$ ), the DDR3 controller returns two output values in two clock

cycles at 200MHz, e.g.  $R0$  and  $R0'$ . Each output data pair ( $R0$  and  $R0'$ ) is comprised of an address and a data field, stored in the DDR3. The  $R0$  and  $R0'$  data fields are compared in parallel with the input data ( $S\_data\_in$ ). The corresponding address field of the matching data set is asserted as the final address value ( $Addr\_out$ ). The total lookup latency for each request is 15 clock cycles at 100MHz. Because the system is fully pipelined, successive address outputs are expected after 15 clock cycles at every clock cycle.



The complete lookup circuit was synthesised using Altera's Stratix III technology and tested with a 64-bit wide DDR3 module. Post-layout synthesis results are shown in Table I. The estimated on-chip power dissipation in this work is 4513.79mW.

Table I. Performance of DDR3 Hash-CAM lookup circuit

Stratix III EP3SL340H1152C3	
Hash-CAM Data width	32bits
Hash-CAM table entrants	128K
CAM-RAM depth	512
Hash function	CRC-16
Lookup Frequency	100MHz
Combinational/Memory ALUTs	16,238/512
Registers	23,549
PLLs	1
DLLs	1

The above experimental results clearly validate the expected performance of the proposed custom-purpose DDR3 controller architecture. For a given random lookup the DDR3 peak memory bandwidth can be achieved. Although the available memory space is one-eighth of the entire memory storage capacity, the look up performance was improved by at least 10 times, in comparison to the Hash-CAM circuit presented in [2].

## V. CONCLUSIONS

In this paper, an advanced DDR3 memory controller architecture for high-performance table

lookup is proposed and its deployment within a high-performance Hash-CAM based lockup circuit is presented. The design study has shown that high-performance and large lookup table circuits can be implemented using low-cost state-of-the-art FPGA and DDR3 technology. The proposed DDR3 Hash-CAM circuit is prototyped for a 128K table entry and verified for a 2Gbyte DDR3 address space. Synthesis results presented in Table I show that a CAM circuit with 104bit wide and 512-entry can be built on standard FPGA devices at 100MHz, operating frequency. Considering such an embedded CAM sub-circuit and a 2Gbyte DDR3 module, the proposed DDR3 Hash-CAM lookup architecture is capable of supporting 104bit wide and 1M-entrant TCP/IP header lookup table with a sustainable lookup performance of up to 100 million packets per second. Assuming a worst case smallest packet size of 64bytes, the proposed lookup circuit is suitable for router/switch ports for address lookup or packet classification at sustainable line-rates above 50Gbit/s.

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