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Efficient Design Of Binary Adders Using Cellular Automata

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ABSTRACT: In this paper, we propose a novel quantum-dot cellular automata (QCA) adder design and that decrease the number of QCA cells used in previous existing designs. The proposed one-bit QCA adder design is based on a new algorithm that contains three majority gates and two inverters for the binary addition. A novel 64-bit adder designed in QCA was implemented. It yields speed performances higher than the existing designs. QCA adders area requirements are comparable with the RCA and CFA. The novel adder operates in the RCA fashion, but it can propagate a carry signal through a number of cascaded MGs significantly lower than the conventional RCA adders. Our proposed QCA Adder architecture will be used as a real time Digital Counter or Clock Circuits. Here we implemented a stop watch using this QCA adder architecture.

As transistors are getting reduced in size largely and more number of transistors can be developed in a single chip, thus increasing the chip computational capabilities. However, transistors can't find much smaller than their actual size. The quantum dot cellular automata method is one of the possible solutions to overcome this physical limit, even though the design of the logic modules in QCA is not straight forward.

Keywords*: Nano Computing, Adders, Majority Gate, Inverter and QCA*

1. INTRODUCTION

Quantum-dot cellular automata (QCA) are a gorgeous rising technology appropriate for the event of radical dense low-power superior performance digital circuits. Quantum-dot cellular automata (QCA) that employs array of coupled quantum dots to develop Boolean logic function. The advantage of QCA lies within the extraordinarily high packing densities possible because of the tiny size of the dots, the simplified interconnection, and also the extraordinarily low power delay product. A fundamental QCA cell contains four quantum dots in a square array coupled by tunnel barriers. Electrons are ready to tunnel between the dots, however can't leave the cell. If two excess electrons are placed within the cell, Coulomb repulsion can force the electrons to dots on opposite corners. There are therefore two energetically equivalent state polarizations are often tagged logic "0"and "1".The basic building blocks of the QCA design structure are AND,OR and NOT. By using majority gate we are able to scale back the amount of delay, by calculative the propagation and the generation of carries.

In this paper, a new QCA adder design is developed that decreases the number of cells in QCA when compared to existing reported designs. We demonstrate that it is possible to design a CLA QCA one-bit adder, with the same reduced hardware as the bit-serial adder, as retaining the simpler triggering scheme and parallel structure of the novel CLA approach. The newly proposed design is based on a brand new algorithmic rule that needs solely three majority gates and two NOT gates for the QCA addition. It is observed that the bit-serial QCA adder uses a variant of the

proposed one-bit QCA adder. By connect proposed one-bit QCA adders.

An adder designed as suggested runs in the Ripple carry adder fashion, but it shows a computational delay lower than all state of the art competitors and achieves the lowest area-delay product (ADP).

2. REGULAR METHOD

A. Description

Multiple full adder circuits can be cascaded in parallel to feature an n-bit number. For an n- bit parallel adder, there should be n number of full adder circuits. A ripple carry adder may be a logic circuit within which the carry-out of every full adder is that the carry in of the succeeding next most important full adder. It's known as a ripple carry adder as a result of every carry bit gets rippled into succeeding stage. During a ripple carry adder the sum and carry bits of any half adder stage isn't valid till the carry in of that stage happens. Propagation delays within the logic circuitry are the reason behind this. Propagation delay is time go on between the applying of an input and incidence of the corresponding output.

Contemplate a NOT gate, once the input is "0″ the output are going to be "1″ and vice versa. The time taken by the NOT gate's output to become "0″ once the applying of logic "1″ to the NOT gate's input is due to the propagation delay here. Equally the carry propagation delay is that the time go on between the applying of the carry in signal and also the incidence of the perform (Cout) signal.

The figure below shows the RCA design.

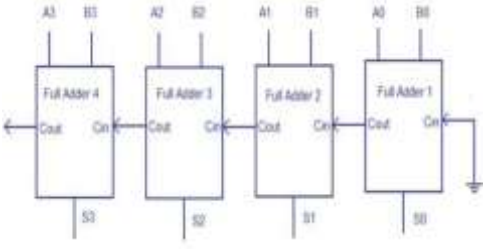

Fig1. RCA design

B. Basic Full adder block

To understand the operating of a ripple carry adder utterly, you wish to own a glance at the complete adder too. Full adder may be a logic circuit that adds two input quantity bits and a Carry in bit and outputs a perform bit and a add bit.. The add out (Sout) of a full adder is that the XOR of input quantity bits A, B and also the Carry in (Cin)bit. Truth table and schematic diagram of a one bit Full adder is shown in below. There is an easy trick to search out results of a full adder. contemplate the second last row of the reality table, here the operands square measure one, 1, 0 ie (A, B, Cin). Add them along that is 1+1+0 = 10. In binary numeration system, the quantity order is 0, 1, 10, 11……. and then the results of 1+1+0 is 10 a bit like we have a tendency to get 1+1+0 =2 in decimal number system. a pair of within the decimal number system correspond to ten within the binary numeration system. Swapping the result "10″ can offer S=0 and Cout = one and also the second last row is even.

Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

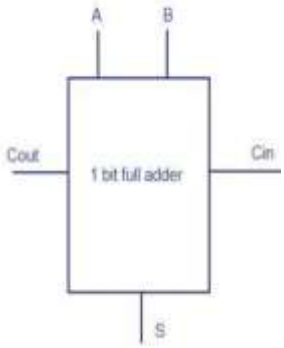

Fig2.1- bit full adder schematic and truth table

2. PROPOSED METHOD

A. BACK GROUND

I) QCA Basics:

QCA is based on the interface of bi-stable QCA cells made from four quantum-dots. A high-level style of 2 polarized QCA cells is shown in Fig. 3. Every cell is enforced mistreatment four

quantum dots organized in a square pattern. The cell is charged with 2 electrons that are freed from charge to tunnel between adjacent dots. These electrons tend to require up antipodal sites as a results of their mutual electricity repulsion. Thus, there exist 2 equal energetically lowest arrangements of the two electrons within the QCA cell as shown in Fig. 3. These 2 arrangements are termed as cell polarization P = +1 and P = -1 correspondingly. By considering cell polarization P = +1 to represent logic "1" and P = -1 to indicates logic "0", binary data can be encoded.

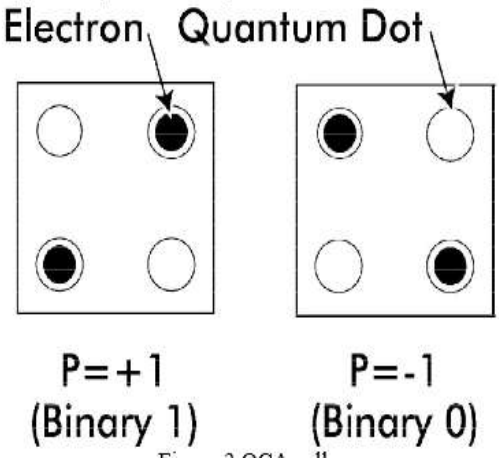

Fig 3. QCA cells

Arrays of QCA cells can be introduced to perform all Boolean functions. This results in Columbic interactions, which influences the polarization of neighboring cells. QCA designs have been proposed with potential barriers between the dots that can be controlled and used to clock QCA designs.

B. ***QCA Logical Devices***

QCA wire: In a QCA wire, the digital signal transfer from input to the output because of the Columbic connections among cells. This results in a system attempting to settle to a ground state. Any cells along the wire that are anti-polarized to the input would be at a high energy level, and would soon settle to the exact ground state. The propagation in a 90-degree QCA wire is shown in Fig. 4. Other than the 90-degree QCA wire, a 45-dgree QCA wire can also be used. In this case, the propagation of the digital signal fluctuates between the two polarizations. Advance, there exists a so-called non-linear QCA wire, in which cells with 90-degree orientation can be placed next to one more, but off center.

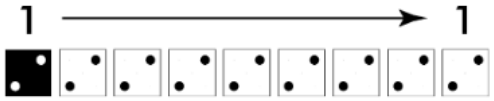

Fig4. A QCA wire (90-degree)

Majority gate and NOT gate : The majority gate and NOT gate are shown in Fig. 5 and Fig.6 respectively. The majority gate performs a three-input Boolean operation. Forward the inputs are A, B and C, the logic operate of function gate is

$$m(A, B,C) = A|B + B|C + A|C \quad (1)$$

By fixing the polarization of one input as logic "1" or "0", we can get an OR gate and an AND gate consequently. More complicated logic circuits can then be designed from OR and AND gates.

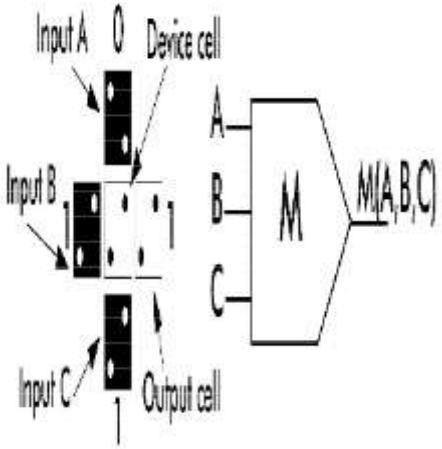

Fig5.A QCA majority gate

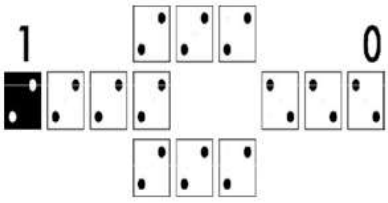

Fig.6.A QCA inverter

C. QCA Full Adders

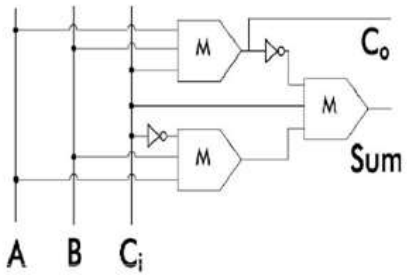

Fig.7. one-bit QCA full adder

D.PROPOSED STRUCTURE

A QCA is a nano-structure contains basic cell a square of four quantum dots structure filled with two free electrons able to tunnel through the dots inside the cell. Because of Coulombic repulsion, the two electrons will accommodate in opposite corners. The locations of the electrons in the cell give two possible stable states that can be related to the binary state 1 and 0.

Although beside cells interact through electrostatic forces and tend to arrange in a line their polarizations, QCA cells do not exhibit intrinsic data flow directionality. To achieve controllable data directions, the cells inside a QCA design are divided into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90°. This clock system named the zone clocking scheme, makes the QCA designs intrinsically pipelined, as each clock zone behaves like a D-latch. QCA cells are used for both logic designs and interconnections that can exploit either the coplanar cross or bridge technique. The fundamental logic gates inherently available within the QCA technology are the NOT gate and the MG. Given three inputs a, b, and c, the MG perform the logic function reported in (1) provided that all input cells are associated to the same clock signal clkx (with x ranging from 0 to 3), whereas the remaining cells of the MG are linked to the clock signal clkx+1.

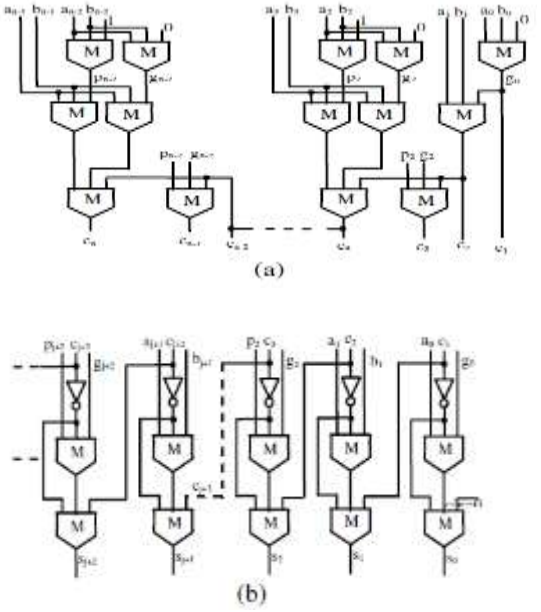

Fig8: Novel n-bit addition (a) carry block and (b) sum block

Several designs of adders in QCA exist in literature. The RCA and the CFA process n-bit operands by cascading n full-adders (FAs). Even although these addition circuits use different topologies of the generic FA, they include a carry-in to carry-out path consisting of one MG, and a carry-in to sum bit path contain two MGs plus one inverter. As aim portended, the worst case computational paths of the n-bit RCA and then-bit CFA consist of (n+2) MGs and one inverter. A CLA design formed by 4-bit slices was also presented. In particular, the auxiliary propagation and generation signals, termed as pi =ai +bi and gi=ai.bi, are compute for each bit of the operands and then they are grouped four by four. Such a designed n-bit CLA has a computational path composed of 7+4×(log4n) cascade MG' s and one inverter. This can be easily verified by observing that, given propagate and generate signals, to compute grouped Log4n propagate and grouped generate signals; four cascade MGs are introduced in the computational path. In addition, to calculate the carry signals, one level of the CLA logic is required for each factor of four in the operands word-length. This means that process n bit addends, log levels of CLA logic are required, every contributing to the computational path with four cascaded MGs. Finally, the calculation of sum bits introduces two further cascaded MGs and

one inverter. The parallel-prefix BKA demonstrated exploits more efficient basic CLA logic designs. As its main advantage over the previously describe adders, the BKA can achieve lower computational delay.

E.NOVEL QCA ADDER

The below figures shows the 16-bit and 32 bit QCA adders

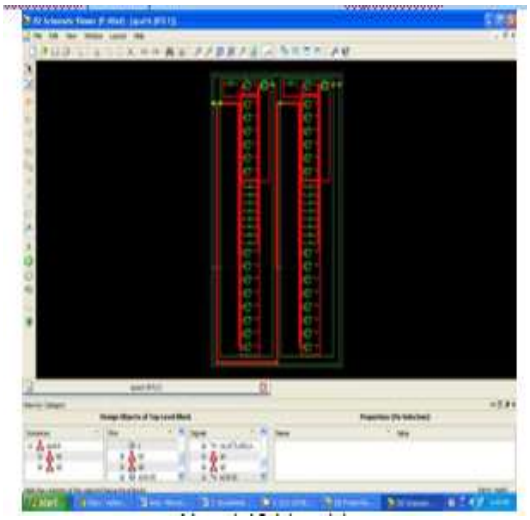

Fig9: Novel 16-bit adder

Fig10: Novel 32-bit adder

3. SIMULATION RESULTS

The proposed addition design is implemented for several operands word lengths using the QCA Designer tool adopting the same rules and simulation settings used.

Fig11. Block diagram of QCA

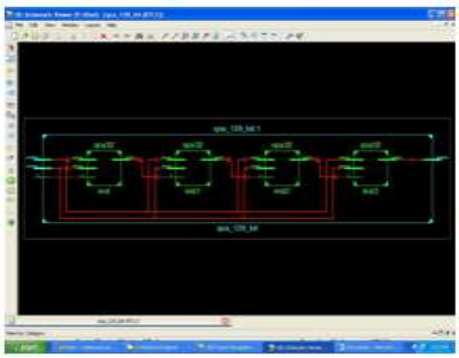

Fig12: RTL schematic

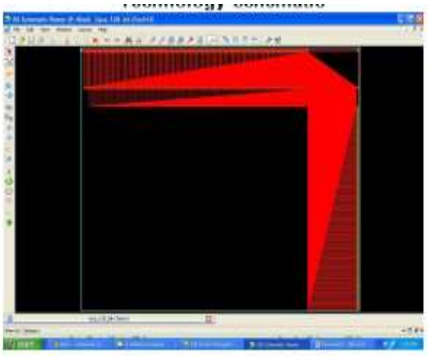

Fig13: Technology schematic

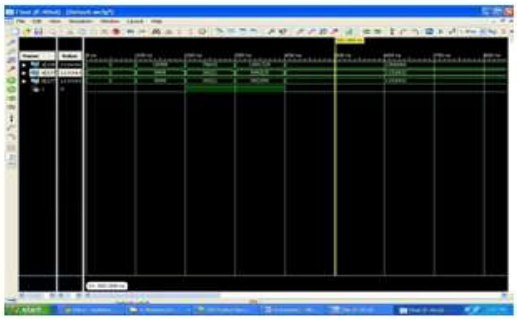

Fig15: SIMULATION RESULT

4. ENHANCEMENT:

Our proposed QCA Adder architecture will be used as a real time Digital Counter or

Clock Circuits. We can implement a stop watch using this QCA adder architecture

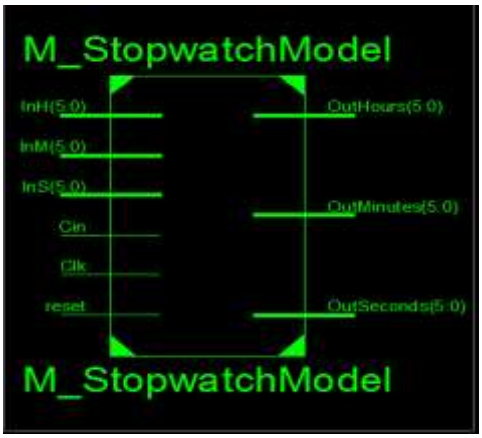

Fig 15: RTL Schematic

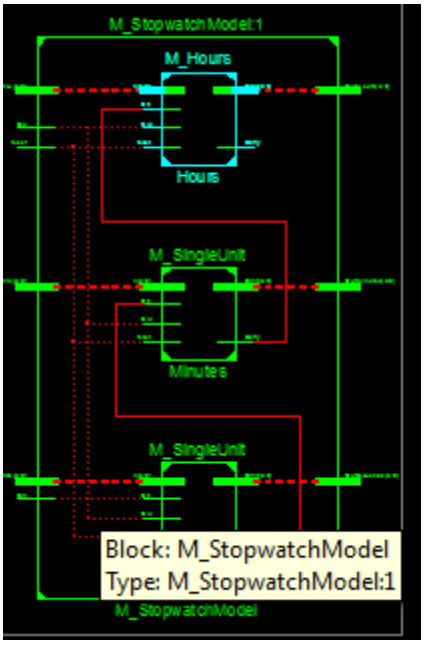

Fig 16: RTL Schematic Internal Structure

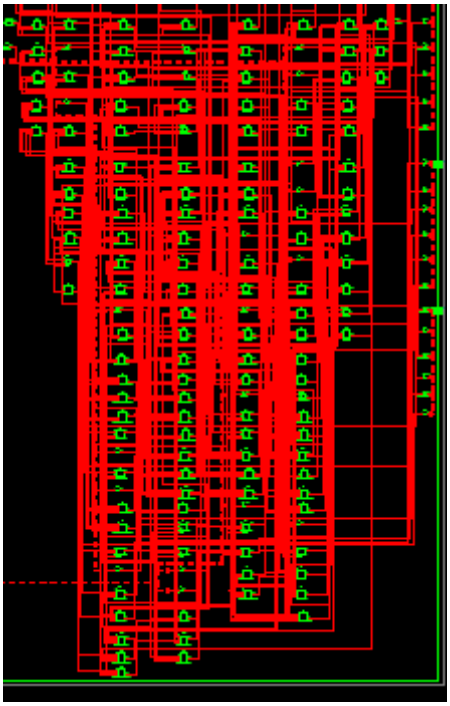

Fig 17: Technology Schematic

Fig 18: Design Summery

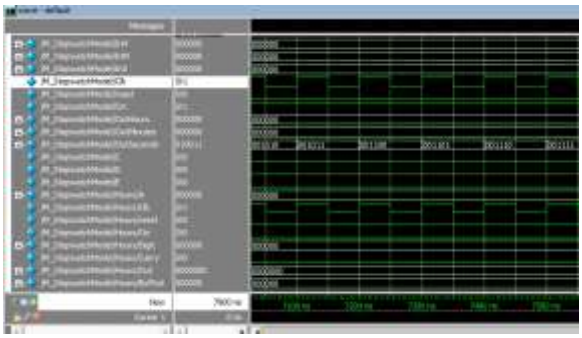

Fig 19: Simulation Result

5. CONCLUSION

A new adder designed in cellular automata was implemented. It achieved speed performances higher than all the existing QCA adders with a neighborhood demand comparable the RCA and

CFA demonstrated. The novel adder operated in the Ripple carry adder fashion, but it could propagate a carry signal through variety of cascaded MGs considerably lesser than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the amount of clock cycles needed for finishing the reason was restricted. A 64-bit binary adder designed as described, and using this architecture we implemented a real time application such as stop watch in this brief.

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