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Optimization Of Cmos Circuits By Using Quaternary Logic LUT

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Abstract: *Now a days due to Interconnections the delay will increase in design of a circuit. The more number of interconnections leads to increase in the area of the circuit due to this the power consumption also more in COMS digital circuits. Multiple-valued logic can reduce the average power required for level transitions and reduces the number of interconnections for the design, hence also reducing the effects of interconnections on overall power consumption. In this paper, we propose quaternary lookup table (LUT) architecture was designed to replace or complement binary LUTs in field programmable gate arrays. The circuit is implemented with the CMOS processes, with a single voltage supply and voltage mode structures.*

A clock boosting technique is used to improve the performance of the design. The proposed implementations can overcome the all drawbacks which are previously published in the quaternary logic. For this design such as the need for special features in the CMOS process or power hungry current-mode cells . We implements a full adder prototype based on the designed LUT, fabricated in a standard 130-nm CMOS technology, able to work at 100 MHz while consuming 122 µW. The performance results will be comparing with the all existing systems.

Keywords- *Multivalve logic, Lookup table(LUT)*
Field Programable Gate Array(FPGA),Quaternary logic

I. INTRODUCTION

IN All Binary digital circuits by using CMOS technology, power consumption is determined by two types Static power consumption and Dynamic power consumption. The Static Power Consumption is more related to leakage currents if leakage currents are more then the static power consumption also high. The Dynamic power consumption is measured by using the formula mentioned below

PD = cvDD2.

Here ***C*** is the load capacitance for the nodes being driven in the design and ***VDD*** is the supply voltage. The Designing of CMOS circuits and performance are improved by using the minimization of the transistor sizes and by lowering the supply voltage, therefore saving the energy , optimize the power consumption and integrate the more functionality into the same area. However the capacitance C also includes the routing capacitance associated with load of the circuit and connect the logic circuits in the buses form. This is particularly observe in the modern FPGAs in this FPGAs the wastage of power will be reaches up to 70% of the total power consumption. Due to the functionality of Reconfigurability in FPGAs we can develop the all modern digital system designs good performance and less cost while compare with the Application-specific integrated circuit (ASIC).

An approach to moderate the effect of inter-connections by using the Multi-valued logic (MVL).multi value means more than single value there are different multi logic methods are used in the design of digital circuits. Multi value logic is the half way between binary logic and signal processing in multi value logic we can perform the operations by using more than two discrete levels. Multi value logic can be implemented either in Voltage Mode Logic(VML) or in Current Mode Logic(CML).

In Voltage mode circuits number of signal levels is limited by the power supply voltage and signal-to-noise ratio, where as in current mode circuit number of signal levels is limited by resolution of current comparators and signal-to-noise ratio for given technology.

The different multi valued methods are present using in the design of digital circuits are

1) Binary Logic(0 or 1)
2) Ternary Logic(1,0,-1)
3) Quaternary Logic(0,1,2,3)

These are all the different Multi valued logic methods.

Therefore in multivalued logic the power consumption can be minimized because the level transition is closer compare with single valued logic so the power consumption can be determined in the multivalued logic by using the below formula

PD α CVDDVav

Here Vav is the average power required for the level transition from one voltage level to other level. More Details about the determination of the energy consumption in Quaternary logic buses and a comparison to their binary logic, it is known that the use of MVL comes at the price of having relatively less noise margin than the binary therefore its use ia not trusted. there is still large and foreseeable room for power optimization exploiting the shrinking and supply voltage reduction of CMOS devices. The current mode multi-valued logic (CMVL) produces the high energy consumption due to high leakage current of the circuit to overcome this we go for Voltage mode multi-valued logic(VMVL).

In this paper we proposes a design of multi value logic circuit by using look up table(LUT) design in the Quaternary logic representation that uses a simple voltage mode standard CMOS circuits and improves the performance by using the clock boosting(CB) technique to reduce the switching resistance and optimize the delay and area. In our implementation we uses a single voltage supply and design of look up table by using the quaternary logic and by using QLUT design the Quaternary Half adder and Full adder compare the Simulation results and synthesis report with the results of binary logic.

Basically this paper organizes the following sections.

I) Abstract
II) Introduction
III) Quaternary logic and lookup table
IV) Existing methods
V) Proposed method and Implementation
VI) QLUT Half Adder
VII) QLUT Full Adder
VIII) Simulation and synthesis results
IX) Compare the results of both existing and proposed methods
X) Conclusion

II. QUATERNARY LOGIC AND LOOK UP TABLE

A quaternary variable can assume four different logic levels. Assuming a rail-to-rail voltage range and equal noise margins for the four logic levels, three different reference voltage values are required, 1⁄6V_{DD}, 3⁄6V_{DD}, and 5⁄6V_{DD}, to determine a quaternary value. This is shown in figure below. Since a quaternary variable (Q) is able to carry twice as much information as a binary variable (B), we have the following relation:

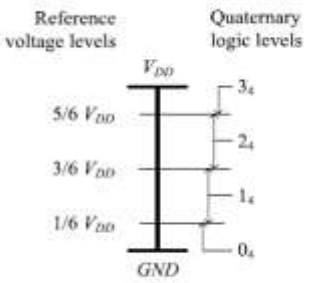


Fig. 1. Quaternary logic and reference voltages levels.

a. $|Q| = 2 \times |B|$.

Therefore, two binary variables may be grouped into one quaternary variable without information loss, merging two nodes into one. It should be noted that there is no direct conversion of binary to quaternary logic gates in conventional CMOS, since the binary circuits use the available power rails to represent the binary symbols. For quaternary logic there are two more intermediate levels, which cannot be obtained directly using the same techniques. On the other hand, viable implementations of quaternary circuits have already been achieved for LUTs. A LUT is an array indexing operator, where the output is mapped by the input, based on the configuration memory. The configuration values are initially stored in the LUT configuration memory, and according to the input, the logic value in the addressed.

position is assigned to the output. By properly programming the LUT configuration memory, the LUT can implement any logic function with the given number of inputs and outputs.

A quaternary function implemented by a QLUT is defined as $g : Qk \rightarrow Q$, over a set of quaternary input variables $Y = (y0, \ldots, yk-1)$, where the values of a variable yi and the function $g(Y)$ are defined in $Q = \{0, 1, 2, 3\}$. In general, if l is the number of logic levels, the total number of different functions $|F|$ that can be implemented in a LUT is given by

$$|F| = l|n \times lk|$$

where n is the number of outputs and k is the number of inputs. For a LUT with a single output ($n = 1$), the number of different functions for binary ($l = 2$) and quaternary ($l = 4$) representations is given, respectively, by

$$|F2| = 22k = 4k \; |F4| = 44k = 256k.$$

The number of possible functions that may be represented in a quaternary LUT is much larger than in a binary LUT with the same number of inputs and outputs. Therefore, apart from reducing the total number of connections, MVL also leads to a reduction of the total number of gates when compared with a binary implementation.

III. EXISTING METHODS

In this paper we over come the drawbacks of the Binary logic and Binary lookup table and design of digital circuits. Binary logic is nothing but the using the numbers either ‘0’ or ‘1’.the look up table is nothing but the array indexing operator and inputs driven by the outputs. The lookup table

can be used in the design of the FPGAs. The drawbacks of the binary logic is nothing but the we can implement less number of functions this leads to larger area required to design large functions and more delay and energy consumption also more for designing of digital circuits, to overcome all these we go for a logic called Quaternary logic.

IV. PROPOSED METHOD AND ITS ARECHITECTURE

The proposed 2-input 1-output QLUT is shown in Fig. 2. or this given QLUT complexity, 16 quaternary configuration inputs are necessary, one for each possible combination of the two quaternary inputs. The configuration word defines the reconfigurable quaternary function. In practice, the input signals are used to select which one of the configuration inputs is connected to the output. The proposed QLUT is composed of two main blocks: a 16-1 multiplexer using an array of switches, that establishes a low-resistance path between one configuration input and the output according to the input values; and a quaternary-to-binary decoder, consisting of a 2-bit analog-to-digital (ADC) frontend followed by combinational logic used to generate the control signals feeding the multiplexer. These blocks are described in the following sections.

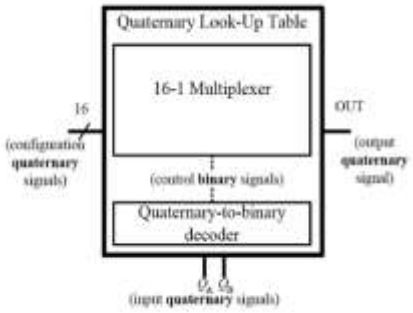


Fig. 2. Proposed quaternary LUT.

V.I. 16-1 Multiplexer

Due to the quaternary nature of its inputs, the 16-1 multiplexer shown in Fig below may be thought of as an analog multiplexer. The output is assumed to be of a capacitive nature and its value is defined by the interconnection network to which the QLUT output is connected. For a binary FPGA this value can go up to tens of pF [10]. Although, the use of quaternary logic allows to reduce the number of wires, leading to a compact layout, reducing the routing capacitance. We used the typical value for a binary FPGA (10 pF), since it allows us to consider that maintaining the same number of wires, we can increase the functionality within the FPGA. The multiplexer path is usually implemented by transmission gates (TGs), which can be modeled by a simple RC circuit, as shown in Fig. 3. The charging time is proportional to the RC time constant, and since the capacitance is already constrained, the only way to reduce propagation delay is to decrease the switch resistance. The straightforward approach to reduce the switch resistance is to increase the transistors width. On the other hand, this increases the gate capacitance, leading to a power increase to turn it on. Moreover, TGs are known to behave worse when the signals are far from the supply rails . This is particularly severe for the intermediate levels in quaternary signals, since there is a reduced overdrive voltage on the MOS transistors. We evaluated two techniques to implement the multiplexer switches, the use of a CMOS TG, Fig. 3(a), and the use of a single nMOS transistor controlled by a CB circuit, Fig. 3(b), which was the implemented solution

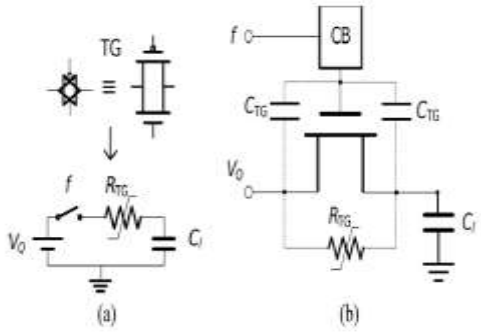
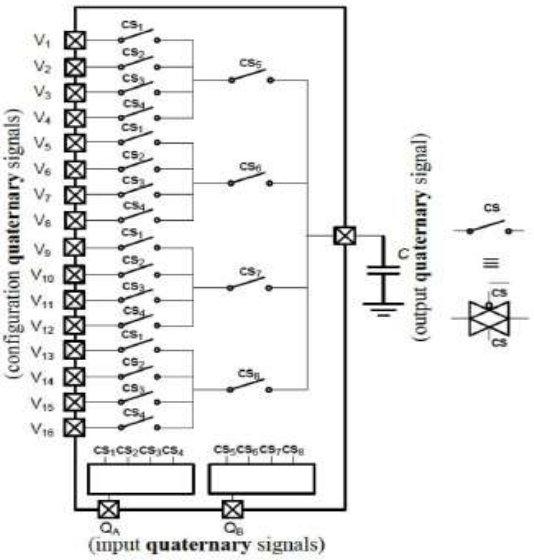
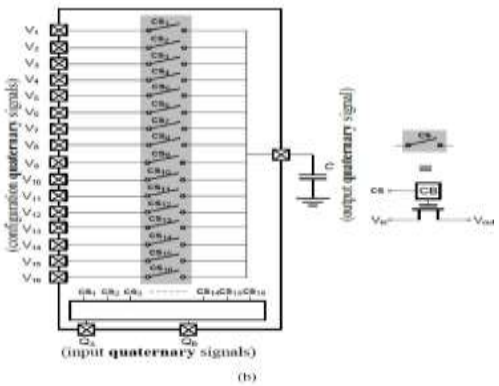


Fig. 3. (a) Multiplexer path RC model. (b) CB switch.





V.II. Quaternary-to-Binary Decoder

The 2-bit quaternary-to-binary decoder allows the use of a single row of switches to drive the input configuration signals to the output of the QLUT. To do so, it

is necessary to generate 16 control signals, to be applied in the clk1 inputs of each switch, shown in Fig. 5(c). These switches are employed to connect one quaternary configuration input to the output. To generate the required control signals, the quaternary variables are decoded into binary, allowing the use of binary logic gates. Thus, an ADC frontend is necessary, considering the analog nature of the quaternary signals. We have implemented inverting self-referenced comparators, shown in Fig. 6, where *Qi* is a quaternary input of the QLUT. The main advantage of this structure, also used in, over previously proposed implementation is that it only uses standard CMOS structures.

VI . QLUT HALF ADDER

Half adder in nothing but the adding of two numbers in quaternary logic we are measure 16 combinations by using QLUT half adder. The architecture of the QLUT Half Adder and logic table is shown in figure below.

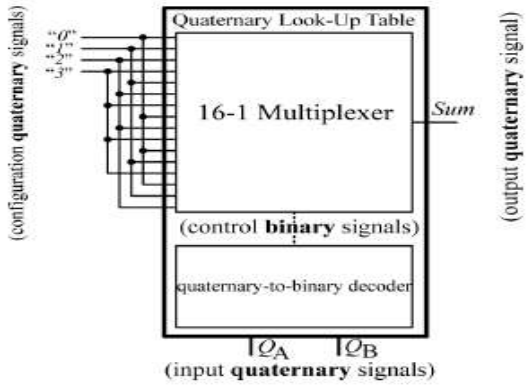


Fig. 10. QLUT half adder high level configuration.

TABLE V

HALF ADDER LOGIC FUNCTION

Q_A	0_4	0_4	0_4	0_4	1_4	1_4	1_4	1_4	2_4	2_4	2_4	2_4	3_4	3_4	3_4	3_4
Q_B	0_4	1_4	2_4	3_4	0_4	1_4	2_4	3_4	0_4	1_4	2_4	3_4	0_4	1_4	2_4	3_4
Sum	0_4	1_4	2_4	3_4	1_4	2_4	3_4	0_4	2_4	3_4	0_4	1_4	3_4	0_4	1_4	2_4

From the above architecture we observe that the QLUT working as a half-adder and the logic table shows the operation about the half-adder from the logic table we can derive the equation for the sum.

Sout = {1[(a0)(b1)] + [(a1)(b0)] + [(a2)(b3)] + [(a3)(b2)] } + {2[(a0)(b2)] + [(a1)(b1)] + [(a2)(b0)] + [(a3)(b3)]} + {3[(a0)(b3)] + [(a1)(b2)] + [(a2)(b1)] + [(a3)(b0)]} .

The QLUT Half adder are designed by using verilog HDL and Observe the Simulation results and Synthesis report and note down the values of area, delay and power consumption

VII . QLUT FULL ADDER

In this section, we employ the proposed QLUT to implement a full adder. The conventional and direct approach would require four QLUTs to properly implement this function, two QLUTs for each output, sum and carry out, working with the two possible values of the carry in. However, we propose minor modifications to the designed QLUT, which allows the reduction of the number of QLUTs only to two. This is achieved at the cost of a slight increase in binary combinational logic and a 2-1 multiplexer, as shown in Fig. 12. These modifications do not affect the original reconfigurability and functionality of the circuit as a regular QLUT.

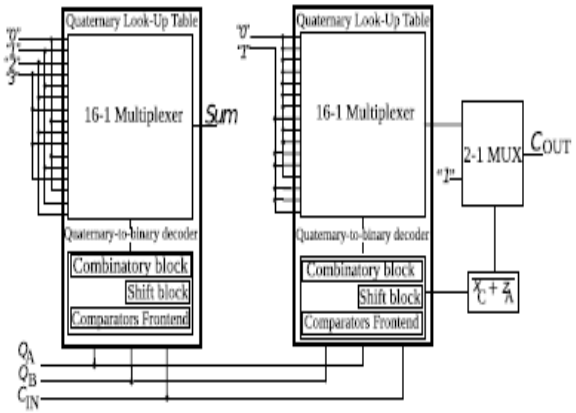


Fig. 12. QLUT full adder high level configuration.

TABLE VI

FULL ADDER LOGIC FUNCTION

Q_A	Q_B	C_{IN}	*Sum*	C_{OUT}	Q_A	Q_B	C_{IN}	*Sum*	C_{OUT}
0_4	0_4	0_4	0_4	0_4	0_4	0_4	1_4	1_4	0_4
0_4	1_4	0_4	1_4	0_4	0_4	1_4	1_4	2_4	0_4
0_4	2_4	0_4	2_4	0_4	0_4	2_4	1_4	3_4	0_4
0_4	3_4	0_4	3_4	0_4	0_4	3_4	1_4	0_4	1_4
1_4	0_4	0_4	1_4	0_4	1_4	0_4	1_4	2_4	0_4
1_4	1_4	0_4	2_4	0_4	1_4	1_4	1_4	3_4	0_4
1_4	2_4	0_4	3_4	0_4	1_4	2_4	1_4	0_4	1_4
1_4	3_4	0_4	0_4	1_4	1_4	3_4	1_4	1_4	1_4
2_4	0_4	0_4	2_4	0_4	2_4	0_4	1_4	3_4	0_4
2_4	1_4	0_4	3_4	0_4	2_4	1_4	1_4	0_4	1_4
2_4	2_4	0_4	0_4	1_4	2_4	2_4	1_4	1_4	1_4
2_4	3_4	0_4	1_4	1_4	2_4	3_4	1_4	2_4	1_4
3_4	0_4	0_4	3_4	0_4	3_4	0_4	1_4	0_4	1_4
3_4	1_4	0_4	0_4	1_4	3_4	1_4	1_4	1_4	1_4
3_4	2_4	0_4	1_4	1_4	3_4	2_4	1_4	2_4	1_4
3_4	3_4	0_4	2_4	1_4	3_4	3_4	1_4	3_4	1_4

VII.1. QLUT With Shift

Table shows the full adder truth table. It may be inferred that the results for the Sum and *C*OUT signals may be easily obtained through logic shifts on the inputs. The shift block is implemented for one of the inputs and performs a single up-shift on the input quaternary value. Using the two QLUTs configured with the results when *C*IN is 0, as shown in Table VI, it is observed that the result with *C*IN 1 can be obtained, for the Sum, by up shifting one level on *QB*. For *C*OUT, the same reasoning can be performed leading to an up shift of one level on the variable *QA*, which corresponds to a shift of four levels on the *C*OUT output, with exception when *QA* has the level 3, which is handled by combining the *yC* and *z A* (which are 0 when *C*IN has the

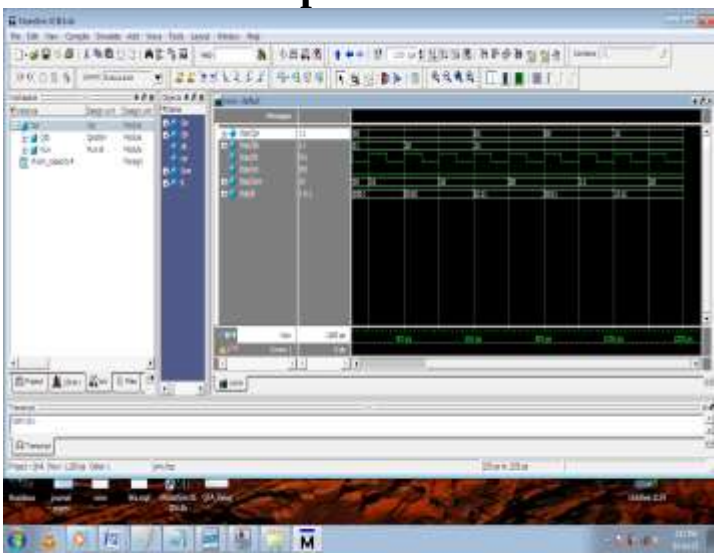
level 1 and *QA* has the level 3) on a NOR to control the 2-1 multiplexer. This block is implemented with two 2-input NAND gates, four inverters and two 2-input NOR gates.
The required logic to perform the shifts and to decode the *C*IN is added to the QLUT. These blocks are implemented keeping area and energy consumption as low as possible while satisfying the delay constraints. Moreover, to convert the quaternary variable *C*IN into binary, we added a comparator CP and an inverter to the comparators frontend, as shown in Fig. 13. This extra block represented an increase of 5% on the QLUT area.

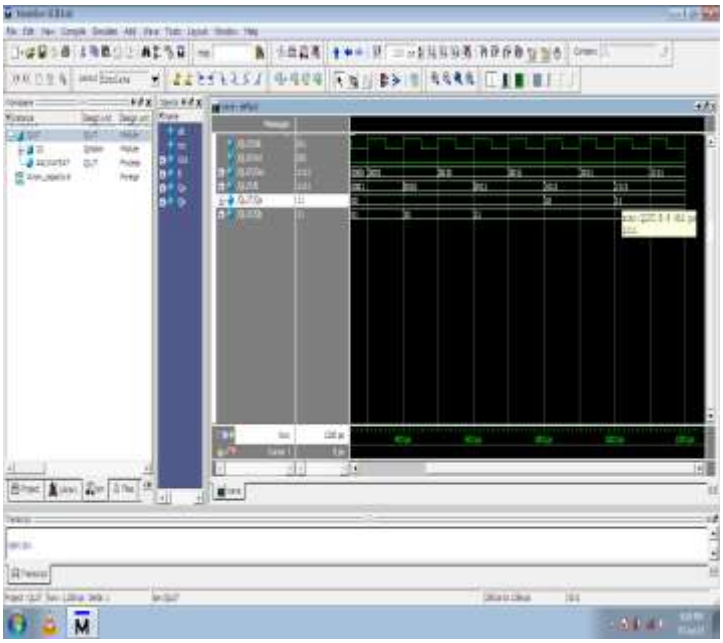
This decoder replaces the previous designed one and this new QLUT is simulated for timing nalysis. The power consumption for this modified QLUT is 36.5 μW, which reveals an overhead of 5.2% in power consumption, when compared with the non modified QLUT.

VIII. SIMULATION AND SYNTHESIS RESULTS

The simulation and synthesis reports of the proposed circuits are shown in below, the simulation can be done by using the MATLAB Simulation Tool and synthesis report and power report can be measured by using XILINX 10.2i software.

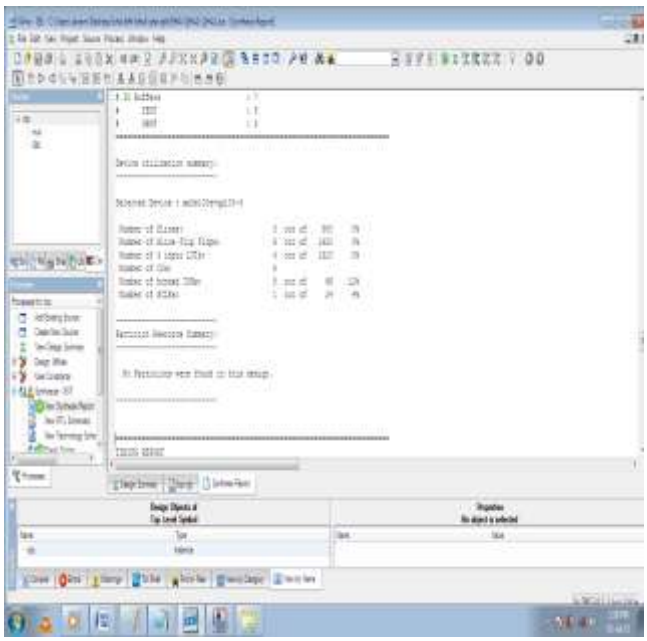
QLUT HALFADDER Simulation Reports:



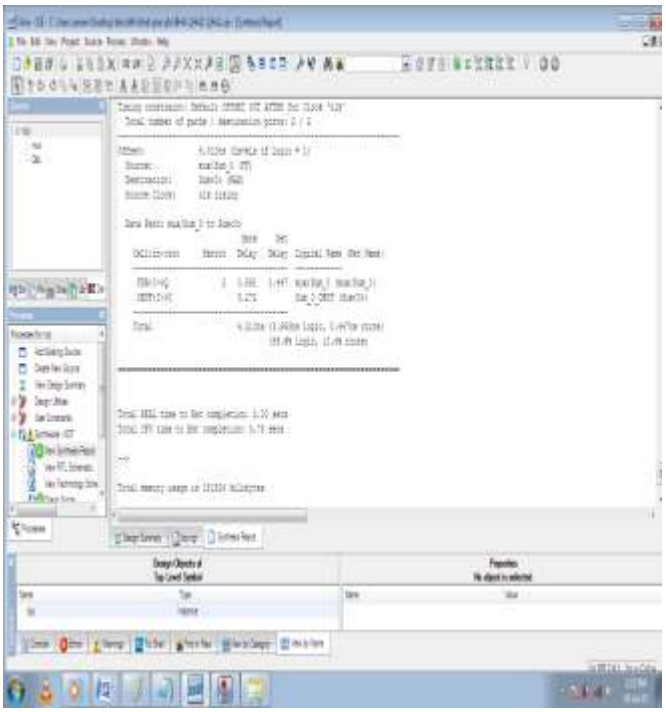


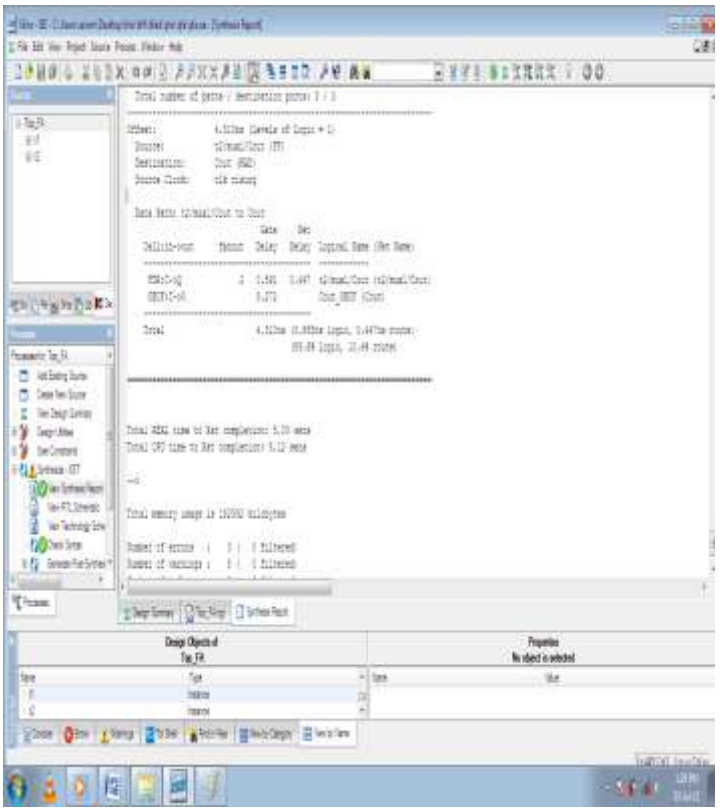
Synthesis Report:

QLUT HALFADDER:

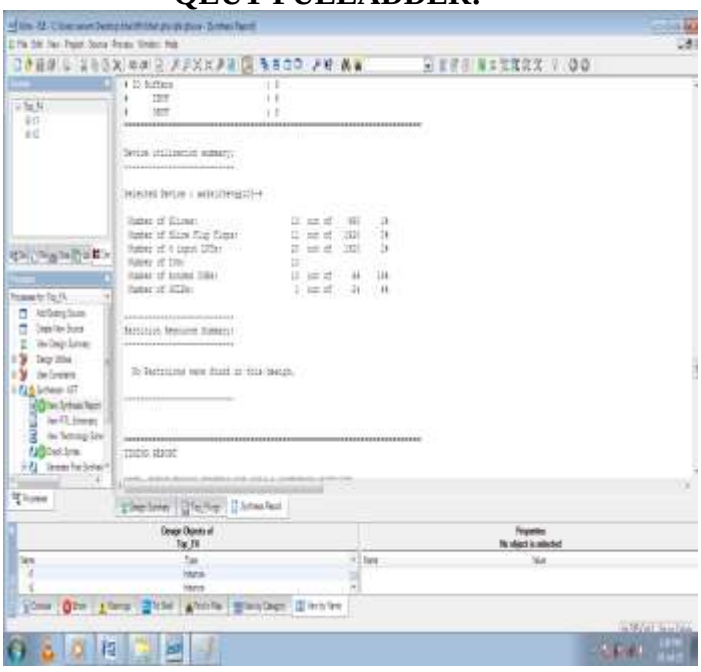


QLUT FULLADDER



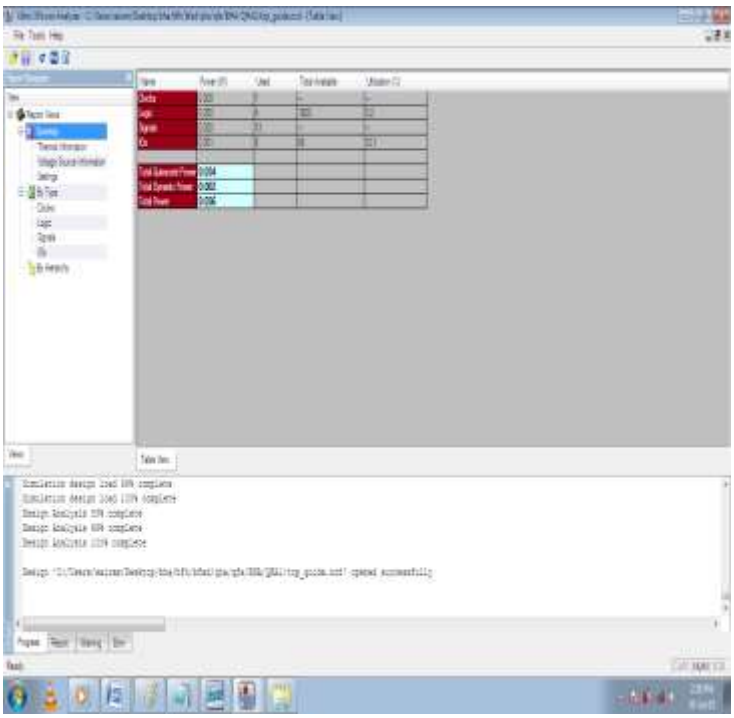


QLUT FULLADDER:

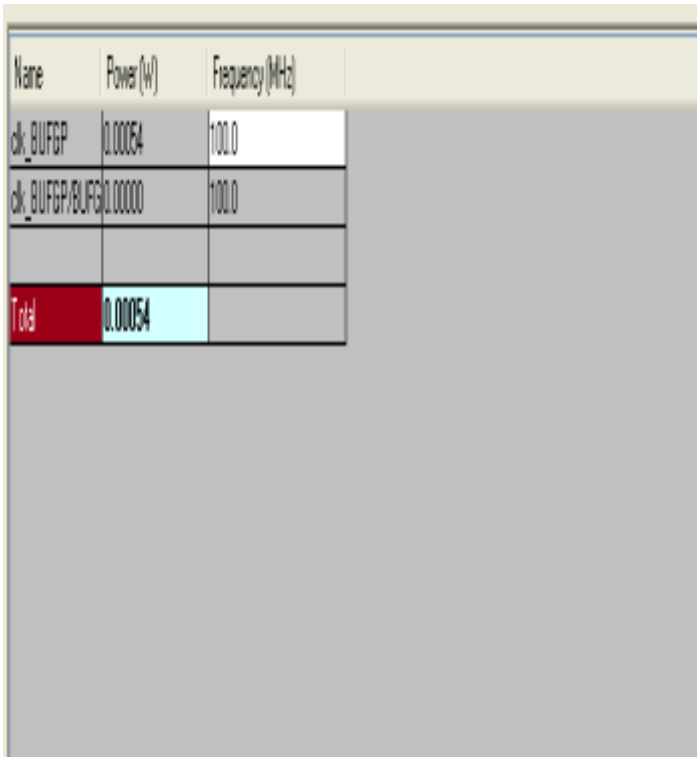


POWER REPORT:

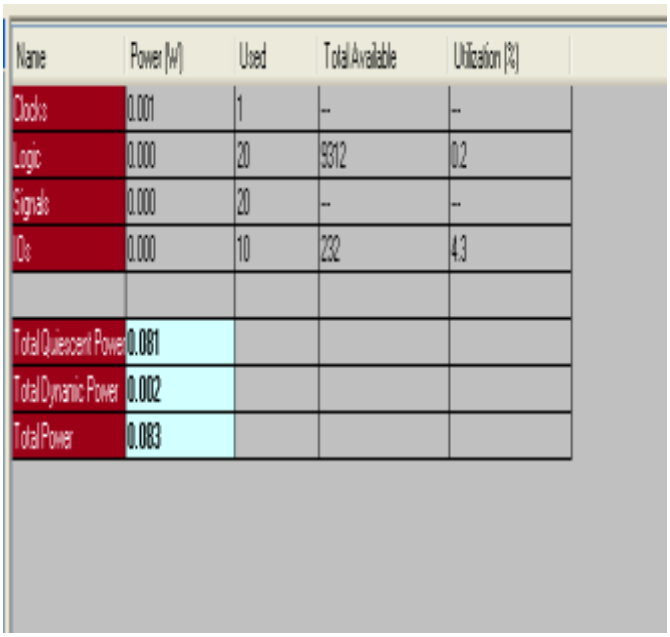
QLUT HALFADDER



QLUT FULLADDER:



Name	Power (W)	Frequency (MHz)
clk_BUFGP	0.00054	100.0
clk_BUFGP/BUFG	0.00000	100.0
Total	0.00054	



Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.001	1	--	--
Logic	0.000	20	9312	0.2
Signals	0.000	20	--	--
IOs	0.000	10	232	4.3
Total Quiescent Power	0.081			
Total Dynamic Power	0.002			
Total Power	0.083			

TABULAR COLUMN

The below table will shows the comparison between the Binary look up table logic and Quaternary lookup table logic

FACTOR	BINARY LOGIC(HALF ADDER)	QUATERNARY LOGIC(HAF ADDER)
DELAY	**4.28ns**	**4.06ns**
POWER	**35uw**	**36uw**
AREA	**7% of total area**	**12% of total area**
CLOCK FREQUENCY	**100MHZ**	**100MHZ**

FACTOR	BINARY LOGIC LUT (FULL ADDER)	QUATERNARY LOGIC LUT (FULL ADDER)
DELAY	4.35ns	3.95ns
POWER (uw)	65	84
AREA	9% of total area	16% of total area
CLOCK FREQUENCY	100MHZ	100MHZ

IX. CONCLUSION

We have reported an innovative QLUT design that can be used for multiple valued ombinational logic, this feature is achieved through a quaternary-to-binary decoder that quantize the input signals. While at the same time, achieving low power consumption, therefore, the presented design is a valid solution to reduce the interconnections impact, without increasing power consumption or losing performance Experimental results were performed on an ASIC implementation of a full adder employing the designed QLUT. The obtained results attested the circuit feasibility and its advantages, and its main characteristics (timing and power). in future we will implement this in many digital circuits in our dialy life appliances. By using QLUT Full adder we can design the Ripple Carry Adder for Extension.

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