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FPGA Design Of High Throughput STBC-OFDM System For Low Power Applications

Mr.A.Muthumanicckam [1] , Mrs.R.Sornalatha[2],Mr.L.Vijay prabakaran

[1]Assistant prof of Electronics & Communication Eng, Shanmuganathan Engineering college, Arasampatti.

[2]UG SCHOLAR,Shanmuganathan Engineering college,Arasampatti.

Emails: [1]muthumanicckam@gmail.com, [2]rslece@gmail.com

Abstract: This proposes a space time block code orthogonal frequency division multiplexing downlink baseband receiver for mobile wireless metropolitan area network. The proposed baseband receiver applied in the system with two transmit antennas and one receive antenna aims to provide high performance in outdoor mobile environments. It provides a simple and robust synchronizer and an accurate but hardware affordable channel estimator to overcome the challenge of multipath fading channels. The coded bit error rate performance for 16 quadrature amplitude modulation can achieve less than under the vehicle speed of 120 km/hr. The proposed baseband receiver designed in 90-nmCMOS technology can support up to 27.32 Mb/s uncoded data transmission under 10MHz channel bandwidth. It requires a core area of mm and dissipates 52.00 mW at 78.4 MHz with 1 V power supply. *Index Terms*—Baseband receiver, channel estimator, space time block code-orthogonal frequency division multiplexing (STBC-OFDM) system, synchronizer, wireless metropolitan area network (WMAN).

I. INTRODUCTION

Next generation portable Internet services require high data rate and mobile capability to provide various multimedia transmissions. IEEE 802.16e standard which usually refers to mobile worldwide interoperability for microwave access (WiMAX) is an extension of IEEE 802.16–2004 for providing mobility of wireless metropolitan area network(WMAN]. It is based on an orthogonal frequency division multiple access (OFDMA) technique to support multiple access scheme and multiple-input multiple-output(MIMO) systems over multipath fading channels. Space time block code-orthogonal frequency division multiplexing(STBC-OFDM) systems with multiple antennas can provide diversity gains to improve transmission efficiency and quality of mobile wireless systems but accurate channel state information (CSI) is required for diversity combining, coherent detection, and decoding. Moreover, the system performance is also sensitive to the synchronization error. Therefore, high quality synchronization and channel estimation are two crucial challenges for realizing a successful STBC-OFDM system in outdoor mobile channels.

MAJOR PARAMETERS OF THE PROPOSED STBC-OFDM SYSTEM
RF frequency
Bandwidth
Sampling frequency
Sampling factor
FFT size
Subcarrier spacing

Parameters		Values
RF frequency		2.5 GHz
System channel bandwidth (BW)		10 MHz
Sampling frequency (F_S)		11.2 MHz
Sampling factor		28/25
FFT size (N)		1024
Subcarrier spacing (Δf)		10.9 kHz
Useful symbol time (T_b)		91.4 μs
Guard time (T_g)		11.4 μs
OFDM symbol duration (T_s)		102.9 μs
Number of OFDM data symbols in a DL sub-frame		40
DL PUSC	Number of pilot subcarriers (N_{Pilot})	120
	Number of data subcarriers (N_{Data})	720

In this paper, an STBC-OFDM downlink baseband receiver for mobile WMAN is proposed and implemented. First, a novel match filter is proposed to precisely detect symbol boundary. Moreover, a ping-pong algorithm is presented to improve the performance of carrier frequency synchronization. Then, we propose a two-stage channel estimator to accurately estimate CSI over fast fading channels. The initialization stage uses discrete Fourier transform (DFT)-based channel estimation with the multipath interference cancellation (MPIC)-based decorrelation to identify significant channel paths. The tracking stage uses decision-feedback (DF) DFT-based channel estimation with Newton's method to track the gain variations of these paths. The proposed baseband receiver designed in90-nm CMOS technology can support up to 27.32 Mbps downlink(uncoded) data transmission under 10 MHz channel bandwidth. This design has a core area of mm and dissipates68.48 mW at 78.4 MHz operating frequency. This paper includes the following features:

Provision of a STBC-OFDM downlink baseband receiver
Architecture that is capable of high-speed transmission at high mobility controls the voltage being fed to the induction motor

and hence the efficiency optimization is obtained to achieve the task of energy saving.

Integration of a simple and robust synchronizer and an accurate but hardware affordable channel estimator to overcome the challenge of outdoor fast fading channel

Implementation of a successful STBC-OFDM downlink Baseband receiver for mobile WMAN.

II. STBC – OFDM

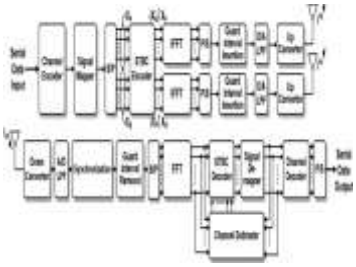


Fig. 1. Proposed STBC-OFDM systems with two transmit antennas and one receive antenna.

The proposed STBC-OFDM system is based on IEEE 802.16e OFDMA specification and supports the distributed Subcarrier allocation of partial usage of sub channels (PUSC) for downlink (DL) transmission. The major parameters are Summarized. The fast Fourier transform (FFT) size is set to 1024. The length of cyclic prefix (CP) is 128 sampling periods. The modulation schemes of quadrature phase shift keying (QPSK) and 16quadrature amplitude modulation (16QAM) are supported for data subcarriers, while binary phase shift keying (BPSK) is adopted for pilot subcarriers and preamble symbols. A DL sub-frame is composed of one preamble symbol and 40 OFDM data symbols. The system design target is to support carry frequency offset (CFO) up to14 ppm and is optimized to enable the vehicle speed up to120 km/hr. The maximum Doppler frequency is about 0.025(normalized to a subcarrier spacing). The coherence time calculated by a typical way] is 1.5 ms which is about 14.8 times of an OFDM symbol time but is smaller than a frame time. Therefore, the channel can be treated asquasi-static within several symbol times but may vary a lot during one frame transmission.

III. BASEBAND RECEIVER

The proposed receiver includes a symbol boundary detector, an integer carrier frequency offset (ICFO) estimator, a fractional carrier frequency offset (FCFO) estimator, an FFT, a two stage channel estimator, an STBC decoder and a Demapper.

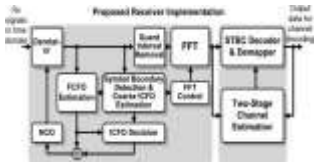


Fig. 2. Architecture of the proposed downlink baseband receiver.

Synchronization includes symbol timing, sample clock, and carrier frequency synchronization. The proposed synchronizer concentrates on the symbol boundary detection and the carrier frequency recovery loop as presented in the following sections.
Symbol Boundary Detection: An ISI free region of symbol timing detection is determined by the difference in length between the CP and the channel impulse response [12]. Since the proposed system has two transmit antennas, the signals transmitted from different antennas may arrive at the receiver with different delays due to multipath effect. Therefore, the decided boundary must locate in the common ISI free region to prevent the respective ISI effects from other symbols. IEEE 802.16estandard provides three types of preamble subcarrier sets.

The FFT size is not a multiple of 3, the time-domain preamble symbol is not exactly periodic. Using delay correlation method is difficult to precisely detect symbol boundary. Since the preamble symbol is a known sequence after system acquisition, a match filter corresponding to the time-domain preamble sequence transmitted from the antenna can be applied to match the received sample sequence and obtain the symbol boundary . The match filter complexity depends on the matching length, so a suitable length must take both performance and complexity into consideration. the mismatch of oscillator frequency in a receiver and a transmitter causes frequency offset effects in the received signals and destroys the characteristic of the matching results.

The filter coefficient sequence which is the known preamble sequence is compensated with the possible values of ICFO.

IV.TWO STAGE CHANNEL ESTIMATOR

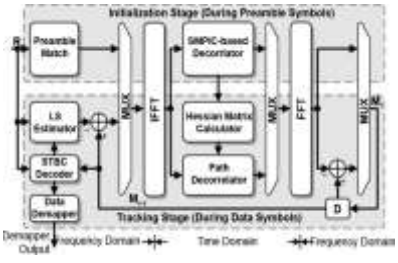


Fig. 3. Block diagram of two stage channel estimator.

The operation of the proposed channel estimator

contains the initialization stage and the tracking stage. The FFT/ IFFT module can be shared between these two stages.

Initialization Stage: The preamble match is used to estimate preliminary CFRs. The preamble subcarrier values are boosted as a constant power. To avoid the multiplier usage in matching calculation, the absolute value of the normalized pre-amble subcarrier can be expressed as a constant canonic signed digit (CSD) code. The preamble match design only re-quires adders and multiplexers controlled by the sign of the pre-amble patterns. Thus, only the sign bits of the preamble pat-terns are stored. The SMPIC -based decorrelator is used to identify the significant paths in a straightforward method. In this de-sign, N_L is 128 and is same as the CP length, and N_P is presumed to be eight. Based on the output SNR evaluation at the vehicle speed of 120 km/hr, the β value is decided to be four. The SMPIC -based decorrelator consists of a partial sorting net-work and a decorrelator.

Tracking Stage: By using dividers, the STBC decoder can be implemented intuitively. However, a divider is very costly. By operating with the two-stage dichotomy demapping method, the divisions can be avoided by scaling the constellation with the normalized term of the STBC decoding.

V. PROPOSED MATCH FILTER

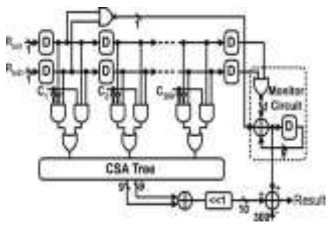


Fig. 4. Block diagram of proposed match filter.

Proposed Match Filter Features

- The proposed match filter applied with the ICFO-compensated coefficients can reduce the CFO effect and provide the precise symbol boundary detection, and the ICFO value can be detected simultaneously.

- The proposed ping-pong algorithm using the estimated FCFO value can refine the ICFO value and improve the accuracy.

- The proposed two-stage channel estimation can highly improve the performance in outdoor mobile channels as com-pared with the interpolation-based methods that are frequently adopted in the baseband implementation.

- In the initialization stage, the proposed SMPIC-based decorrelator uses a straightforward method to identify significant paths and cancel the multipath interference, which can highly reduce the implementation cost.

- In the tracking stage, the matrix inverse computation is efficiently avoided by employing the strongly diagonal property, which can highly save the computation complexity.

VI.LS ESTIMATOR

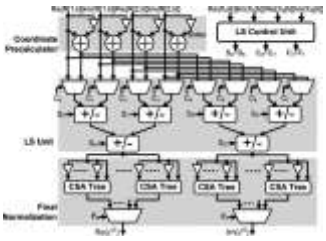


Fig. 5. Design of LS Estimator

In the path decorrelation, the complex multiplications of the order $O(N_L^3)$ for the Hessian matrix inverse $\mathbf{H}_N^{-1}$ are effectively saved by considering the strongly diagonal property. Nevertheless, for each entry calculation, we still require a lot of cycles to sum the cosine and sine values by using a lookup table.

VII.PATH DECORRELATOR

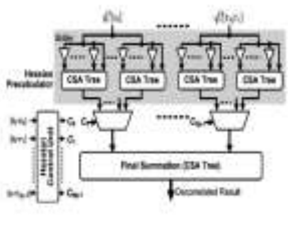


Fig. 6. Design of Path Decorrelator

The path decorrelator is composed of a Hessian precalculator, a Hessian control unit, multiplexers, and a final

summation. The Hessian precalculator is used to multiply [illegible] with the nonzero values of [illegible] and is only executed once during the path decorrelation.

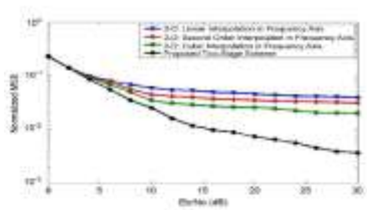
FLOW CHART OF THE PROPOSED RECEIVER

The flow chart of the proposed receiver is under the flowchart after phase compensation, the preamble symbol is first written to MB_ R2_0, but MB_R1_2 is no access. The following two OFDM symbols are then written to MB_R1 _0 and MB_R2_1 while the preamble symbol in MB_R2_0 are calculated by FFT processor and then ready at the time slot 0 for the channel estimation and STBC decoding access. Similarly, when the other two OFDM symbols are written to MB_R1_1 and MB_ R2_0, the two OFDM symbols in MB_R1_0 and MB_ R2_1 are ready at the time slot 1. Following the flow chart, the access scheme of MB_R1 _2 and MB_R2_0 at the time slot 6 is similar as that at the time slot 0, but the written data are two OFDM symbols in a time slot. The memory access schemes of these five memory banks are repeated every six time slots.

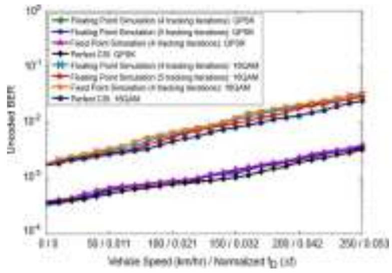
The performances of the proposed baseband receiver are demonstrated through fixed point simulations of the proposed system with two transmit antennas and one receive antenna. The carrier central frequency is set to 2.5 GHz with CFO to be + 14 ppm. The multipath fading channel uses the International Telecommunication Union (ITU) Veh-A channel model with relative path power profiles of 0, 1, 9, 10, 15, and 20(dB), and the path excess delays are uniformly distributed from 0 to 50 sample periods.

These methods perform linear interpolation among contiguous time slot in time axis and linear, second order, and cubic interpolations in frequency axis. Mean square errors (MSEs) of channel estimation which is normalized to channel power for 16QAM modulation at the vehicle speed of 120 km/hr.

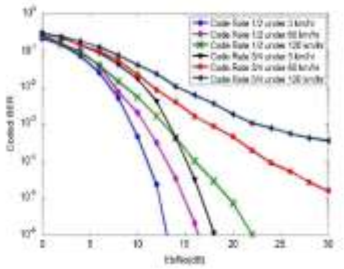
The proposed two-stage channel estimation method has much lower MSE than the 2-D interpolation methods. Moreover, the curves of the 2-D interpolation methods present an error floor phenomenon. The 2- D interpolation methods with limited pilot information cannot recover the channel variations well in outdoor fast and selective fading channels.



MSE Channel Estimation



BER Performance



Coded BER Performance

The coded BER performance of the proposed receiver combining with the convolution code for 16QAM modulation. IEEE 802.16e specification does not provide the performance requirement in mobile transmission. However, in code rate 1/2, the proposed receiver at ν of 3, 60, and 120 km/hr can achieve the coded BER less than of 10^-6 with E_b/N_o of 13.1, 16.1, and 22.1 dB.

In code rate 3/4, the proposed receiver under 3 km/hr can achieve the coded BER less than [illegible] with E_b/N_o of 18.2 dB. Even at ν of 60 and 120 km/hr, the proposed receiver in code rate 3/4 can achieve the coded BER to about [illegible] and [illegible]. However, IEEE 802.16e standard provides the advanced channel coding schemes such as block turbo code (BTC), convolution turbo code (CTC) and low density parity check code (LDPC) as the optional modes, and these schemes may further improve the coded BER performance.

The proposed receiver is implemented in 90-nm 1P9M 1 V CMOS technology. The post- layout result of the proposed receiver is summarized in Table IV, and the chip layout is shown. The gate count is about 1386.5 K gates. There are two clocks, 11.2 and 78.4 MHz, to be used as the sampling frequency and the operating frequency, respectively.

VIII.ERROR DETECTION AND ERROR CORRECTION

ERRORS

1. Random Error

2. Burst Error and
3. Orthogonal Error

Orthogonal error pattern is detected and corrected by orthogonal error detector.

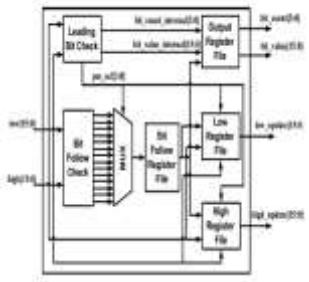


Fig. 7. Orthogonal Error Detector

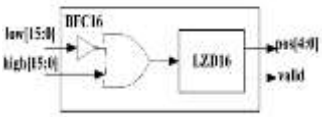


Fig. 10. Bit Follow Check (Exor gate)

The BFC denotes the bit follow check of two vectors, which can be implemented by a simple logic gate and an LZD circuit.

VIII (a).MODULES

1. Leading bit check module
2. Bit follow check module
3. Bit follow register module

VIII (b). LEADING BIT CHECK MODULE

In CBD, the leading bit check (LBC) detects the common bits between low and high registers which consists of a 16-XOR gate and a leading zero detector for 16 bits (LZD16) circuit used to detect the similarity between 2-16 bits.

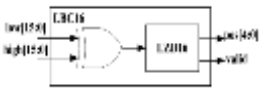


Fig. 8. Leading Bit Check Module

VIII (c). BIT FOLLOW CHECK

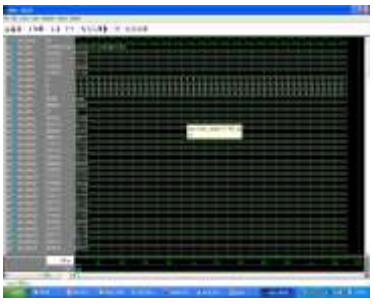


Fig. 9. Bit Follow Check

VIII (d). BIT FOLOW REGISTER FILE

The corresponding bit follow value is then registered in the Bit Follow Register File, which is used for the output.

The output of the orthogonal error detector at the final stage has low update and high update which are of 16bits each. Among these 16 bits, eight bits are of address and the remaining eight bits are data.

These are the data bits obtained at the STBC – OFDM decoder without error. It is error free from random errors, burst errors and orthogonal errors.

IX.SIMULATION AND RESULTS

X.CONCLUSION

Due to the system work in this project, number of slices will be reduced, number of look up tables will be reduced and Power Consumption is also to be reduced when compared with the normal transmission system.

PERFORMANCE EVALUATION ANALYSIS

Slices – 29

LUT's – 56

Gate Counts – 486k gates

Power Consumption – 52mW

Latency – 19.519ns

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