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Design of high performance SRAM cell using 12T MTCMOS Technology

M. Gangasukanya, P. Asiya Thapaswin
M.Tech-ECE(VLSI)
Vaagdevi institute of Technology & sciences JNTUA
Proddatur, India
Assistant professor in ECE
Vaagdevi institute of Technology & sciences JNTUA
Proddatur, India
www.mallelachenna@gmail.com

Abstract: this paper focus on the stability analysis at different pull up ratios and power dissipation at different tempetures of a novel low power 12T MT CMOS SRAM cell. The MT CMOS Technology the SRAM cell will be contains low V_T (LVT) transistors and two high V_T (HVT) sleep transistors. for reducing the wake up power During transition from sleep mode to active mode based on using sleep transistors and LVT transmission gate. The sleep power During transition from sleep mode to active mode for writing operations of SRAM cell. This will reduce the static energy dissipation of the cell. to reduce the swing voltage at the output nodes of the bit bar line and bit line based on the two Additional voltage sources are used, one connected with the bit bar line and another one connected with the bit line. the reduction in swing voltage causes the reduction in dynamic power dissipation, low leakage currents in MT CMOS technology and the simulation results of proposed 12T SRAM cell have been determined and compared to those of some other existing models of SRAM cell and the simulation have been done in 45nm CMOS Technology based on tanner tool.

Keywords: Charge recycling, Dynamic power, SRAM, static power, voltage swing.

I.INTRODUCTION

The SRAM cell design having low power and high stability. SRAM design as the demand of the portable electronic market constantly urgs for less power- hungry architectures [1]. Here the some technique are introduced such as scaling the supply voltage using MTCMOS process. The SRAM is to ensure the reasonable noise margin which is normally measured by the static noise margin. According to [2] this design degrade when the threshold voltage variation increases and are also linearly depend on the reduction of the supply voltage. So result is difficult to maintain the cell stability and technology enters less than 100nm regime.

The 6T SRAM cell design [3-4] given to improve the stability and power dissipation. In this Design having separate read and write operations. To minimizing the static power dissipation and dynamic power dissipation in SRAM cell during write/read operation. sense-amplifying cell[5], kim et al. [6] have been proposed low design technology. Here the another common method is used to improve the write operation which is boosted word line technique [7]. MTCMOS technology provides low leakage and high performance operation by utilizing high speed, low threshold voltage transistor during active mode and low leakage, high threshold voltage transistor during sleep mode in this technology also called as power gating.

During mode transitions a charge recycling technique is used to minimize the leakage current and static power dissipation. During switching activities two voltage sources are used at the output nodes to reduce the swing voltage resulting in reduction of dynamic power dissipation.

Section II describes some existing SRAM cells, section III describes a proposed method of 12T MTCMOS technology design and working principle, section IV describes existing and proposed methods of schematic diagrams and wave forms, V results of power dissipation at different temperatures, static noise margin analysis and power consumption values, VI describes finally concluded the paper.

II. EXISTING SRAM CELLS

(A). Conventional 6TSRAM cell:

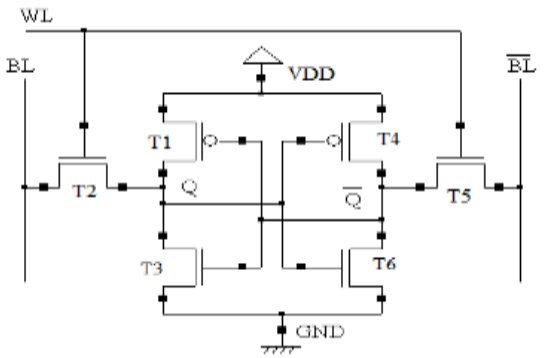

fig1: Conventional 6T SRAM cell.

Here the two cross coupled inverters are using. Here the will be stored in pull up section. To enabling the transistors T2 and T5 for write operation so word line is asserted to high

state. To store the data we are using two bit lines that is one bit bar line another one is bit line. For write operations one bit line is asserted high and another bit line is asserted low. For writing '0' the bit line (BL) is low and bit bar line (BLBAR) is high. When the word line is asserted high then two transistors T2 and T5 are ON stage. the charge stored in the BL goes through T2, T3 and path to ground due to low value of bit line the T4 is ON state so the charge will be stored at q bar. Here the bit line bar is high due to that T3 is ON so the charge will be discharge to ground. Similarly in the write '1' operation BL is '1' and BL BAR is '0'. Due to bit line (BL), then T6 is ON so any charge stored at q bar will be discharge from T5, T6 and path to ground. When the bit line bar (BLBAR), goes low then T1 is ON so the charge will be stored at q. Here the differential voltage will be developed between the bit line and bit bar lines. For read operation both bit lines will be asserted high. In the 6T SRAM cell not having successful read operation so we are going to use 8TSRAM cell.

(B). 8T SRAM Cell:

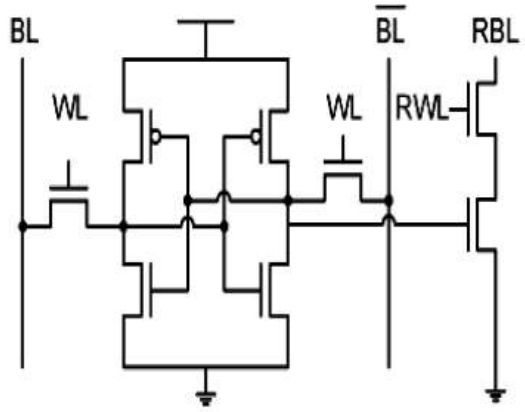

fig2: 8T SRAM cell

The 8T SRAM cell [14] is as shown in fig2. the writing operation is same as the 6T SRAM cell design and for the read operations it uses the separate bit line, RBL with RWL as its control signals. the RBL is read according to the value stored at the storage node when RWL is high. To restabilizing the read operation we are using 9T SRAM cell.

(C). 9T SRAM cell:

The 9T SRAM is as shown in figure 3, here the write operation is same as the 6T SRAM cell design. The read operation done separately through N5, N6, N7 these are controlled by the read signal 'RD' will be high. This design has the problem of the high bit line capacitances with more pass transistors on the bit line and bit bar line.

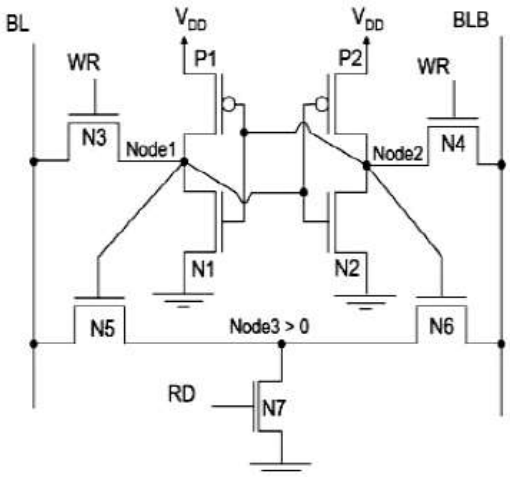

Fig3: 9T SRAM cell.

(D). 11T SRAM cell:

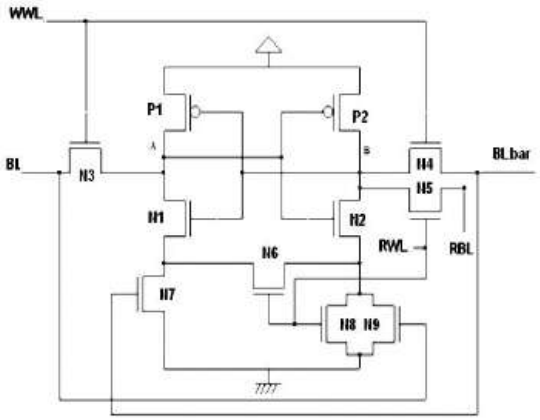

Fig4: 11T SRAM cell.

To writing faster here the cell disconnects the node to which a logical high is to be written from the ground. In case of it uses a separate read bit line and N5, N2, N8, N9 are ON state. Here the N9 and N8 are give the low effective resistance to the read operation and hence faster read.

III. PROPOSED 12T MT CMOS SRAM CELL:

To achieve low power we are using 12T MTCMOS SRAM architecture. Here the two voltage sources are using which is V1 and V2. The two voltage sources V1 and V2 are connected the output of bit line and bit bar line. the two NMOS transistors VT1 and VT2 are used one connected at the bit line and the bit bar lines to directly switch ON and switch OFF the voltage sources during write operations. Here the two cross coupled inverters are having low voltage transistors and the two sleep transistors of S1 and S2 are the high voltage transistors while in sleep condition. The low voltage transistor and high voltage transistor are the type of MT CMOS Technology. Here the S1 of NMOS sleep transistor connects from node 'M' to 'ground' where as the S2 of PMOS sleep transistor connects from 'Vdd' to

node ‘N’. If when the sleep transistors are in sleep condition then disconnect the logic cells from the supply node or ground node and to reduce the leakage current. For providing the charge sharing from one node to another node we are connecting the LVT transmission gate TG between the two nodes of virtual ground node’ M’ and virtual supply node ‘N’. Here the transmission gate TG and the sleep transistors S1 and S2 are having larger size than compared to the two cross coupled invertors of transistors T1, T3, T4, T6 to maintain some trade-off between increased static and dynamic power dissipation. Here the sleep transistor ‘ST’ and charge sharing control signal ‘CS’ provide the switching activity control on sleep transistors and TG.

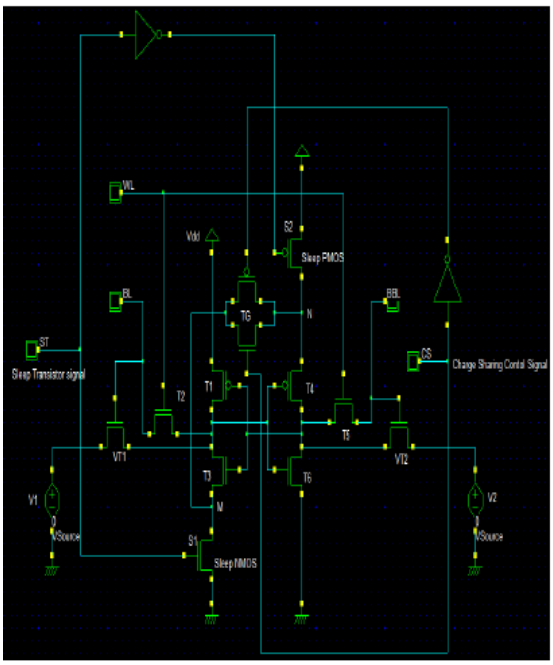

Fig5: 12T SRAM cell.

(A).OPERATIN OF SLEEP TRANSISTOR

In the active region the two sleep transistors S1 and S2 are in the linear region and virtual ground node ‘M’ and virtual supply node ‘N’ are equal to ‘0’ and ‘vdd’. During in the write ‘1’ operation the both sleep transistors S1 and S2 are OFF. So two transistors will chosen to high threshold device, due to that a very little sub threshold leakage current is flow through the circuit design so the virtual ground and virtual supply nodes are floating. During in the sleep time period if when sleep period long then virtual ground node ‘M’ charged to some voltage value of’ Vdd’ not closely’ Vdd’. Due to that the leakage current flow through the transistor T3 (with T1 ON). Similarly the virtual supply node ‘N’ discharged to some voltage value of ‘0’ not closely ‘0’. Due to that the leakage current flow through T4 (with T6 ON). Here the total capacitances of the virtual ground ‘M’ and virtual supply ‘N’ are denoted as C_M and C_N respectively. So the C_M is charged from 0 to very closely ‘Vdd’. Similarly C_N is discharged from ‘Vdd’ to very closely ‘0’. In the write ‘0’ operation the two sleep transistors to turn them ON. Due to that the virtual ground node ‘M’ fall towards ‘0.’Similarly the virtual supply node ‘N’ rise towards ‘Vdd’. Thus C_M is discharged from ‘Vdd’ to ‘0’ and C_N is charged from ‘0’ to ‘Vdd’.

The virtual ground and virtual supply nodes of charging and discharging will be having static energy dissipation. This will be equal to ($C_M V_{dd}^2 + C_N V_{dd}^2$). These is an write ‘1’ and write ‘0’ operation’s of one complete cycle.

(B).CHARGE RECYCLING THROUGH

TRANSIMISSION GATE

In the section ’A’ explaining without connecting the transmission gate, here to reduce the static energy dissipation so we connect the transmission gate between the virtual ground node ‘M’ and virtual supply node ‘N’.

During write ‘1’ operation, before active to sleep transition of the sleep transistors the TG is turned ON. So the capacitance of virtual ground C_M rise from’ 0’ to ‘A.vdd’ (A<1), not closely ‘Vdd’. similarly the voltage of N node will fall from ‘Vdd’ to ‘A.vdd’ and the capacitance of virtual supply node ‘C_N’ fall from ‘Vdd’ to ‘A.Vdd’ not closely ‘0’ then sleep signal ST is applied due to that the sleep transistors to turn them off. And due to that the capacitance of ‘C_M’ rise from ‘A.Vdd’ to closely’ Vdd’ and similarly the capacitance of ‘C_N’ fall from ‘A.vdd’ to closely ‘0’. For write ‘1’ operation the ofter charge sharing if calculated. So equating the total charge of both capacitance in before and right after charge recycling is

C_N. Vdd = (C_M + C_N) V_{write1}

Therefore V_{write1} = C_N. Vdd/ (C_M + C_N)

V_{write1} = A. Vdd

Where A = C_N/ (C_M + C_N)

Between the two nodes end of the charge sharing is A Vdd.

If neglecting the energy consumption the TG and sleep transistors. The energy supply of charging capacitance

C_M = C_M. Vdd (Vdd – A. Vdd)

C_M = (1-A). C_M. Vdd^2

For write ‘1’ operation the reduction of static energy dissipation is ‘ A. C_M. Vdd^2’

In the sleep mode period ‘S1’ of NMOS sleep transistor reduce the leakage current through from ‘S1’ to ground and ‘S2’ of PMOS sleep transistor reduce the leakage current through T4 and Vdd to ground. Obviously the output of Q is stored ‘1’ and the output of Q bar is stored ‘0’.

During write ‘0’ operation before sleep to active transition of the sleep transistors, the TG is turn ‘ON’. So the capacitance of virtual ground node C_M fall from ‘Vdd’ to ‘B.vdd’ (B<1), not closely ‘0’ and the capacitance of virtual supply node C_N rise from ‘0’ to ‘B. Vdd’ not closely Vdd. Then sleep signal ST is applied. Due to that capacitance of virtual ground node ‘C_M’ fall from ‘B.Vdd’ to closely ‘0’ and similarly the capacitance of ‘C_N’ rise from ‘B. Vdd’ to closely’ Vdd’.

For write ‘0’ operation the charge sharing if calculated so equating the total charge of both capacitance in before and right after charge recycling is

C_M. Vdd = (C_M + C_N). Vwrite0

Therefore V_{write0} = C_M. V dd / (C_M + C_N)

V_{write0} = B. Vdd, where B = C_M/(C_M + C_N)

Between the two nodes end of the charge sharing if ‘B.Vdd’. If neglecting the energy consumption the TG and sleep transistors the energy supply of charging capacitance is

C_N = C_N. Vdd (Vdd – B. Vdd)

C_N = (1-B). C_N.Vdd^2

For write ‘0’ operation the reduction of the static energy dissipation is ‘ B.C_N.$Vdd^{2'}$

During write ‘1’ and write ‘0’ the total reduction of static energy dissipation for one complete cycle is A. C_M.Vdd^2 + B.C_N.Vdd^2

Due to charge recycling the energy saving ratio is

ESR=(A.C_M.Vdd2+BC_N.Vdd2)/(C_M.Vdd2+C_N.Vdd2) (1)

Substituting the A and B equations in equation ‘1’ and X=C_M/C_N, so ESR(X) can be rewritten as

ESR(X) = 2X/ $(1+X)^2$ (2)

The ESR(X) of optimum value for ‘X’ is obtained by equating the derivative of the ratio results in X=1 or C_M=C_N.

In order to obtain best energy saving one needs to have equal capacitance between the node M and node N. Then maximum energy saving can be obtained by keeping X=1 in equation (2). Then ESR=0.5. This means that maximum energy saving is 50% is achieved by using the charge recycling technique. So the power needed to turn ON or OFF the TG the total saving ratio is actually less than 50% threshold voltage and size of TG.

((C).SWING VOLTAGE

During the mode transition from ‘0’ to’1’ or ‘1’ to ‘0’ at the bit line or bit bar line swing voltage is required. Due to that dynamic power dissipation is increases. During the write operation the switching activity is improved. In the proposed design of 12T MTCMOS of SRAM model then voltage sources V1 and V2 are reduced. The voltage sources V1 and V2 are reduced. The voltage swing the dynamic power can be expressed as

P dynamic = α C. Vdd V swing f (3)

Where C = load capacitance, α= activity factor,

f = clock frequency. V swing = voltage

Swing at output node, Vdd is the power supply voltage if when the frequency increases and the switching activity also increases. Due to that dynamic power dissipation is also increases [6].the voltage source reduces the voltage swing at the output. The dynamic power dissipation constant at higher frequency. Due to better switching capability the stability is also improved in proposed method. Compared to other SRAM methods.

In the write ‘0’ operation, BL is low and BL bar is high. Due to that the transistor VT1 is OFF and the transistor VT2 is ON. So then voltage sources V2 decreases the swing at the output of the BL bar line.

In the write ‘1’ operation BL is high and BL bar is low. Due to that the transistor VT1 is ON and another transistor VT2 is OFF. So then voltage sources V1 decreases the swing at the output of the BL line.

IV. EXISTING AND PRAPOSED METHODS OF SCHEMATIC DIAGRAMS AND WAVE FORMS

(A).6T SRAM cell

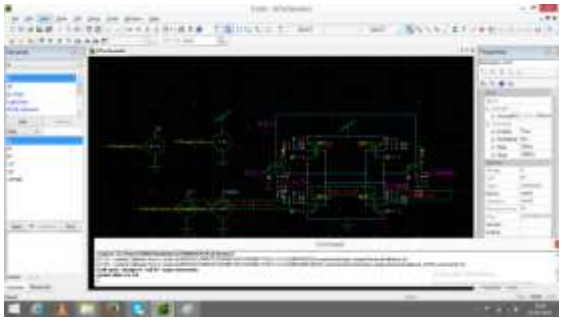

Fig6: schematic diagram of 6T SRAM cell.

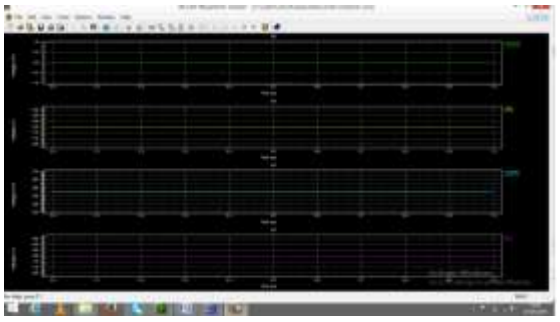

Fig7: write’0’ wave forms of 6T SRAM cell

The above fig of 6T SRAM cell the write ‘0’ simulation of bit line is low and bit bar line is high, in the write ‘1’ operation bit line is high and bit bar line is low.

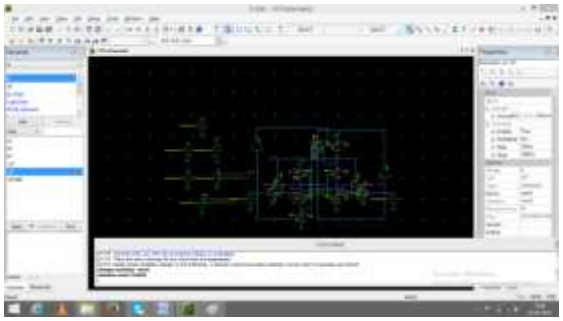

Fig8:12T SRAM cell

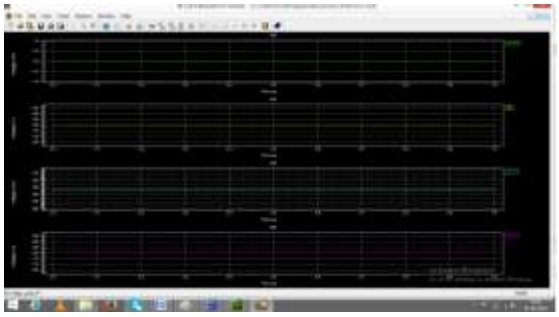

Fig10:write'0' operation of 12T SRAM cell

The above fig of 12T SRAM cell the write '0' simulation of bit line is low and bit bar line is high, in the write '1' operation bit line is high and bit bar line is low.

V.RESULTS OF POWER DISSIPATION AT DIFFERENT TEMPERATURES, STATIC NOISE MARGN ANALYSIS AND POWER CONSUMPTION VALUAS

TABLE I. COMPARISON OF POWER DISSIPATIONS AT DIFFERENT TEMPERATURES

Temperature (^{0}C)	Total Power Dissipation (pW)				
	6T SRAM [3]	8T SRAM Cell [14]	9T SRAM Cell [15]	11T SRAM Cell [16]	Proposed 12T SRAM Cell
5	3.596e-9	2.59e-9	2.59e-9	9.80e-8	4.79e-11
10	4.087e-9	2.98e-9	2.98e-9	1.05e-7	5.58e-11
15	4.623e-9	3.43e-9	3.43e-9	1.14e-7	6.58e-11
20	5.082e-9	3.92e-9	3.92e-9	1.22e-7	7.81e-11
30	6.531 e-9	5.073e-9	5.073e-9	1.13e-7	1.12e-11
40	8.069e-9	6.47e-9	6.47e-9	1.57e-7	1.58e-11

TABLE II. COMPARISON OF SNMS AT DIFFERENT PULL-UP RATIOS

Pull-up Ratio	Static Noise Margin (mV)				
	6T SRAM [3]	8T SRAM Cell [14]	9T SRAM Cell [15]	11T SRAM Cell [16]	Proposed 12T SRAM Cell
1.05	91.9	242.3	237.23	231	234.23
1.2	93	243.6	238.04	232	235.67
1.4	93.6	259.1	244.34	234	251.89
1.6	94	253.4	249.15	236	254.11
1.8	94.5	258	253.88	239	259.26
2.0	95	262.5	257.26	240	263.47
2.1	96.7	284	259.55	241	255.29
2.2	96.8	279.8	263.57	243	259.45
2.4	98.2	276.3	270.89	247	264.12
2.6	99.4	280	285.39	259	268.59
2.8	101.3	285.4	289.86	250	274.17

Table '2' shows static noise margin results at different pull up ratios in 'mv'

TABLE III. COMPARISIONS OF POWER COSUMPTION VALUAS

S.NO	CELL DESIGN TYPE	AVERAGE POWER CONSUMED
1	6T SRAM	5.8e-9
2	8TSRAM	4.469e-9
3	9T SRAM	4.469e-9
4	11T SRAM	1.31e-7
5	12 SRAM	9.31e-11

VI. CONCLUSION

The proposed design of 12T MT CMOS of SRAM cell consumed low power and provide high speed performances. In the proposed design provide low power solution in high speed devices like laptops, mobile phones programmable logic devices etc. The simulation results are less power consumption and dissipation is also less.

EXTENSION

BODY BIAS TECHNIQUE: body bias technique means which add a additional voltage to the PMOS or NMOS of substrate. This improves the threshold voltage of the transistor due to that leakage can be minimised.

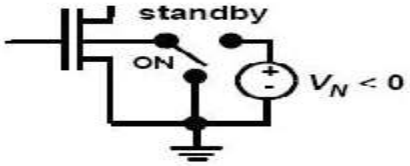

Fig 10: Body Bias techniques

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