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An Efficient Design and Implementation of ALU using Gated Diffusion Index

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***Abstract*-- This paper implements a design of a 4-bit Arithmetic Logic Unit (ALU) using the concept of gated diffusion index (GDI) technique. In central processing unit and microprocessors ALU is the most crucial component. 4x1 multiplexer, 2x1 multiplexer and full adder are used in ALU design to implement the arithmetic operations such as ADD,SUBSTRACT etc. and logical operations such as AND,OR. In multiplexers and full adders GDI cells are used. The simulation is carried out Tanner EDA 13.0 simulator using TSMC BSIM 250nm technologies and compared with previous designs realized with Pass transistor logic and CMOS logic. CMOS uses both PMOS and NMOS transistors. CMOS design gives high power dissipation, and delay is also high. The occupation of area is also high. The simulation shows that the design is more efficient with less power consumption, less surface area and is faster as compared to pass transistor and CMOS techniques.**

***Keywords* -- GDI technique, ALU, CMOS technique.**

I. INTRODUCTION

In the era of growing technology and scaling of devices up to nanometer regime, the Arithmetic and Logic circuits are to be designed with less power, compact size and propagation delay. For any high speed low power applications such as digital signal processing, microprocessors, image processing arithmetic operations are the basic functions. Addition is most important part of the arithmetic unit rather approximately all other arithmetic operation includes addition. In the design of any Arithmetic Logic Unit the primary issue is low power high performance adder cell. To design full adder cell efficiently there are various topologies and Methodologies proposed. This project implements the concept of GDI technique in the design of ALU and its sub blocks as Multiplexers and Full adders.

The rest of paper is organized as follows Section II describes previous works. Section III consists of the description of Gate Diffusion Input Technique. In section IV Arithmetic Logic Unit design, its operation and schematic is explained. Section V describes simulation result and analysis. At last conclusion is made in section VI.

II. PREVIOUS WORKS

There are different types and designs of full adder which is discussed in various papers at state of the art level

and process and circuit level. Twelve state of the art full adder cells are: conventional CMOS, CPL, TFA, TG CMOS, C2MOS, Hybrid, Bridge, FA24T, N-Cell, DPL and Mod2f. R. Shalem, E. John, and L.K. John, proposed a conventional CMOS full adder consisting of 28 transistors [1]. Later, the number of transistor count is reduced to have less area and power consumption. A. Sharma, R Singh and R. Mehra, Member, IEEE, have improved performance with Transmission Gate Full adder using CMOS nano technology where 24 transistors are used [2]. The Complementary Passtransistor Logic (CPL) full Adder contains the 18 transistors. The power consumption of this structure is 2.5µw [3]. A Transmission Function Full Adder (TFA) based on the transmission function theory has 16 transistors. The power consumption of this structure is 12µw. N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. The power consumption of this structure is 1.62µw. Mod2f Full Adder contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. The power consumption of this structure is 2.23µw [3]. Saradindu Panda, N. Mohan Kumar, C.K. Sarkar, optimized the full adder circuit to 18 Transistor using Dual Threshold Node Design with Submicron Channel Length [4]. T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy, designed 14 transistor high speed CMOS full adder and significantly improved threshold problem to 50% [5].

For reducing power dissipation, propagation delay and area Gated Diffusion Input Technique is a new method . T. Esther Rani, M. Asha Rani, Dr. Rameshwar Rao, designed an area optimized low power arithmetic and logic unit in which Arithmetic Logic Unit is implemented using logic gates, pass transistor logic, as well as GDI technique [6]. Manish Kumar,

Md. Anwar Hussain, and L.L.K. Singh explained a Low Power High Speed ALU in 45nm Using GDI Technique and Its Performance Comparison [7].

We have designed ALU in different way by using GDI cells to implement multiplexers and full adder circuit. The input and output sections consist of 4x1multiplexers and 2x1 multiplexers and ALU is implemented by using full adder

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III. GATED DIFUSSION INPUT (GDI) TECHNIQUE

Morgenshtein has proposed basic GDI cell shown in Fig.1 [8]. For designing of low power digital combinational circuit GDI technique is the new approach.GDI technique is basically two transistor implementation of complex logic functions which provides in-cell swing restoration under certain operating condition. GDI technique approach leads to reduction in propagation delay, area and power consumption of digital circuits is obtained while having low complexity of logic design. In GDI technique the important feature is that the source of the PMOS is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI design more flexible than CMOS design.

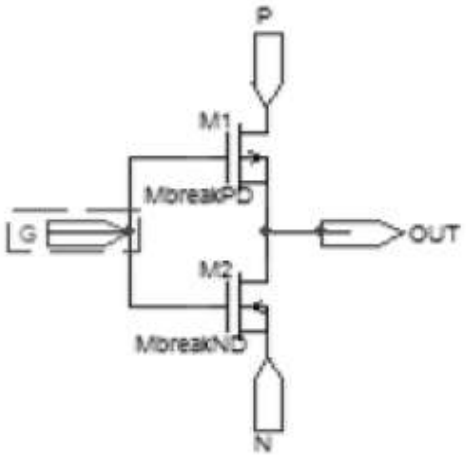

Fig. 1. Basic GDI Cell

There are three inputs in a GDI cell - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N and P respectively. Table 1 shows different logic functions implemented by GDI logic [8] based on different input values. So, various logic functions can be implemented using GDI technique with less power and high speed as compared to conventional CMOS design.

TABLE1: GDI Cell Logic Functions

S.NO	N	P	G	Out
1	0	B	A	A’B
2	B	1	A	A’+B
3	1	B	A	A+B
4	B	0	A	AB
5	C	B	A	A’B+AC
6	0	1	A	A’

A. Multiplexer

Multiplexer is a digital switch. The multiplexer has number of input data lines and only one output line. By using a set of selection line the particular input is selected at the output. There are ‘2n’ input lines and ‘n’ selection lines whose bit combinations determine which input is selected. Fig 2 shows implementation of 2x1 multiplexer using GDI cell. The 4x1 multiplexer has four inputs, two selection lines and only one output. Depending on the two selection lines, one output is selected at a time among the four input lines. Fig. 3 shows implementation of 4x1 multiplexer using GDI cell.

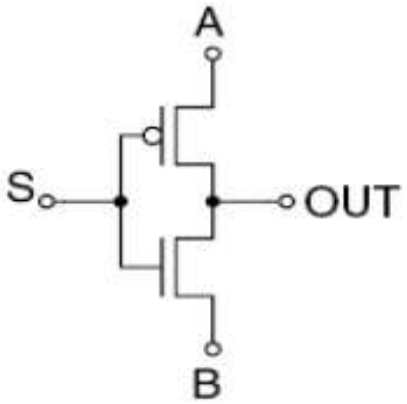

Fig.2.GDI based 2x1 Multiplexer

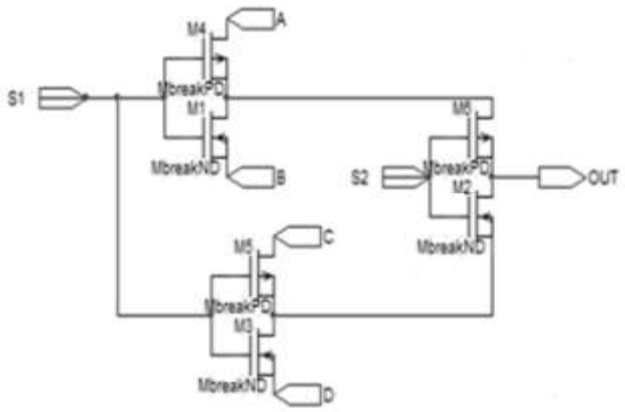

Fig 3. GDI based 4x1 Multiplexer

B. XOR Gate

The main building block of full adder circuit is the XOR gate .The XOR gate gives sum output. By optimizing XOR gate the overall performance of full adder circuit can be improved. Fig.4 shows the implementation of XOR gate using GDI technique [9]. It uses less number of transistors as compared to conventional design of XOR gate using CMOS logic Units.

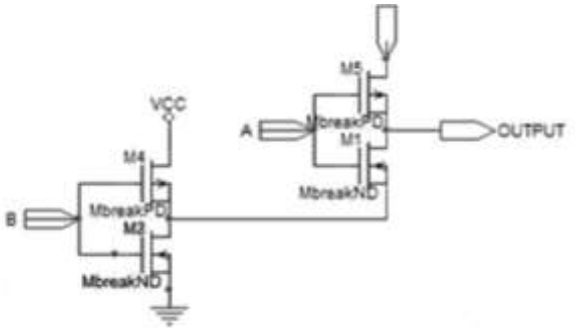

Fig. 4. GDI based XOR Gate

C. Full Adder

The Full Adder circuit adds three one-bit binary numbers (A, B & C) and outputs two one-bit binary numbers, a sum (S) and a carry (C_{out}). The full adder is usually a component in cascade of adders, which add 4, 8, 16 etc. binary numbers. The basic building block of Arithmetic and Logic Unit is implementation of Full Adder cell using GDI technique has been shown in Fig 5.

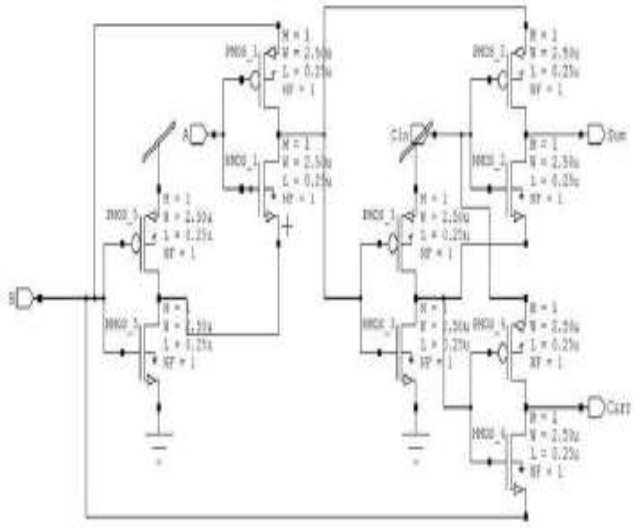

Fig.5.GDI based full adder cell

IV. DESIGN OF ARITHMETIC AND LOGIC UNIT (ALU)

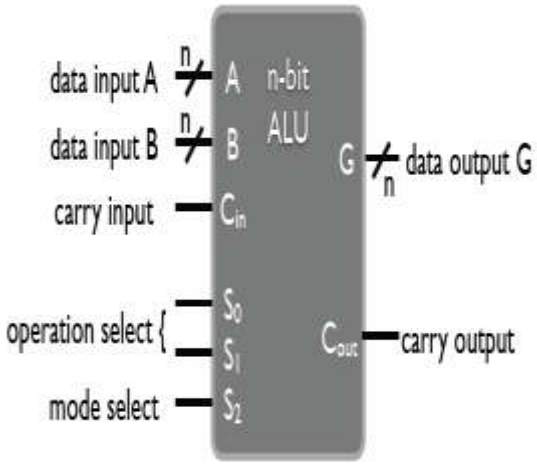

Fig: 6 Block diagram of Arithmetic and Logic Unit

In Central Processing Unit (CPU) of a computer, Arithmetic and Logic Unit (ALU) is a fundamental building block and even the simplest microprocessors contain ALU. It is responsible for performing arithmetic as well as logical operations such as addition, subtraction, increment ,decrement, logical AND, logical OR, logical XOR and logical XNOR.

Eight 4x1 multiplexers, eight 2x1 multiplexers and four full adders are present in 4bit ALU. The 4-bit ALU is designed in 250nm, n-well CMOS technology. An INCREMENT and DECREMENT operations takes place when logic '1'and logic '0' are applied as an input. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is seen as a subtraction operation [6]. For SUBTRACTION operation two's complement method is used in which complement of B is used. The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR.

Fig. 7 shows the 4-bit ALU where first stage to fourth stage is cascaded with the CARRY bit. Symbolic representation of 4-bit ALU as shown in fig. 8.

Based on the condition of the select signals, the multiplexer selects the appropriate input and gives it to the full adder which then computes the results. At the output of the multiplexer stage selects the appropriate output and route it to output port. Table 2 shows the truth table for the operations performed by the ALU based on the status of the select signal .The operation being performed and the inputs and outputs being selected are determined by set of three select signals incorporated in the design. Fig9. shows multiplexer logic at input port and Fig 10.shows multiplexer logic at output port.

TABLE II. OPERATIONS OF ALU

Selection Lines			Operations
S2	S1	S0	
0	0	0	AND
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBSTRACTION
1	1	0	INCREMENT
1	1	1	DECREMENT

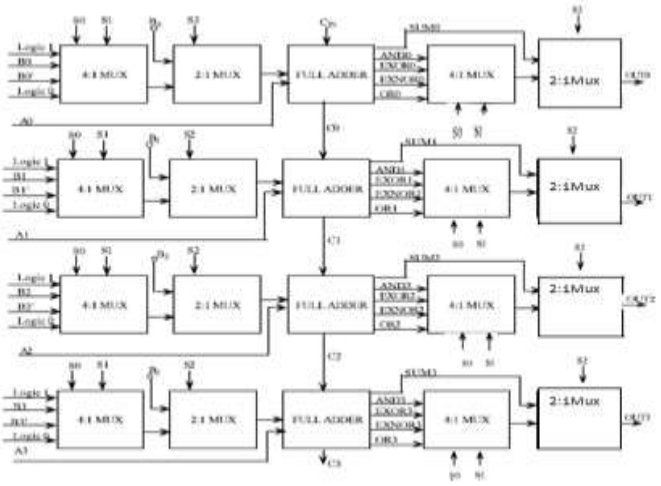

Fig.7. 4-bit Arithmetic and Logic Unit

By using schematic editor of Tanner EDA the schematic of 4 bit ALU is designed. It shows connectivity between the components and describes aspect ratios of the transistor that can be modified along with the design. Figure 10 represents the complete schematic view of ALU. The 4-bit ALU consists of two 4-bit inputs, three selecting lines, and one carry input, one carry output and four output bits.

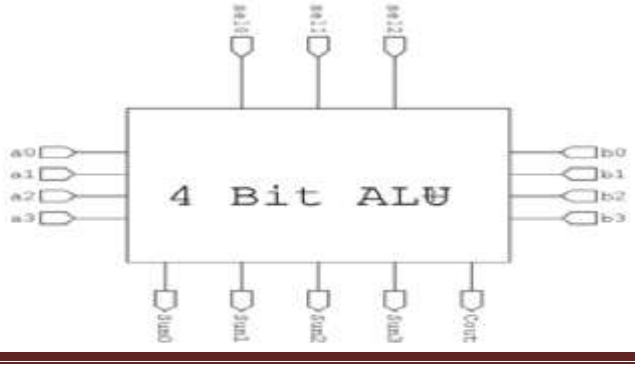

Fig.8.Symbol for 4-bit ALU

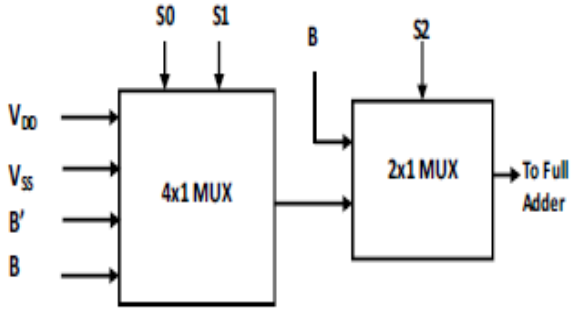

Fig.9.Multiplexer block diagram at the input stage

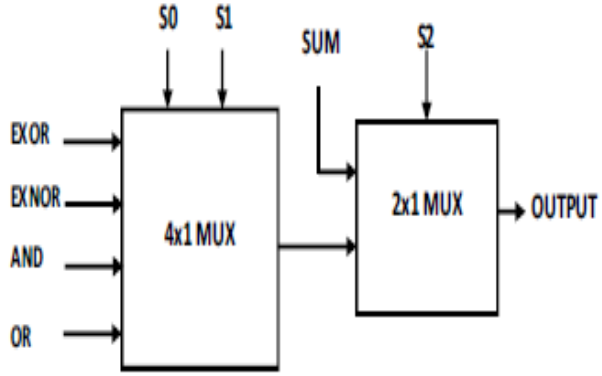

Fig .10. Multiplexer block diagram at the output stage

V. SIMULATON RESULTS AND ANALYSIS

This section describes performance of the proposed design using Tanner EDA tool on 250nm technology. The simulated output of 2x1 multiplexer, 4x1 multiplexer and full adder is shown in Figure 11, Figure 12 and Figure 13.The number of transistor required and power consumption for the individual cells of the ALU is listed in table III and the total power consumption and number of transistor of the ALU designed in different ways is listed in table IV.

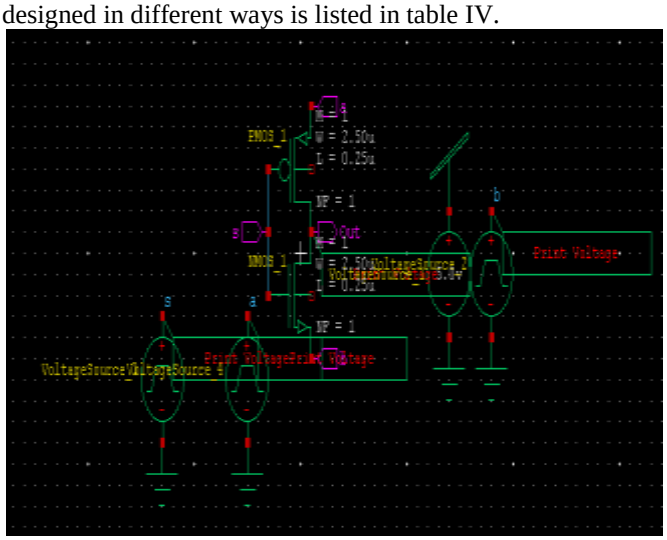

Fig :11: Schematic of 2x1 Multiplexer

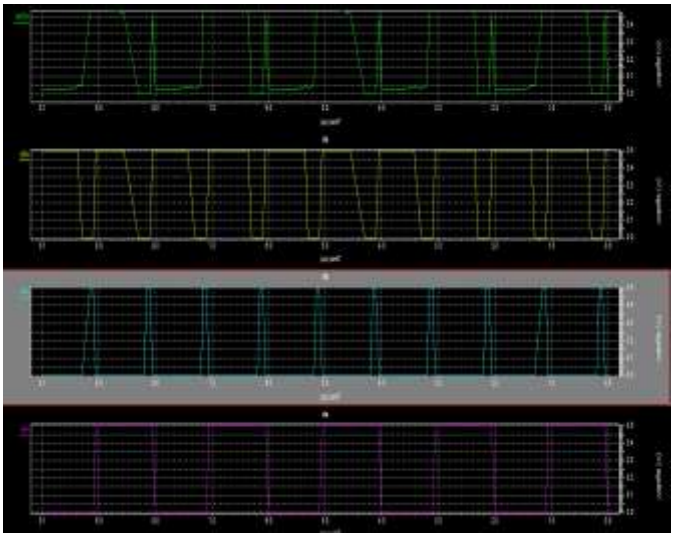

Fig : 12: Simulated output of 2x1 Multiplexer

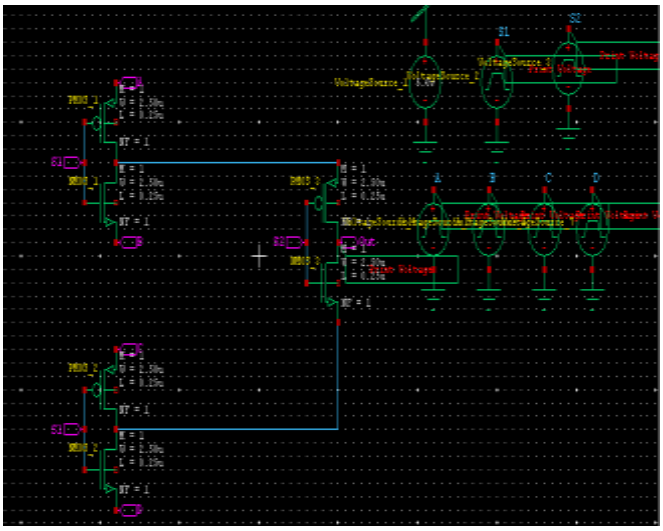

Fig 13 Schematic of 4x1 Multiplexer

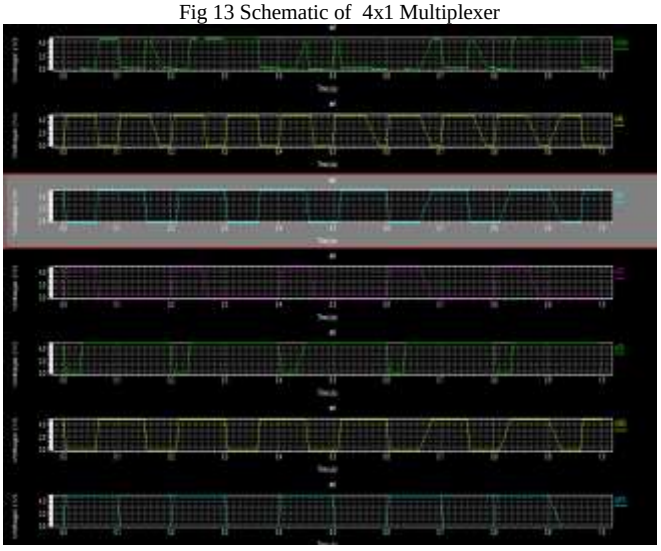

Fig. 14.Simulated output of 4x1 Multiplexer

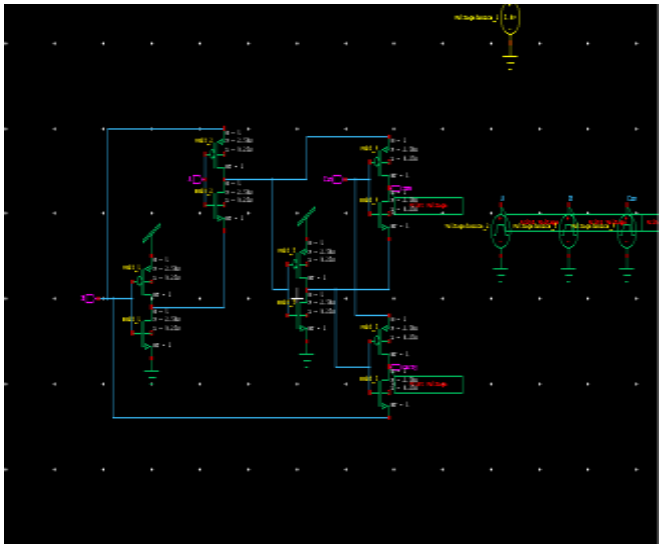

Fig .15. Schematic of 2x1 Full Adder

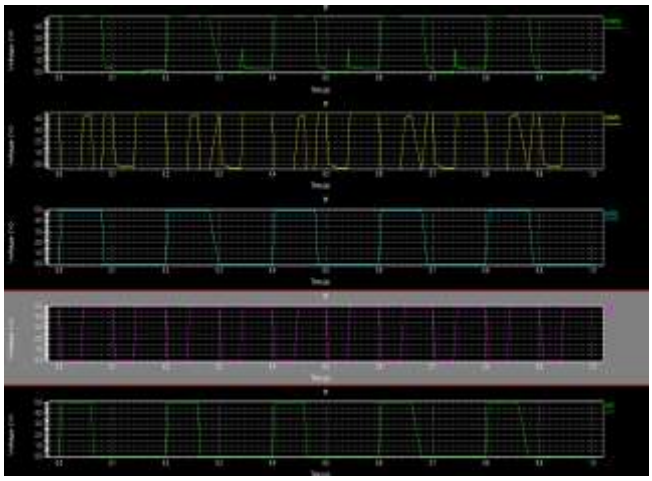

Fig.16. Simulated output of Full Adder

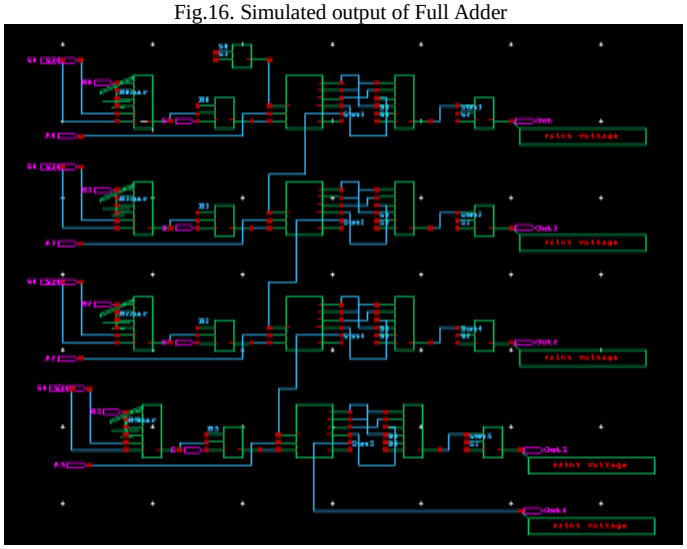

Fig 17 Schematic of 4 bit Arithmetic and Logic Unit

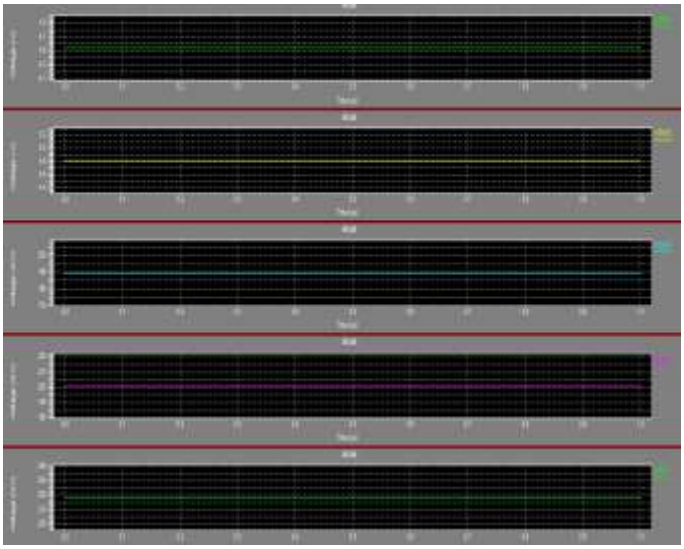

Fig 18Simulated output of 4 bit Arithmetic and Logic Unit

TABLE III. ANALYSIS RESULT OF DIFFERENT BLOCK OF ALU

Design	Cell	Power	No. of. Transistors
CMOS	2x1 MUX 4x1MUX Full adder	4.6073 e-6 watts 15.123 e-6 watts 16.675 e6 watts	6 18 28
GDI	2x1 MUX 4x1MUX Full adder	2.500000e-011 watts 3.700000e-011 watts 4.363099e-006 watts	2 6 10

TABLE. IV. POWER CONSUMPTION OF 4-BIT ALU

S.NO	Design	Power	No. of. Transistors
1	4 bit ALU design using CMOS	4204.5 e-006 watts	204
2	4 bit ALU design using GDI	1.492305e-003 watts	104

VI. CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuit static power dissipation is negligible when compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by $P = C_L f V_{DD}^2$. The power supply is directly related to dynamic power. power supply to ground connections are reduced in GDI implementation which reduces the dynamic power consumption. This work presents a 4-bit ALU designed in 250nm technology for low power and minimum area with GDI technique. Various topologies of multiplexer and full adder implementation is studied and compared. The 2x1 multiplexer, 4x1 multiplexer, full adder designed using GDI technique is

chosen for lowering power consumption and minimum possible area. Power dissipation , and the number of transistors of ALU were compared using CMOS, and GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques.

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