Low Power Modeling Of Topologically Compressed Static Flip-Flop.

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Abstract— The increasing market trends of extremely low power operated handy applications like laptop, electronics gadgets etc requires microelectronic devices with low power consumption. It is obvious that the transistor dimensions continues to shrink and as require for more complex chips increases, power management of such deep sub-micron based chip is one of the major challenges in VLSI industry. The manufacturers are always targeting for low power designs for the reason that to provide adequate physical resources to withstand against design hurdles and this lead to increases the cost and restrict the functionality of the device. This power reduction ratio is the highest among FFs that have been reported so far. The reduction is achieved by applying topological compression technique, merger of logically equivalent transistors to an eccentric latch structure. Fewer transistors, only three, connected to clock signal which reduces the power drastically, and the smaller total transistor count assures to retain the chip area as conventional FFs. In addition, fully static full-swing operation makes the cell lenient of supply voltage and input slew variation. An experimental chip design with 32 nm CMOS technology shows that almost all conventional FFs are expendable with proposed FF while preserving the same system performance and layout area. The performance of this paper is evaluated on the design simulation using Microwind 3.1 simulator

Index Terms — **Low power systems, Flip-Flops, Topological Compression, Supply Voltage, 32 nm CMOS Technology.**

Power dissipation has become a significant and more critical design parameter for VLSI circuits especially at deep sub-micron technology. The new requirement for portable operations of all types of electronic designs has invited for reduction in the weight and size of the device which is firmed by the number of power sources used and their lifetime. With the existing tendency of tumbling the transistor size, reducing the supply voltage and making more complex designs at chip level has resulted in large power dissipation. The variation of power dissipation with technology trends has predicted in figure1. This gives rise to rise in temperature of the chip thereby increasing need for cooling and packaging. But the system cost is also one of the key maker in the IC market diffusion. Therefore, there has been an increased demand for low power CMOS designs. When target is a low power circuit design, the search for the most advantageous solution must be done at each level of the design process. Decrease of power consumption makes a device more consistent. The necessitate for devices that consume a least amount of power was a major powerful force behind the development of CMOS technologies. At the circuit design level, there are many alternative to power savings exists for implementing combinational circuits. This is because all the important parameters leading power dissipation are identified to be of switching capacitance, transition activity, and short-circuit currents are strongly predisposed by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different presentation aspects become more significant.

There are three main sources of power dissipation in digital CMOS circuits, which are shortened in subsequent equation: **Ptot = P(dynamic) + P(static),** The first phrase represents the switching component of power, where CL is the load capacitance, f_{clk} is the clock frequency. Pd = CL * VDD2 * fclk Where: Pd=transient power consumption VDD =supply voltage. The second expression is due to the direct-path short circuit current, Isc, which contributes when both the NMOS and PMOS transistors are concurrently active, conducting current directly from supply to ground. Leakage current $I_{leakage}$ which can be generated from substrate injection and sub-threshold effect is mainly determined by fabrication technology considerations. The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage. And this leakage current can be modelled as $I_{leakage}$ = Is * e (qv/kT-1), where Is = reverse saturation current, v = diode voltage, k = Boltzmann's constant (1.38 * 10−23J/K), q = electronic charge (1.602 * 10−19C) and T = temperature. Therefore from above conclusion it is clear that reduction of V_{DD} emerges as a very useful resource to limit the power consumption. Yet, the saving in power dissipation comes at a major cost in terms of increased circuit delay.
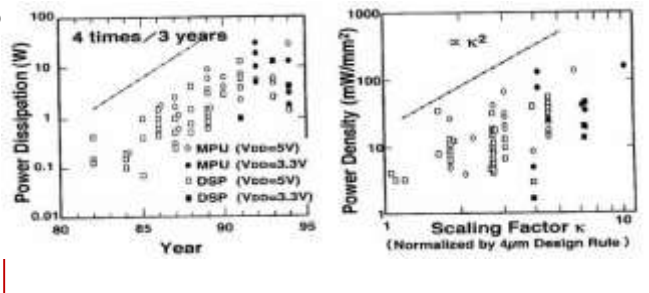
Figure1: Power Dissipation Vs Technology Trends

DESIGN DEVELOPMENT

It is observed with traditional FFs, the FF reduces power dissipation by 75% at 0% data activity. This power reduction ratio is the maximum amongst FFs that have been practically observed so far. The decrease is accomplished by applying topological compression method, fusion of logically equivalent transistors to an eccentric latch structure. A few numbers of transistors, only three, connected to clock signal to diminish the power drastically, and the smaller total transistor count assures the same cell area as conventional FFs. In addition, fully static full-swing working principle makes the cell lenient of supply voltage and input slew variation. The proposed architecture of topologically compressed flip-flop (TCFF) is realized in 32nm CMOS technology.

In Large Scale Integration usually more than 50% of the power is dissipated in random logic of and thereby in almost all sequential design half of the power is dissipated by flip-flops (FFs). During the past research, several low-power FFs have been swift into logic development. However, in actual chip design, the conventional FF is still used most often as a ideal FF because of its well-balanced power, performance and cell area. The intention of this paper is to present a clarification to attain all of the goals of power reduction without any degradation of timing performance and the target area.

Active Designs:

Various designs of flip-flops, their topologies and designs are discussed here and there by referred with proposed architecture here with.

Differential Sense-Amplifier Flip-Flop (DiffFF)

Figure2 shows a typical circuit of differential sense-amplifier type FF (DiffFF). This type of circuit is very useful to amplify small-swing signals; therefore it is generally used in output of memory circuits. Practical observations are predicted for this FF that effect of power reduction goes down in the condition of lower data activity, since these kinds of circuits have pre-charge operation in every clock-low state. Furthermore, if we use reduced clock swing, a tailored clock generator and an extra bias circuit are essential which leads to more and more power dissipation.
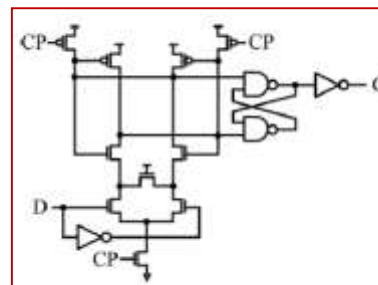

Figure2: Differential Sense-Amplifier FF

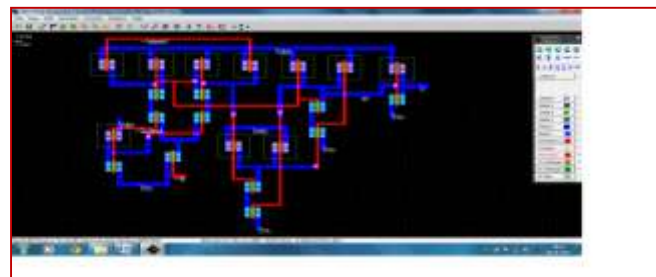The 32 nm technology based layout of this DiffFF is shown in Figure3.

Figure3: DiffFF layout design

Cross-charge Control Flip-Flop (XCFF)

The circuit design of cross-charge control FF (XCFF) is shown in the figure4. The attribute of this circuit is to drive output transistors autonomously in order to reduce charged and discharged gate capacitance. Nevertheless, in actual operation, some of the internal nodes are pre-set with clock signal in the case of data is high, and this operation dissipates additional power to charge and discharge internal nodes. As a consequence, the effect of power reduction will decrease. Circuits including pre-set condition is also suffers with the same problem.
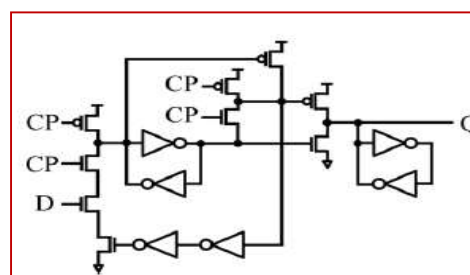

Figure4: Cross-Charge Control FF

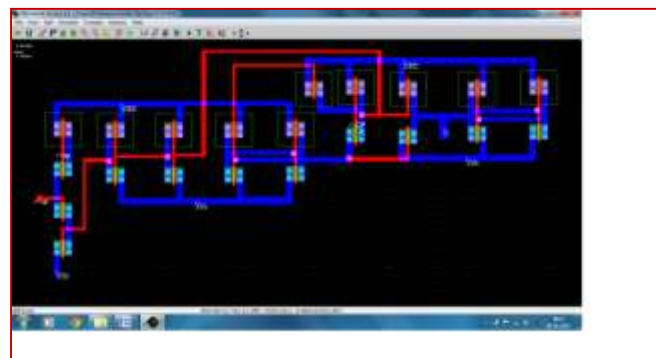The 32 nm technology based layout of this XCFF is shown in Figure5.

Adaptive- Coupling Flip-Flop (ACFF)

The adaptive-coupling type FF (ACFF) is shown in Figure6; the design of this kind of FF is mainly relay on a 6-transistor memory cell. In this design, as an alternative to the usually used double-channel transmission-gate, a single channel transmission-gate with extra dynamic circuit has been used for the data line in order to diminish clock-related transistor count. Nevertheless, in this circuit, delay is affected without difficulty by input clock slew variation because different types of single channel transmission-gates are used in the same data line and connected to the same clock signal. Furthermore, performance metrics of single-channel transmission-gate circuits and dynamic circuits are strongly affected by process variation. Accordingly their optimization is relatively difficult, and performance humiliation across various process corners is a major issue.
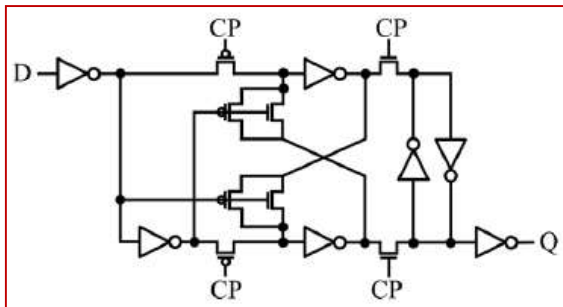

Figure6: Adaptive- Coupling Flip-Flop

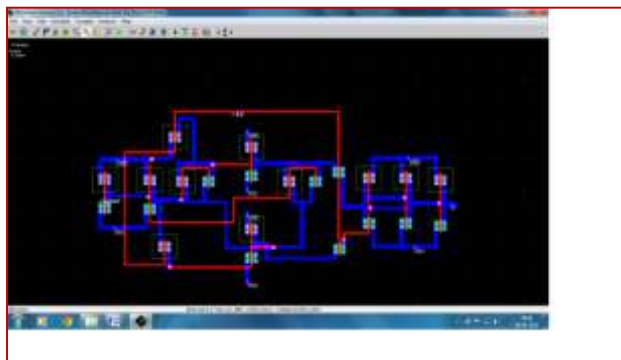The 32 nm technology based layout of this ACFF is shown in Figure7

Figure7: ACFF layout design

Proposed design: Topologically Compressed FF (TCFF)

Subsequent to study and estimation of power budget for various kinds of sequential circuits, an eccentrically structured FF is proposed as shown in Figure8. This FF contains various types of latches in the master and the slave parts. The slave-latch is a well-known Reset-Set (RS) type, but the master-latch is an unbalanced single data-input type unit. The characteristic of this circuit is that it operates in single phase clock, and it has two sets of logically equivalent input AND logic, X1 and Y1, and X2 and Y2. Based on this

proposal, logically corresponding transistors are fused as described here with. For the PMOS side, two transistor pairs in M1 and S1 blocks can be joined each other. While either N3 or CP is Low, the shared common node becomes V_{DD} voltage level, or N2 and N5 nodes are controlled by PMOS transistors gated N1 and N4 independently. When both N3 and CP are High, both N2 and N5 nodes are pulled down to VSS by NMOS transistors gated N3 and CP. As well as M1 and S1 blocks, two PMOS transistor pairs in M2 and S2 blocks are shared. For the NMOS side, transistors of logically comparable operation can be shared as well. Two transistors in M1 and M2 blocks can be shared. Transistors in S1 and S2 are shared as well. Additional to this in the PMOS side, CP-input transistors in S1 and S2, can be fused, because N2 and N3 are logically inverted to each other. When CP is Low, both nodes are in VDD voltage level, and either N2 or N3 is ON. When CP is High, each node is in self-sufficient voltage level. In reflection of this performance, the CP-input transistors are shared and connected. The CP-input transistor is working as a switch to connect S1 and S2. This procedure leads to the circuit as shown in Figure8. This circuit consists of seven fewer transistors than the actual circuit. The number of clock-related transistors is only three. Interestingly the proposed unit does not contains any dynamic circuit or pre-charge circuit which leads to the advantage of target reduction of power dissipation. The reduction method is known as Topological Compression (TC) method and the relevant FF is Topologically-Compressed Flip-Flop (TCFF).
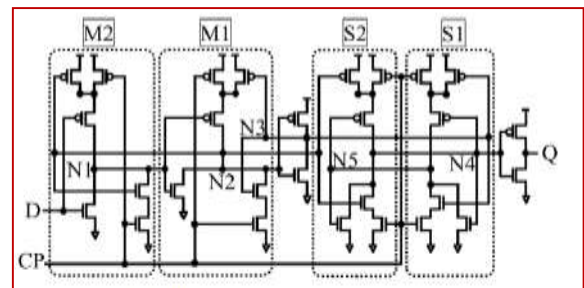

Figure8: Topologically Compressed FF

The 32 nm technology based layout of this ACFF is shown in Figure9
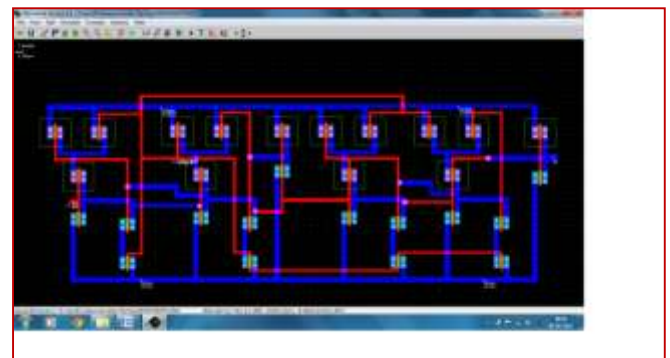

Figure9: TCFF layout design

All the layout design description of the above article is simulated and analyzed using Microwind 3.1 Layout design tool and physical design layout results are observed separately with the help of 32nm technology, it is noticed that

at some instance of simulation time the power and time delays are greatly improved with the implementation of proposed architecture, the various results are shown below.
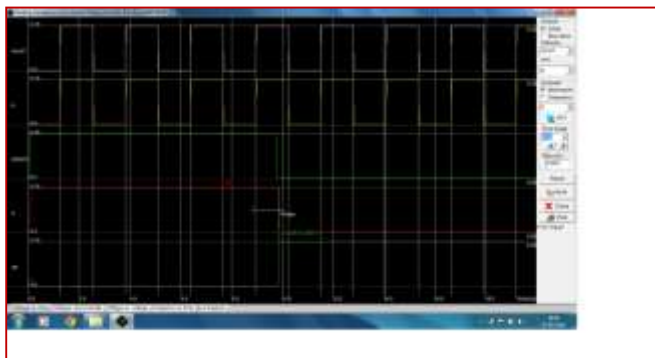

Figure10: Simulation output of DiffFF
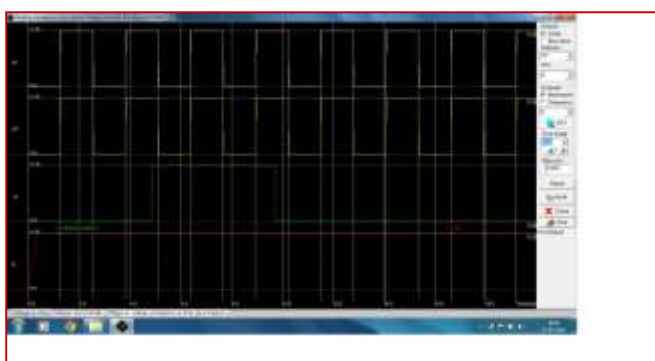
Figure11: Simulation output of XCFF
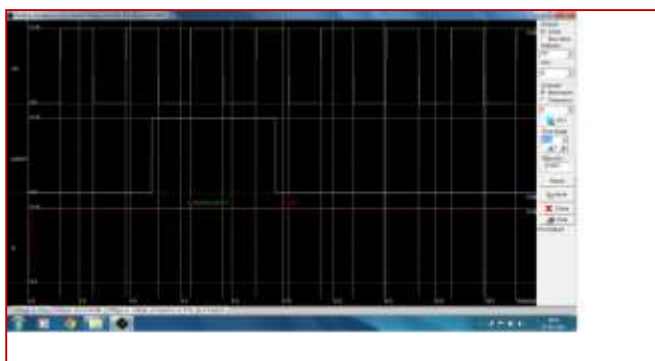
Figure12: Simulation output of ACFF

Figure12: Simulation output of TCFF

The performance metrics are summarized in the following Table1.

TABLE 1
SUMMARY OF PERFORMANCE REPORT

parameter	DiffFF	XCFF	ACFF	TCFF
Power	1.110μW	1.986μW	2.646μW	0.681μW
Delay	897 pS	538 pS	521 pS	320 Ps
I_{dd} Max.	0.018 A	0.045mA	0.027mA	0.017Ma
V_{dd} Max.	0.35 V	0.35 V	0.35 V	0.35 V
W/L	1/0.04	1/0.04	1/0.04	1/0.04

This paper analyzes the existed FF topologies and suggested a compressed FF to overcome unnecessary power dissipations occurred in the FF due to their large switching activity. The proposed work may eliminate the problem of CMOS total power dissipation between logic transitions occurred in FFs. Topologically Compressed FF design improves the area utilization also this paper has realized with Layout design tools and the relevant layouts are analyzed and various physical parameters are studied at 32 nm Technology. Such designs are suggested to exhibits a competitive performance with current work.

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