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A 16-Bit Ripple Carry Adder Design Using High Speed Modified Feedthrough Logic

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Abstract: ***This paper presents the design and simulation of high speed 16-bit ripple carry adder using a new CMOS logic family called feedthrough logic(FTL). FTL arithmetic circuits provides for smaller propagation time delay when compared with the standard CMOS technologies. The proposed circuit has very small propagation time delay as compared to existing dynamic logic circuits. The proposed modified feedthrough logic completely eliminates the output distortion occurs in existing FTL structure having reference voltage Vdd/2. In This paper, a long chain of inverters (20-stages) and 16-bit ripple carry adder is designed by modified feedthrough logic. Then comparison analysis has been carried out by simulating the circuits in 180nm CMOS process technology from TSMC using Tanner EDA 14.11.***

Keywords: Feedthrough logic(FTL), High speed, Ripple carry adder(RCA), Propagation delay, Domino CMOS logic**.**

1. INTRODUCTION

In modern digital system, arithmetic circuits have always been an important building block in delivering high-performance, energy efficient computing, because arithmetic operations such as addition and binary number comparison are two of the most commonly used computing instructions**.** Besides the manufacturing CMOS process, the two most critical design considerations for arithmetic circuits are the logic style and micro-architecture. As CMOS technology further scales down to allow faster IC with less energy consumption, continuous circuit innovation, in particular, logic implementation, is a necessity in order to avail its benefits.

Over last two decades many improvements has been done to enhance the speed of digital circuitry for example dynamic logic [1]. But dynamic logic suffers from charge leakage, charge sharing and requirement of additional output inverter during cascading of logic blocks. To avoid such problems a new CMOS domino logic family called feedthrough logic was proposed in [3].This logic works on domino concept along with the important feature that output is partially evaluated before all the inputs are valid, and due to use of extra supply voltage [3] very fast evaluation in computation blocks have been achieved.

The FTL concept was successfully used for design of high speed and low power arithmetic circuits in [2]. We also extend our research to high speed circuits and analyzed the 16-bit ripple carry adder (RCA) sensitivity against capacitive load (fF) and temperature (^{o}c). Our results showed substantial performance improvement in FTL with respect to basic FTL structure.

In this work a 16-bit ripple carry adder is designed using modified feedthrough logic and comparison analysis has been carried out between existing FTL structure and modified FTL structure using 180nm CMOS process technology from TSMC Supply voltage is fixed for all simulations and is 1.8v, at 10fF capacitive load.

2. BASIC FTL PRINCIPLE

The basic structure of FTL is shown in Fig. 2 (a). It consist a NMOS reset transistor Mr for resetting the output node to low logic level, a pull up PMOS load transistor Mp and an NMOS block. Mp and Mr controlled by the clock signal CLK.
The basic principle of operation of a FTL circuit was presented in [3] and is explained here. During CLK=1, (reset phase) Mr turned on and the output node pulled to ground through Mr . Since the output node is pulled to ground during reset phase the need of inverter during cascading is eliminated.

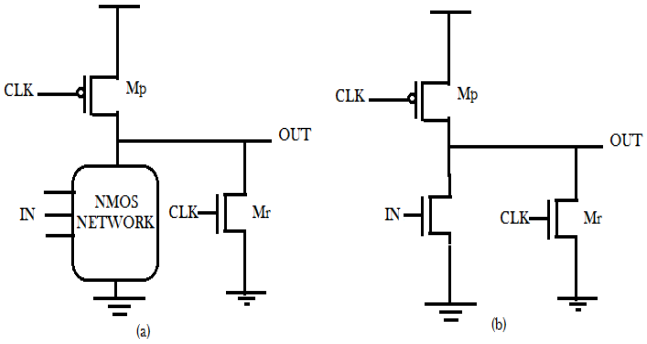
When CLK goes low (evaluation phase) Mr is turned off and the output node conditionally evaluates to logic high (V_{OH}) or low (V_{OL}) depending upon input to NMOS block. If the NMOS block evaluates to high then output node pulled toward V_{DD} otherwise it will remain at logic low.

A long chain of inverter (1st to 29th stages) is designed using existing FTL structure [3]. When CLK=1, all the output nodes are at logic zero. When CLK goes low, the output node of the cascaded gate rises to the gate threshold voltage V_{TH}. At this point any small variation in the input node causes a fast variation in voltage at the output node. At this stage if NMOS block evaluates logic high then partial transition from V_{TH} to V_{OH} occurs otherwise V_{OL} obtained. Hence a fast evaluation is done due to use of feedthrough logic technique.

Fig. 2(a) shows basic FTL structure as in [3]. Fig. 2(b) shows Inverter designed by basic FTL and, Fig. 2(c) shows output waveform of 1st to 29th stages.

Despite of high speed, FTL structure suffers from low noise margin, high dynamic power dissipation as described in [3], it is more convenient in digital circuits where high switching rate

is essentially requirement. Dynamic power dissipation is also quite high in FTL than static CMOS logic.



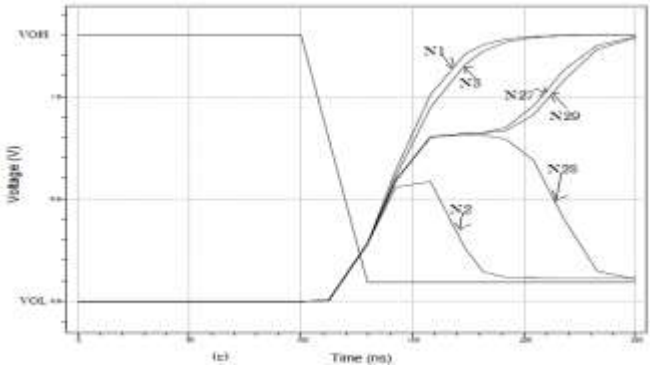


Fig. 2:- (a) Basic FTL structure, (b) Inverter using basic FTL, (c) Output waveform of 1st to 29th inverter stages.

3. PROPOSED MODIFIED FTL

The proposed modified FTL circuit is presented in fig. 3(a). The circuit contains two extra NMOS transistors M3 and M4 compared to basic FTL structure having reference voltage Vdd/2 as in [3]. These two transistors prevent the leakage current through NMOS block. This is done to avoid glitches in output signal caused by Vdd/2 source. The operation of this circuit is similar to that of FTL in [3]. During reset phase i.e. when CLK = 1, output node is pulled to V_{dd2} through M2, when CLK goes low (evaluation phase) M2 is turned off and the output node conditionally evaluates to logic high (V_{OH}) or low (V_{OL}) depending upon input to NMOS block. If the NMOS block evaluates to high then output node pulled toward V_{dd} i.e. $V_{OH} = V_{dd}$, otherwise it goes at logic low i.e. V_{OL}.

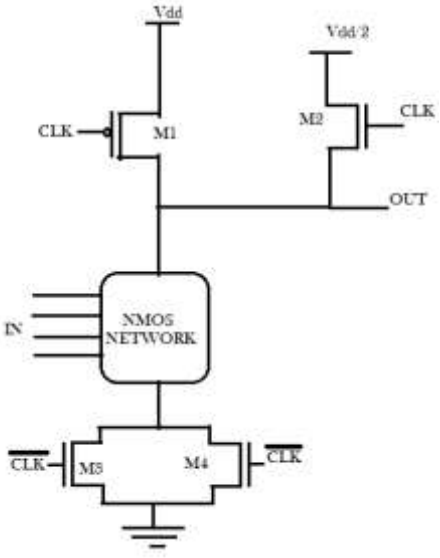


Fig. 3(a) Proposed Modified FTL structure

4. PERFORMANCE ANALYSIS OF PROPOSED FTL LOGIC

The proposed FTL structure has been verified against basic FTL structure in [3] by designing a long chain of inverters consisting 20 stages. We have used 180nm CMOS process technology model file from TSMC at 25^0C. Power supply V_{dd} is constant for all simulations and is equal to 1.8V. Circuits are simulated in Tanner EDA 14.11 tool.

Table I shows the dynamic power consumption, average values of propagation delays (tp), and power delay product comparison of proposed modified FTL and the existing FTL for 10 fF capacitive load at 100 MHz. When simulating long chain of inverters (20 stages), the proposed FTL shows 32% faster speed with respect to existing FTL.

Logic Family	Power (µwatt)	Propagation delay(nsec)	PDP (µwatt*nsec)
FTL	887	0.795	705.17
Modified FTL	857	0.540	462.78

Table I :- Simulation result for FTL and Modified FTL (20 stages of inverter)

5. 16-BIT RIPPLE CARRY ADDER DESIGN

Fig.5.(b),and (c) shows basic sum and carry cell designed by proposed modified feedthrough logic. Simulation is done in 180nm technology at 25° C using Tanner EDA 14.11 Tool. Bar graph shows power dissipation, propagation delay and PDP of 16-bit RCA using modified FTL and existing FTL.

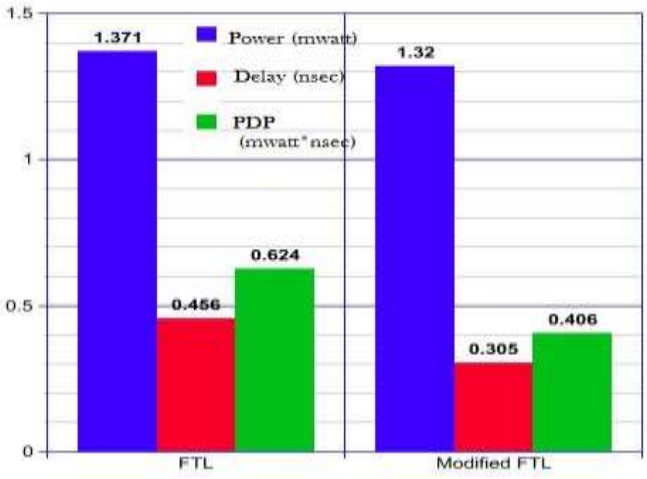


Fig. 5(a) Bar graph showing comparison analysis between existing FTL and Modified FTL for 16-bit RCA

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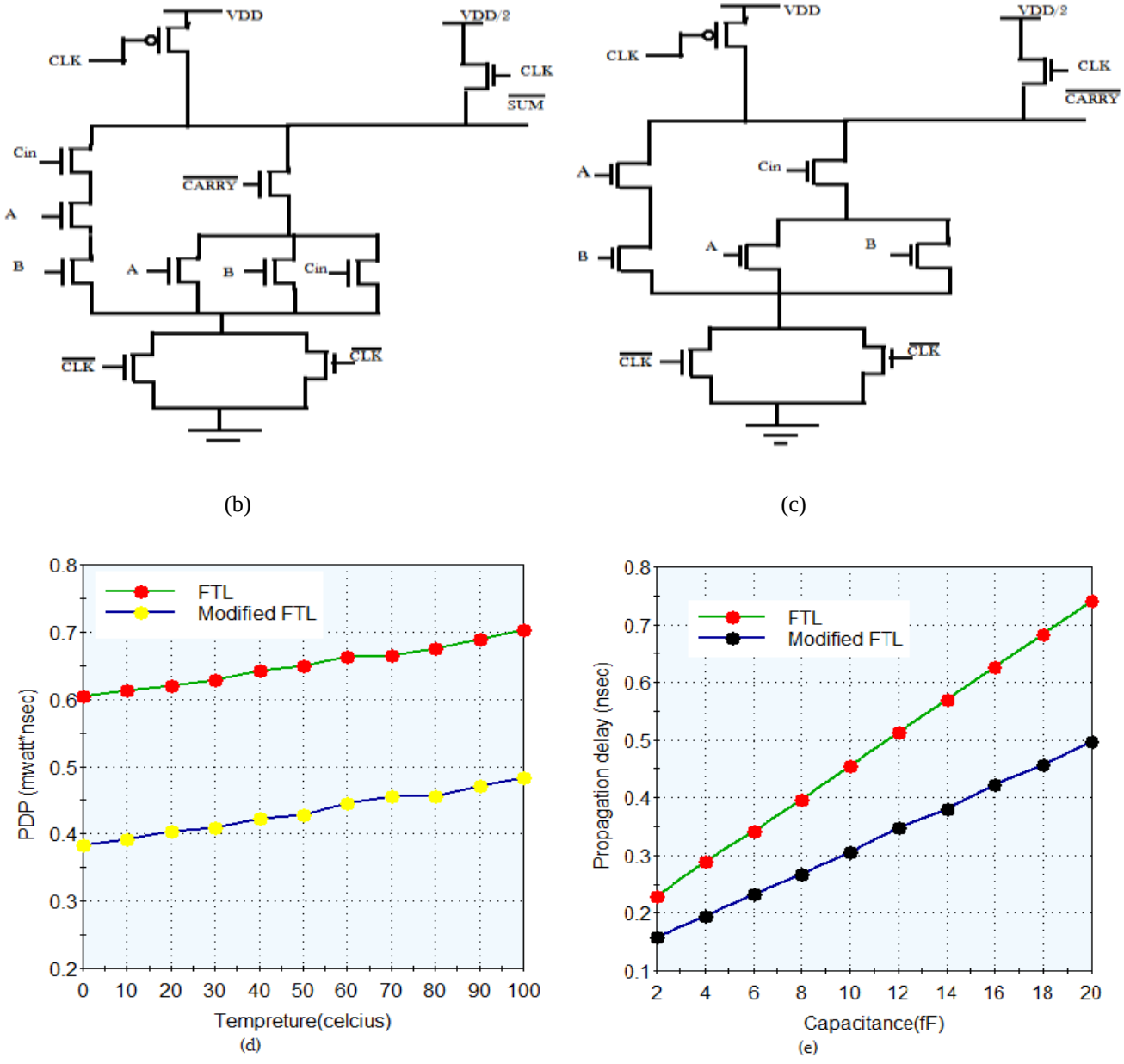

Fig. 5 (b) Sum cell designed by modified FTL, (c) Carry cell designed by modified FTL, (d) Effect of temperature on PDP, (e) Effect of load capacitance in propagation delay.

6. BASIC FTL VERSUS MODIFIED FTL

From bar graph fig.5 (a) we can conclude that our proposed modified FTL consumes approximately equal power but gives much better speed than existing FTL. And in proposed modified FTL structure we have eliminated the problem of distortion created by voltage source Vdd2 in basic FTL with reference voltage Vdd2 [3].

Fig. 5 (d) shows the effect of temperature on power delay product. Our proposed modified FTL structure has better PDP than basic FTL. Fig. 5 (e) shows effect of load capacitance on propagation delay. It is clear that modified FTL structure has less sensitive to load capacitance variation than basic FTL. However the propagation time delay is very much sensitive to load capacitance variation in both the structures. The power dissipation in both structures is almost independent to load capacitance variation.

All the above results clearly explain that our proposed modified FTL structure is more suitable for high speed applications than basic FTL without compromising with power dissipation.

7. CONCLUSION AND FUTURE SCOPE

In this paper, we proposed high speed dynamic circuit. The proposed circuit is simulated in 180nm CMOS process technology from TSMC using tanner EDA 14.11 tool. The proposed modified circuit when compared with recently modified circuits does not enhance speed at a cost of high power dissipation. It consumes approximately equal power

as basic FTL does and have higher speed. The simulation for a long chain of inverter (20-stage) and 16-bit ripple carry adder is also carried out in this work. The simulation result confirms that for a given load and at same frequency of operation the power delay product of the proposed circuit is much better than that of existing FTL structure. The proposed circuit can be used for designing of high speed processor where high speed is essential requirement. Furthermore it can be used in communication system to overcome the problem of delay.

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Avinash Singh received his B-tech degree in Electronics & Communication Engineering from Maharana Pratap Engineering College affiliated to Uttar Pradesh Technical University, Lucknow, India and is currently working toward his M-Tech degree in Microelectronics Engineering with the research interest in reducing power consumption and enhancing speed of digital circuits, from Institute of Engineering and Technology, Lucknow Uttar Pradesh

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