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Implementation of Digital Pixel Sensor Based Parallel Architecture For Automatic Braking System in Automobiles

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Abstract- While automobiles moving on the road, if a pedestrian or an animal or anything commits to come on to the road unintentionally, then their motion features will be extracted, by which the automatic braking system of the automobile will be activated. Row-Parallel Processing of the input image achieves directional edge filtering and essential motion features are extracted with the Pixel-Parallel Processing based on the Digital Pixel Sensor(DPS) Technology.

Keywords- Motion features, Parallel Processing, Digital Pixel Sensor.

I. INTRODUCTION

Object Tracking using extracted motion features has its major importance in various applications such as Human Computer Interaction [1], Video Surveillance [2], Surgery Support, Automotive Vehicle Control, Sign Language Interpretation [3], [4], Remote Gesture Control [5] and so forth. This paper deals with the object tracking in automobiles. While automobiles moving on the road, if a pedestrian or an animal or anything commits to come on to the road unintentionally, then their motion features will be extracted, by which the automatic braking system of the automobile will be activated.

Software based Object Tracking is more efficient in extracting motion features but failed in its usage in Real Time. For real time application Virtex5 is used. The Virtex5 xc5vlx220 is intended for logic intensive applications. But utilization percentage of number of registers, LUTs, LUT-FF pairs is very less in Virtex5. This paper used FPGA Spartan3 as its utilization percentage is more.

II. EXISTING SYSTEMS

Motion Features are extracted using Software based Object Tracking system. Matlab is a high-level tool used in interactive environment including Computer Vision and Image Processing and it is also a technical computing language. Matlab is used to develop quickly vision applications with
the fast coding which is its positive side. When Matlab encountered with a problem, it can automatically stop the script but it doesn't have specific programming problems like memory allocation. Also it allows users to execute code using command lines even an error occurs and fix the error while the code is still in execution mode. Software based Object Tracking is more efficient in extracting motion features but failed in its usage in Real Time.

The Virtex series of FPGAs are based on Configurable Logic Blocks (CLBs), where each CLB is equivalent to multiple ASIC gates and multiple slices are present in each CLB. Input/ Output pins on the Virtex chip are controlled by I/O Blocks which support a variety of signaling standards. I/O Banks support a different voltage where each I/O Bank is a group of I/O pins. The Virtex5 xc5vlx220 is intended for logic intensive applications. Xilinx increased the four-input LUTs to six-input LUTs with in this Virtex5. The new six-input LUT reduced number of LUTs per device which becomes an advantage of the Virtex5 and also increased the better handling of complex combinational functions. But utilization percentage of number of registers, LUTs, LUT-FF pairs is very less in Virtex5 compared to FPGA Spartan3, so here the motion features are extracted using the FPGA Spartan3.

III. MOTION-FEATURE-EXTRACTION ALGORITHM

Motion Feature Extraction is be done in two steps [6]. One is Merged Significant Edge Map Generation and in this step the static features for every frame are extracted. The second step is Motion Feature Extraction, in which motion features are extracted. Fig 1 shows the block diagram of how the motion features will be generated from the input image.

A. Merged Significant Edge Map Generation

Fig 2. describes the merged significant edge map generation from the input image. For the input

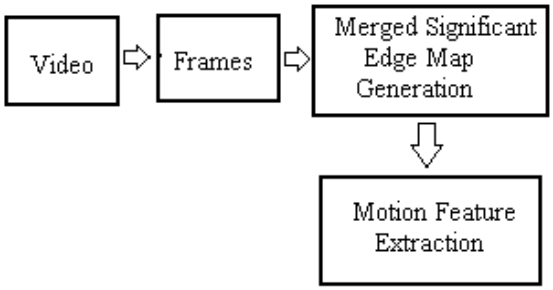

Fig 1. Block Diagram

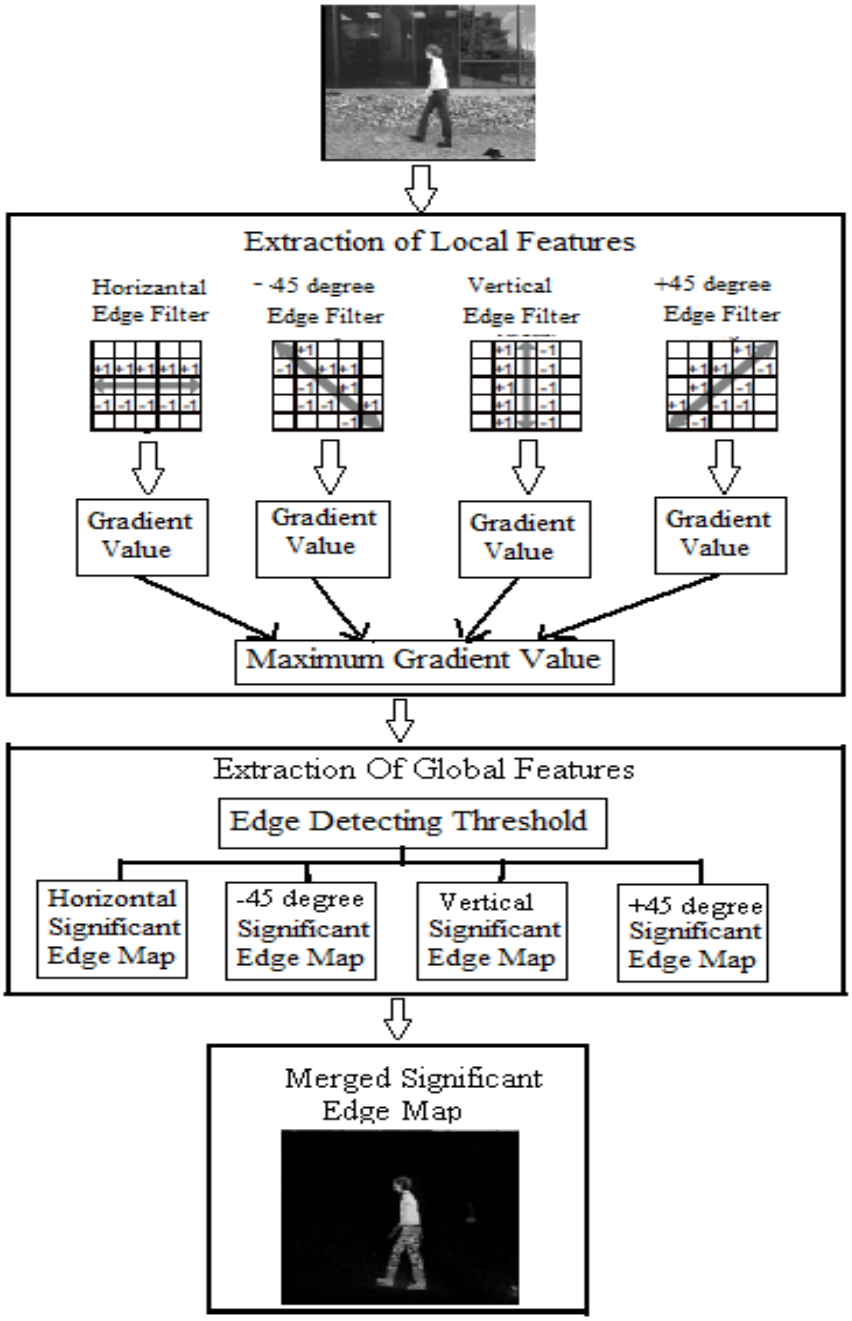

image four directional edge filtering (horizontal, +45◦, vertical, and −45) [7] is performed. With this four directional edge filtering two main processes takes place. They are Extraction of Local Features and Extraction of Global Features. In the fig 2,these two processes are illustrated. The local Feature Extraction is shown in the top of the figure, where initially convolutions between 5X5 filtering kernels and 5X5 pixel sites is performed. Selection of the Maximum Gradient Value and the Edge Direction is done based on the Convolution results.

Fig. 2. Merged Significant Edge Map Generation

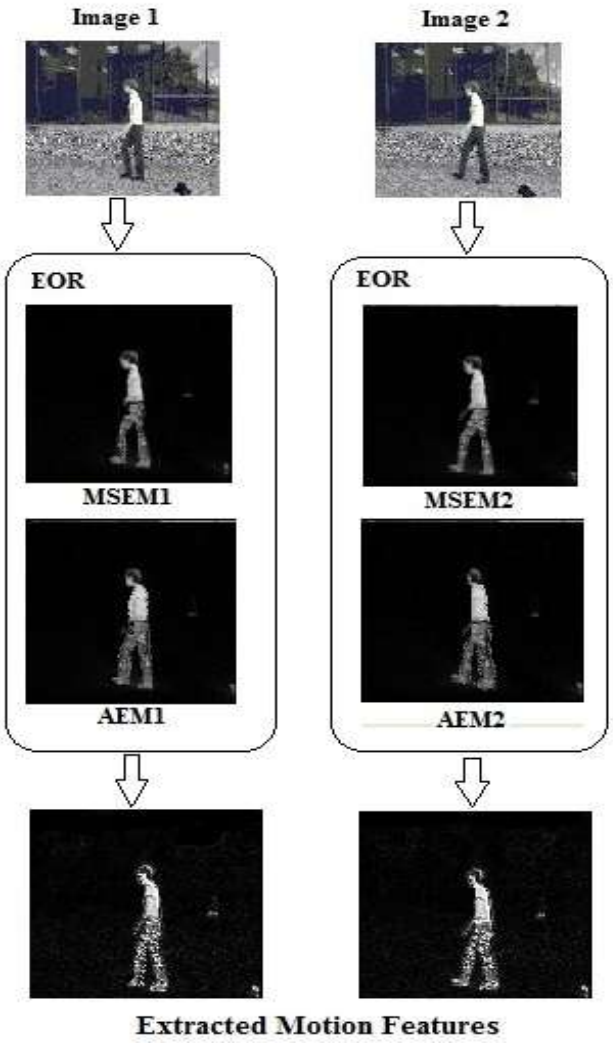

Fig 3.Motion Feature Extraction

As the LFE contains a lot of redundant information, significant edge maps are generated which contains the salient features. By performing the Logical OR operation among the four significant edge maps, they are merged to form the Merged Significant Edge Map (MSEM).

B. Motion Feature Extraction

Fig 3 shows the extraction of Motion Features from the Merged Significant Edge Maps. For the first image Merged Significant Edge Map is generated and it is considered as the Accumulated Edge Map (AEM) for this image. For the second image MSEM is generated and logical OR operation is performed between previous AEM and present MSEM in order to update the Accumulated Edge Map. Motion Features are extracted by performing Exclusive OR operation between the Merged Significant Edge Map and Accumulated Edge Map of present image. By this the automatic brakes of the automobile will be activated.

C.VLSI Architecture

Digital Pixel Sensor Technology [8] performs the Analog to Digital conversion of input image. Every four pixel rows of image are grouped together to scan them with 5X5-pixel-size filtering kernels. All the pixel rows of the image are controlled by the Block-readout control [9]. In the fig 4 each LFE circuitry receives two 4X8 data blocks to form 8X8 blocks of data. Kernel Convolution is carried out in row parallel manner. With these results, the motion features are extracted in the pixel parallel manner.

Field-Programmable Gate Arrays (FPGA's) unit of measurement versatile and reusable high-density circuits which can be simply re-configured by the designer, enabling the VLSI vogue / validation /simulation cycle to be performed additional quickly and fewer expensive . Increasing device densities have prompted FPGA manufacturers, like Altera and Xilinx, to combine the larger embedded parts, additional as DSP blocks, embedded processors and multipliers.

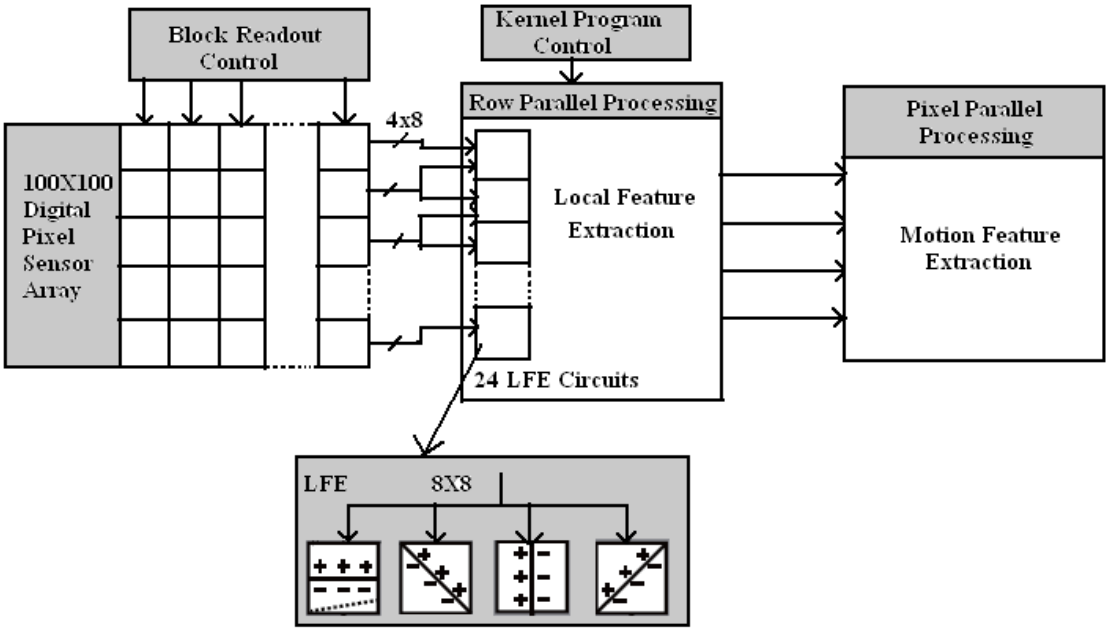

Fig 4. VLSI Architecture

Fig 5 shows the experimental setup of Object Tracking System. One in each of the recent subject enhancements at intervals the Vertex family, Xilinx Spartan architectures is that the introduction of the PowerPC405 hard-core embedded processor and small Blaze (Soft IP).

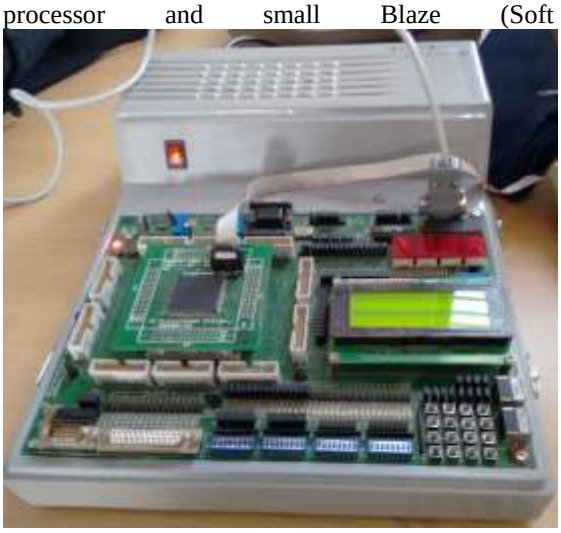

Fig 5. Experimental Setup of Object Tracking System

Due to the advancement inside the fabrication technology and thus the rise inside the density of logic blocks on FPGA, the employment of FPGA is not restricted to any extent further to debugging and prototyping digital electronic circuits. As a results of the huge similarity realizable on FPGA and thus the increasing density of logic blocks, it's

obtaining used presently as a replacement to ASIC solutions throughout a few of applications where

the time to plug is very important and on entire embedded processor systems unit of activity enforced on these devices with soft core processors embedded inside the system.

The small Blaze soft core processor is incredibly configurable, allowing you to make your mind up on a selected set of selections required by your vogue. However this paper uses FPGA Spartan3 for Object Tracking. A high configurable small blaze processor was used, our rule was written among the system C cryptography degree synthesized exploitation the XILLINX Platform Studio and our output unit seen through VB application that reads the pixels values of the image that comes from the FPGA to pc through UART communication.

IV. SIMULATION RESULTS

The experimental results of Object Tracking System are shown below.

a. Input Image

b. Merged Significant Edge Map

c. Motion Features

Fig 6. Simulation Results

Fig 6 shows the Simulation Results of a Dog crossing the road while the automobile is stopped because after extracting the motion features of the dog the automatic brakes of the automobile are activated.

TABLE I

COMPARISON RESULTS

Logic Utilization	Virtex5 xc5vlx220			Spartan3 3s200tq144-4		
	Used	Available	Utilization	Used	Available	Utilization
Number of Slice Regis-ters	4916	138240	3%	1880	1920	97%
Number of slice LUTs	6595	138240	4%	2971	3840	77%

In the comparison Table I between Virtex5 and Spartan3, we come to know that the utilization percentage of slice registers and LUTs is more in Spartan3 compared to Virtex5.

V CONCLUSION

A self speed adaptive Motion Feature Extraction is achieved using Row Parallel and Pixel Parallel Processing based on Digital Pixel Sensor Technology. Object Tracking has its usage in automobiles, where automatic bakes will be activated after extracting motion features for safer driving.

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