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A Design of Low Power Low Area High Speed Full Adder Using GDI Technique

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***Abstract*— Full Adder is the basic building block for various arithmetic circuits such as compressors, multipliers, comparators and so on. 1-bit Full Adder cell is the important and basic block of an arithmetic unit of a system. Hence in order to improve the performance of the digital computer system one must improve the basic 1-bit full adder cell. In this, Full Adder is designed by using Hybrid-CMOS logic style. Hybrid designs are used to build a low power Full Adder cell. In the hybrid logic style more than one network is present. In general, it consists of three modules. Here we proposed the new Full Adder design by using the GDI (Gate Diffusion Index/Input) technique.GDI is a new method for reducing the power consumption, propagation delay, with less transistor count and power delay product (PDP).The simulation results are carried out on Tanner EDA tool. The simulation shows that the design has more efficient with less area, less power consumption and high speed as compared to CMOS techniques.**

Keywords—***GDI technique, Low power, Full Adder, High speed.***

I. INTRODUCTION

Full Adder is the heart of the digital and data processing application like specific integrated circuit (ASIC) is its data path. At the heart of data path and addressing units in turn are arithmetic units such as the comparators, adders and multipliers. Finally , the basic operation found is most arithmetic components is the binary addition.

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application specific digital signal processing (DSP) architectures and micro processors . This module is the core of many arithmetic operations such as addition/subtraction, multiplication, divison and address generation. Our aim is the design of a Full Adder having low power consumption, low area and low propagation delay results of great interest for the implementation of modern digital systems.

Full Adder plays an important role in the arithmetic related designs, many IC designers puts a lot of efforts on Full Adder circuit research. Consequently, there are many different types of Full Adders have been developed for a variety of different applications.

Several logic styles are used for designing the Full Adder. Normally Full Adder is designed by using the CMOS structure [2]. Due to the CMOS logic style no exact logic will be passed. Here we are using the hybrid CMOS design style to design the Full Adder.

The standard static CMOS [3] Full Adder is depends on the regular CMOS structure with conventional pull-up (PMOS) and pull-down (NMOS) transistors provides the good driving capabilities and full swing output. In this the main drawback is input capacitance is high. Due to this the speed of the structure is degraded. The dynamic CMOS [3] logic style speed is higher but the drawbacks are high load, switching activities are high, charge sharing.

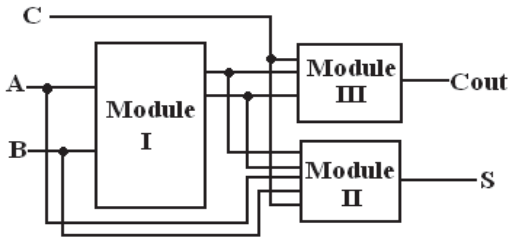

Fig.1. Full adder logic architecture with three modules.

Hybrid designs are used to build a low power Full Adder cell.The main aim is to reduce the number of transistors in the adder cell and to reduce the number of power dissipating nodes. To design the hybrid CMOS Full Adder it interconnects more than one module is shown in Fig.1.

In this design style full adder structure is designed by breaking the full adder into three modules. First module is an XOR-XNOR circuit [12] which is useful to drive the other modules. Module I having good driving capability and provides full swing output. Second module is a SUM circuit [12] which uses the output of Module I and also third input to produce the sum output. Module II is also a XOR circuit. Third module is a CARRY circuit [12] which uses the output of Module I and also third input to produce the carry circuit. Module III is also a multiplexer circuit.

Hybrid-CMOS logic design and gate diffusion index techniques are presented in this paper. One of the efficient low power technique known as Gate Diffusion Input (GDI) [7] is proposed by Morgenshtein . It is a genius and power efficient

design with lesser number of transistor counts. GDI technique is used to reduce power consumption, propagation delay while

maintaining low complexity of logic design . Here we have introduced a 10-T GDI based full adder circuit which can be used for low power applications. This paper is organized as follows. Full Adder is design by using hybrid-CMOS logic style is described in Section II. Section III explains the GDI based Full Adder. Section IV gives a conclusion.

II. HYBRID-CMOS FULL ADDER

The term hybrid means it interconnects more than one network. The 1-bit full adder having three binary inputs A, B, & C_{in} and two outputs sum (S) and carry (C_{out}) [10] are given by

$$Sum = A \oplus B \oplus C_{in} \quad (i)$$
$$S = C_{in}' . (A \oplus B) + C_{in}(A \odot B) \quad (ii)$$

$$Carry = A.B + C_{in}(A \oplus B)$$
$$= C_{in}(A \oplus B) + A(A \odot B) \quad (iii)$$

$$A \oplus B = A'B + AB' \quad (iv)$$
$$A \odot B = A.B + A'B' \quad (v)$$

In the hybrid-CMOS Logic design , we get module I outputs are XOR (H) and XNOR (H') for A and B inputs. These input signals and another input C_{in} are useful for the input of module II and module III.

Module I is a XOR-XNOR circuit. Module II is a Sum circuit and Module III is a Carry circuit. The new expression for Sum and Carry by using XOR output H and XNOR output H'[1] are,

$$Sum = H \oplus C_{in}$$
$$= H.C_{in}' + H'.C_{in} \quad (vi)$$

$$Carry = H'.A + H.C_{in} \quad (vii)$$

$$H = A \oplus B \quad (viii)$$
$$H' = A \odot B \quad (ix)$$

It is clear that H and its complement H' are the key variables in both adder equations. If the generation of H and H' is optimized, this could greatly enhance the performance of the full-adder cell. A special module should be dedicated to the generation of these two signals. Another module is needed to generate the sum using H , H' and C_{in}. A third module is needed to generate C_{out} given H , H' , A , and C_{in} .

A Full Adder is made up of an XOR–XNOR module, a sum module and a carry module [4]. The XOR–XNOR module performs XOR and XNOR [11] logic operations on inputs A and B, and then generates the outputs H and H′. Subsequently, H and H′ both are applied to the sum and the carry modules for generation of sum output S and carry output C_o. A block diagram for the full adder with hybrid-CMOS logic style is shown in Fig.2.

In the designing of the circuit we interconnect three modules. Those are Module I (XOR-XNOR), Module II (SUM circuit), Module III (CARRY circuit). This full adder contains 16 transistors. In the hybrid-CMOS logic style the designer has freedom to select the different modules based on the application.

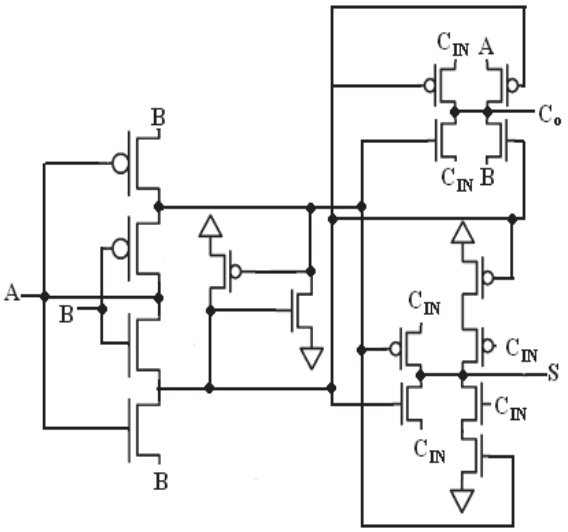

Fig.2. Hybrid-CMOS Full Adder

In the Hybrid CMOS Full Adder the Module I XOR/XNOR module was designed using 6 transistors using CPL with swing restored logic [3] was added in order to generate full output swing.

Module II XOR between H and C_{in} was designed in such a way that all the input logics should have a high logical swing output.

Module III Multiplexer was designed with same as the Module II for every input it should have high logic swing.

The main aim is to design a low power full adder cell [9]. This design has less area occupation than the previous full adder. The drawback of this design is no exact logic will be passed due to the CMOS logic style.

A. Simulation results for Hybrid-CMOS full adder

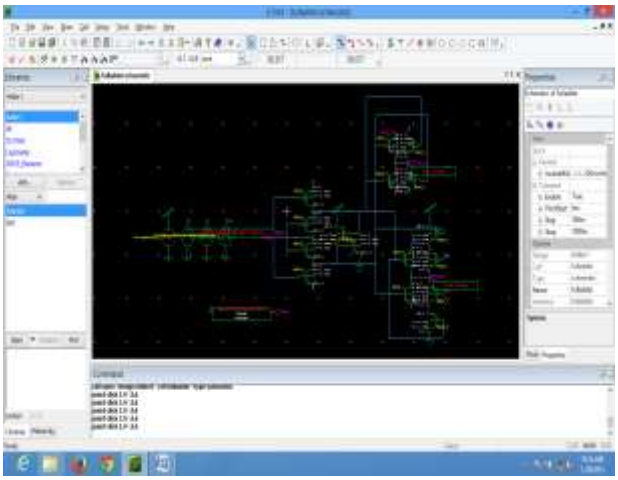

Fig.3. Hybrid-CMOS full adder design

The schematic design of the hybrid-CMOS full adder is shown in above fig.3. Here we can observe the 16 transistors which are useful to design hybrid-cmos full adder. For designing the circuits we are using the Tanner EDA tool. In tanner we have
S-Edit, W-Edit and T-Spice.

S-Edit means schematic editor, here we can draw the schematic diagram of the circuit.

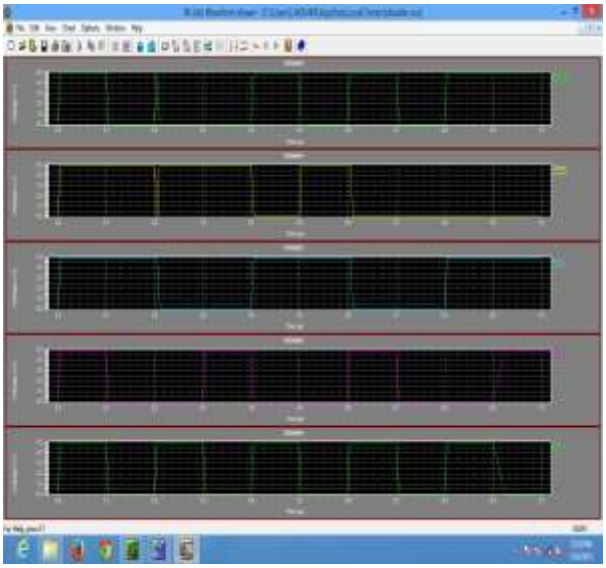

Fig.4. Waveforms for Hybrid-CMOS full adder

W-Edit means waveform editor, in this we can observe the waveforms of the circuit. In T-Spice we can calculate the power consumption values. Hybrid-CMOS full adder waveforms are shown in fig.4. The area, power consumption, delay and PDP (power delay product) of hybrid-cmos full adder is shown in table I.

TABLE I

PERFORMANCE ANALYSIS FOR HYBRID-CMOS CIRCUIT

S.No.	Factors	Hybrid-CMOS
1	Area(μm^2)	10
2	Power(μw)	$1.535569*10^{-1}$
3	Sum Delay(s)	$3.41685*10^{-8}$
4	Carry Delay(s)	$1.750151947*10^{-8}$
5	Sum PDP(pJ)	$5.246808938*10^{-3}$
6	Carry PDP(pJ)	$2.687479075*10^{-3}$

III. GDI BASED FULL ADDER

The Gate Diffusion Input (GDI) is a new method [5] for reducing power dissipation , propagation delay and area. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for the design of fast, low power circuits [8].This technique uses the reduced number of transistors as compared to CMOS and existing pass transistor logic techniques [13]-[15]. While improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library.

GDI is a new approach for designing the low power digital combinational circuit. The basic GDI cell is shown in fig.5. Basically this technique is two transistor implementation of the complex logic functions. This approach provides in cell swing restoration under certain operating condition.

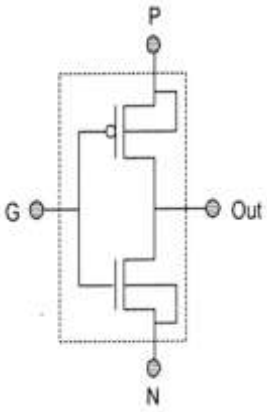

Fig.5. Basic GDI cell

It contains two transistors those are PMOS transistor and NMOS transistor. It is more fiexible than the CMOS design [6], because in CMOS design V_{dd} is connected to the source of PMOS and GND (ground) is connected to the source of NMOS. But in the GDI technique instead of V_{dd} and GND it uses two extra input pins. So totally we have three inputs in a GDI cell. Those inputs are G (common gate input of PMOS and NMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS). It is a simple cell like inverter whose PMOS and NMOS are connected to P and N respectively. This cell is a multifunctional device which gives different boolean functions with three inputs those are G, P&N.

The Full adder is designed by using GDI technique is represent in fig.6. This circuit contains only 10 transistors [16]-[17]. Here we are having three inputs those are A,B & Cin and two outputs SUM and CARRY (COUT). This technique leads to reduction in propagation delay, power consumption and area of digital circuits. It is obtained while having low complexity of logic design.

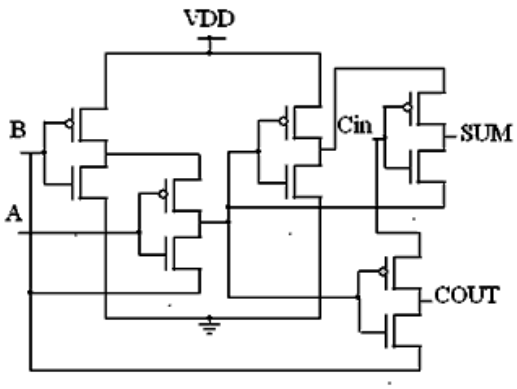

Fig.6. GDI based Full Adder

GDI has some advantages over CMOS those are low power circuit design, allows reducing power consumption,maintaining low complexity of logic design, reducing propagation delay, and reducing area of digital circuit.

B. Simulation results for GDI based full adder

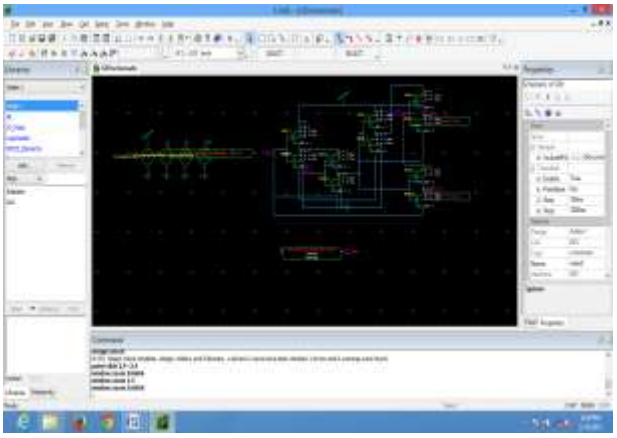

Fig.7. GDI based full adder design

The schematic design of GDI full adder is represent in above fig.7. Here we can observe the 10 transistors which are useful to design the GDI based full adder. Waveforms for the proposed GDI based full adder is shown in below fig.8. Here we can observe the waveforms for all combinations. When the inputs A=0,B=0,Cin=0 then the outputs SUM=0 & COUT=0. When A=0,B=0,Cin=1 then SUM=1,COUT=0. When A=0,B=1,Cin=0 then SUM=1 & COUT=0. When A=0,B=1,Cin=1 then SUM=0 & COUT=1. When A=1,B=0,Cin=0 then SUM=1 & COUT=0. When A=1,B=0,Cin=1 then SUM=0 & COUT=1. When A=1,B=1,Cin=0 then SUM=0 & COUT=1. When A=1,B=1,Cin=1 then SUM=1 & COUT=1.

The area, power consumption, delay and PDP of GDI based full adder is shown in table II. Comparison results for Hybrid - CMOS full adder and GDI based full adder is shown in table III. Here we are going to compare the power consumption in terms of micro watts (μw) , delay in terms of seconds (s), area in terms of micro meter square (μm^2) and power delay product (PDP) in terms of pico joules (pJ) .

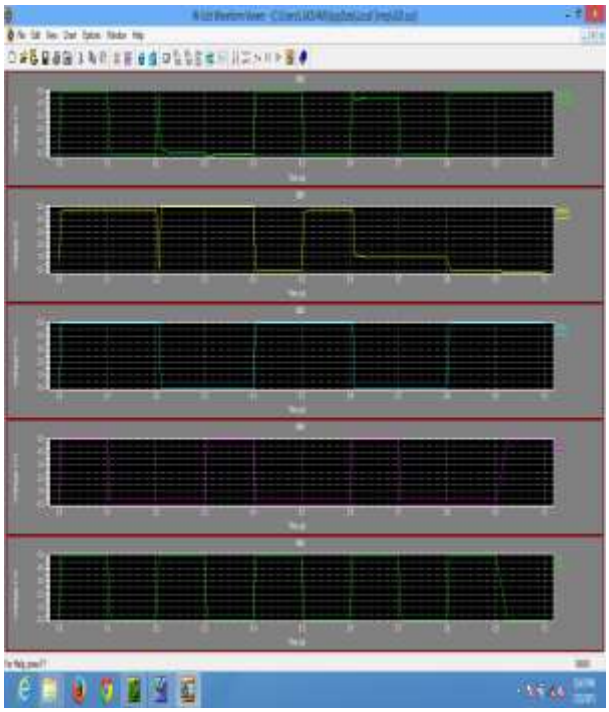

Fig.8. Waveforms for GDI based full adder

TABLE II

PERFORMANCE ANALYSIS FOR GDI BASED FULL ADDER CIRCUIT

S.No.	Factors	GDI Based Full Adder
1	Area(μm^2)	6.25
2	Power(μw)	$9.725216*10^{-3}$
3	Sum Delay(s)	$3.409156667*10^{-8}$
4	Carry Delay(s)	$1.75008844*10^{-8}$
5	Sum PDP(pJ)	$3.315478496*10^{-4}$
6	Carry PDP(pJ)	$1.70199881*10^{-4}$

TABLE III

COMPARISON OF HYBRID-CMOS AND GDI TECHNIQUES

Factors	Hybrid-CMOS Full Adder	GDI Based Full Adder
Area(μm^2)	10	6.25
Power(μw)	$1.535569*10^{-1}$	$9.725216*10^{-3}$
Sum Delay(s)	$3.41685*10^{-8}$	$3.409156667*10^{-8}$
Carry Delay(s)	$1.750151947*10^{-8}$	$1.75008844*10^{-8}$
Sum PDP(pJ)	$5.246808938*10^{-3}$	$3.315478496*10^{-4}$
Carry PDP(pJ)	$2.687479075*10^{-3}$	$1.70199881*10^{-4}$

The above circuits of full adder are simulated using the Tanner tools using TSMC018 CMOS process technology.

IV. CONCLUSION

As the core of an arithmetic circuit that is a key module in a large number of portable electronic systems, an high speed Full Adders are presented in this paper as a way to simplify the circuit architecture and hence improve the performance. For performance validation, Tanner simulations were conducted on Full Adders implemented with TSMC018 CMOS process technology in aspects of power consumption, delay and area. In contrast to other types of Full Adders GDI is superior to other ones and can be applied to design related adder based portable electronic products in practical applications in today's competitive markets.

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