

# Transformerless Inverter With Virtual Dc Bus Concept For Cost-Effective Grid-Connected Pv Power Systems

Dr.V.Balakrishna Reddy<sup>1</sup>, Mohd.Mastafa<sup>2</sup>,

<sup>1</sup>Professor,Dept of EEE,Vijaya Rural Engg College,Nizamabad,Telangana State,India.  
vbkreddy12@gmail.com

<sup>2</sup>Asst.Professor,Dept of EEE, ASTRA, Bandlaguda,Hyderabad,Telangana State,India.  
Mohdmustafa022@gmail.com

**ABSTRACT:***In order to eliminate the common-mode (CM) leakage current in the transformer less photovoltaic (PV) systems, the concept of the virtual dc bus is proposed in this paper. By connecting the grid neutral line directly to the negative pole of the dc bus, the stray capacitance between the PV panels and the ground is bypassed. As a result, the CM ground leakage current can be suppressed completely. Meanwhile, the virtual dc bus is created to provide the negative voltage level for the negative ac grid current generation. Consequently, the required dc bus voltage is still the same as that of the full-bridge inverter. Based on this concept, a novel transformer less inverter topology is derived, in which the virtual dc bus is realized with the switched capacitor technology. It consists of only five power switches, two capacitors, and a single filter inductor. Therefore, the power electronics cost can be curtailed. This advanced topology can be modulated with the uni polar sinusoidal pulse width modulation (SPWM) and the double frequency SPWM to reduce the output current ripple. As a result, a smaller filter inductor can be used to reduce the size and magnetic losses.*

Keywords: PV System,Transformerless Inverter,SPWM,Virtual DC bus concept,Operation Modes of the circuit, Hardware Theory

## 1. Introduction

The distributed photovoltaic (PV) power generation systems have received increasing popularity in both the commercial and residential areas. In most occasions, the inverters are used to feed the PV power into the utility grid. It is important for the PV inverter to be of high efficiency, due to the relatively high price of the PV panels. Small size is also strongly desired for the low-power and single-phase systems, especially when the inverters are installed indoor.

### 1.1 MODULE DESCRIPTION

#### PV System

The word “photovoltaic” combines two terms – “photo” means light and “voltaic” means voltage. A photovoltaic system in this discussion uses photovoltaic cells to directly convert sunlight into electricity. Photovoltaic power generation employs solar panels composed of a number of solar cells containing a photovoltaic material. Materials presently used for photovoltaics include mono crystalline silicon, polycrystalline silicon, amorphous silicon, cadmium telluride, and copper indium gallium selenide/sulfide. Due to the increased demand for renewable energy sources, the manufacturing of solar cells and photovoltaic arrays has advanced considerably in recent years. Solar photovoltaics is a sustainable energy source where 100 countries are utilizing it. Solar photovoltaics is now, after hydro and wind power, the third most important renewable energy source in terms of globally installed capacity. Installations may be ground-mounted or built into the roof or walls of a building. (either building-integrated photovoltaics or simply rooftop).

#### Transformerless Inverter

The largest recent shift in inverter technology is the availability of transformer less inverters in the United States. They have long been popular in Europe, but now most inverter manufacturers have added a transformer less option to their existing inverter line. Without a heavy transformer, they weigh

about 50% to 70% less than a transformer-based inverter of similar output, and the size of the inverter housing can be (but isn't always) reduced. Inverter efficiency is also increased there are no longer losses associated with having a transformer to step up the voltage. And because the transformer (which is comprised of copper windings on an iron or steel core) is eliminated, they are less expensive to produce. The majority of inverter manufacturers are now including a transformer less inverter line. Exeltech, Ingeteam, and Solar Edge are few examples. They require the DC wiring to be ungrounded. Because neither the positive nor negative conductor is connected to ground, they must meet more NEC requirements, including the use of PV wire (a double-insulated single conductor cable having added sunlight and mechanical protection) for exposed wires (i.e., module interconnects and exposed home run wiring). Over current protection and disconnect devices are required on both the positive and negative conductors, since they are both ungrounded. Arrays that require the positive conductor be grounded (those using Sun Power modules, for example) are not recommended for use with transformer less inverters, because the array must be ungrounded.

#### 1.2 SPWM

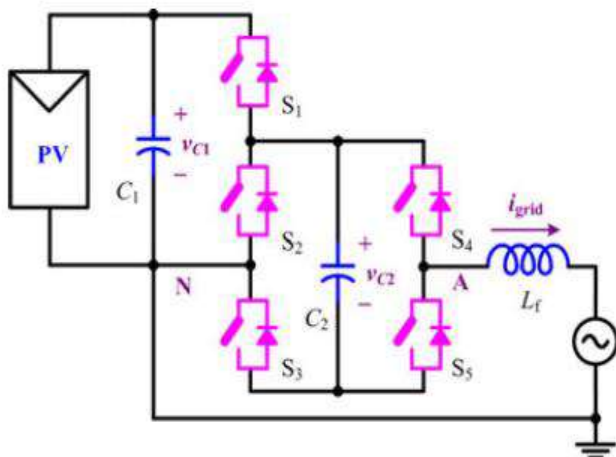
SPWM technique is based on classical SPWM technique with carriers and reference sine waveform. Only difference between them is, in digital SPWM a sine table consisting of values of sine waveform sampled at certain frequency is used. As result reference wave form in digital SPWM represents a sample and hold wave form of sine wave form. A simple comparator with a sawtooth carrier can turn a sinusoidal command into a pulse-width modulated output. In general, the larger the command signal, the wider the pulse as shown in Fig. Output stays high as long as the command is greater than the carrier. Pulse-width modulation (PWM), as it applies to motor control, is a way of delivering energy through

a succession of pulses rather than a continuously varying (analog) signal. By increasing or decreasing pulse width, the controller regulates energy flow to the motor shaft. The motor's own inductance acts like a filter, storing energy during the "on" cycle while releasing it at a rate corresponding to the input or reference signal. In other words, energy flows into the load not so much the switching frequency, but at the reference frequency. The energy of each push is stored in the inertia of the heavy platform, which accelerates gradually with harder, more frequent, or longer-lasting pushes. The riders receive the kinetic energy in a very different manner than how it's applied.

### Virtual DC bus Concept

The positive pole of the virtual bus is connected to the ground point N, so that the voltage at the midpoint C is either zero or  $-V_{dc}$ . The dotted line in the figure indicates that this connection may be realized directly by a wire or indirectly by a power switch. With points B and C joined together by a smart selecting switch, the voltage at point A can be of three different voltage levels, namely  $+V_{dc}$ , zero, and  $-V_{dc}$ . Since the CM current is eliminated naturally by the structure of the circuit, there is not any limitation on the modulation strategy, which means that the advanced modulation technologies such as the unipolar SPWM or the double-frequency SPWM can be used to satisfy various PV applications.

### Module Diagram



## 1.3 TECHNIQUES USED

Grid Tie Inverter: Double frequency SPWM

## 2 TECHNIQUES DESCRIPTION

### Grid Tie Inverter

Inverters take DC power and invert it to AC power so it can be fed into the electric utility company grid. The grid tie inverter must synchronize its frequency with that of the grid (e.g. 50 or 60 Hz) using a local oscillator and limit the voltage to no higher than the grid voltage. A high-quality modern GTI has a fixed unity power factor, which means its output voltage and current are perfectly lined up, and its phase angle is within 1 degree of the AC power grid. The inverter has an on-board computer which will sense the current AC grid waveform, and output a voltage to correspond with the grid. However, supplying reactive power to the grid might be necessary to keep the voltage in the local grid inside allowed limitations. Otherwise, in a grid segment with considerable power from renewable sources voltage levels might rise too much at times of high production, i.e. around noon. Grid-tie inverters are also designed to quickly disconnect from the grid if the utility grid

goes down. This is an NEC requirement that ensures that in the event of a blackout, the grid tie inverter will shut down to prevent the energy it transfers from harming any line workers who are sent to fix the power grid. Properly configured, a grid tie inverter enables a home owner to use an alternative power generation system like solar or wind power without extensive rewiring and without batteries. If the alternative power being produced is insufficient, the deficit will be sourced from the electricity grid.

## 2 MODULATION STRATEGIES: DOUBLE FREQUENCY SPWM Technique

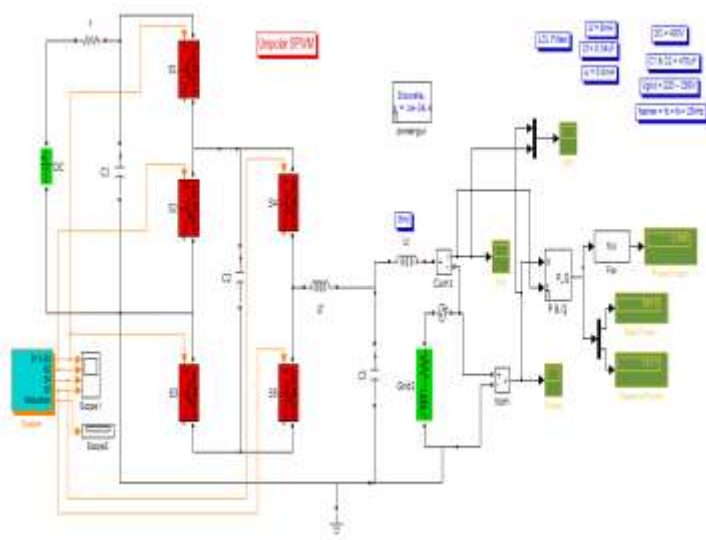
The proposed topology can also work with double-frequency SPWM to achieve a higher equivalent switching frequency. In the double-frequency SPWM, the five power switches are separated into two parts, and are modulated with two inverse sinusoidal waves respectively.  $S_1$ ,  $S_2$ , and  $S_3$  are modulated with  $u_{g1}$ , while  $S_4$  and  $S_5$  are modulated with  $u_{g2}$ . During the positive half grid cycle, the circuit rotates in the sequence of "state 4 – state 1 – state 2 – state 1," and the output voltage  $v_{AN}$  varies between  $+V_{dc}$  and the zero with twice of the carrier frequency. During the negative half grid cycle, the circuit rotates in the sequence of "state 4 – state 3 – state 2 – state 3," and the output voltage  $v_{AN}$  varies between  $-V_{dc}$  and zero.

The aforementioned two modulation strategies both have their own advantages. The double-frequency SPWM can provide a higher equivalent switching frequency so that the size and weight of the filter inductor can be reduced. On the other hand, the unipolar SPWM can guarantee that the virtual dc bus  $C_2$  is charged by the real bus every switching cycle, so that the current stress on  $S_1$  and  $S_3$  caused by the operation of the switched capacitor can be reduced. In this paper, the unipolar SPWM is chosen as an example for the performance evaluation and experimental verification. For all of the four operation states, there is no limitation on the direction of the output current  $i_{grid}$ , since the power switches with antiparallel diodes can achieve bidirectional current flow. Therefore, the proposed topology has the capability of feeding reactive power into the grid to help support the stability of the power system.

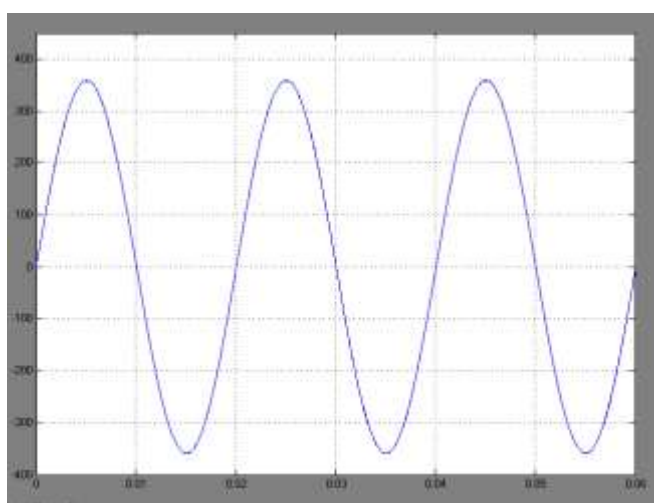
The proposed topology is also immune against transient overvoltage of the grid. During the mains positive voltage spikes, the voltage at point A is clamped at  $V_{dc}$  by  $C_1$  and the antiparallel diodes of  $S_1$  and  $S_4$ . Similarly, during the negative voltage spikes, the voltage at point A is clamped at  $-V_{dc}$  by  $C_2$  and the antiparallel diodes of  $S_2$  and  $S_5$ . Therefore, the mains transient over voltage does not pose a safety threat for the inverter.

## 3 Simulation Design without Modulation

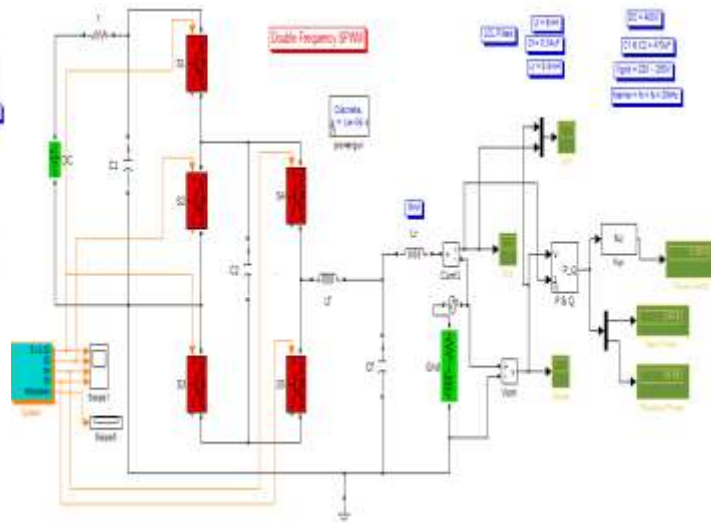
A simulation design modulation technique as shown in Fig.1 & Fig.4 is implemented in MATLAB SIMULINK with the help of pulse generators where the Unipolar & Double polar frequency is varied (Fig.2 & Fig.5). A modified circuit of the system ie a Unipolar and Double polar frequency Grid Tie inverter is also designed which is shown in Fig 1 & 7. The THD analysis is also compared for all the three simulations which is shown below in Fig 3 & 6



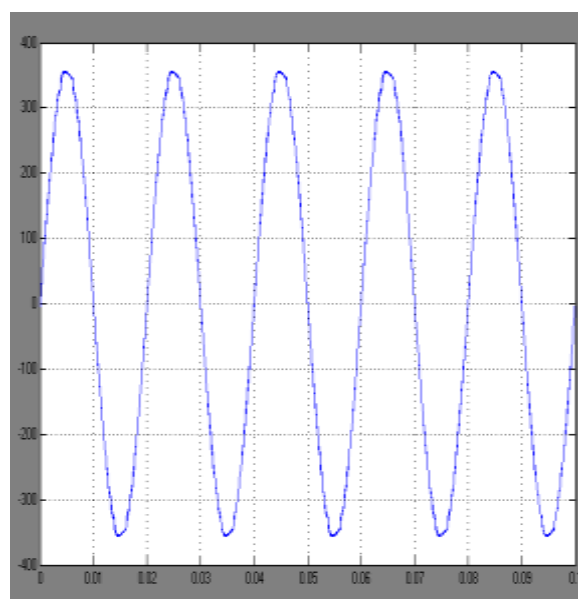
**Fig. 1. Proposed Unipolar Frequency Grid Tie Inverter**



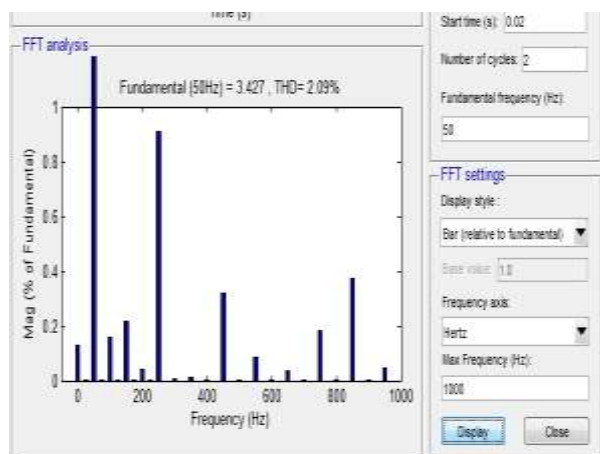
**Fig. 2. Output Voltage Waveform**



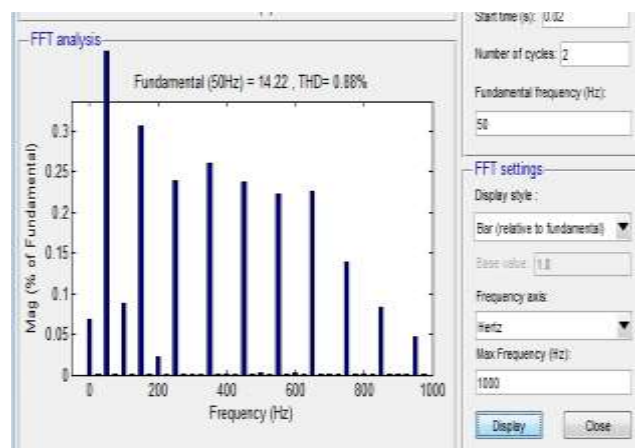
**Fig. 4 Proposed Double SPWM GTI**



**Fig. 5. O/P Double SPWM Voltage Waveform**



**Fig. 3. O/P Current Distortion**



**Fig. 6. O/P Current Distortion**

**4.4 Modulation Technique  
VIRTUAL DC BUS CONCEPT**



The concept of the virtual dc bus is depicted. By connecting the grid neutral line directly to the negative pole of the PV panel, the voltage across the parasitic capacitance  $C_{PV}$  is clamped to zero. This prevents any leakage current flowing through it. With respect to the ground point N, the voltage at midpoint B is either zero or  $+V_{dc}$ , according to the state of the switch bridge.

The purpose of introducing the virtual dc bus is to generate the negative output voltage, which is necessary for the operation of the inverter. If a proper method is designed to transfer the energy between the real bus and the virtual bus, the voltage across the virtual bus can be kept the same as the real one.

The positive pole of the virtual bus is connected to the ground point N, so that the voltage at the midpoint C is either zero or  $-V_{dc}$ . The dotted line in the figure indicates that this connection may be realized directly by a wire or indirectly by a power switch. With points B and C joined together by a smart selecting switch, the voltage at point A can be of three different voltage levels, namely  $+V_{dc}$ , zero, and  $-V_{dc}$ . Since the CM current is eliminated naturally by the structure of the circuit, there is not any limitation on the modulation strategy, which means that the advanced modulation technologies such as the unipolar SPWM or the double-frequency SPWM can be used to satisfy various PV applications.

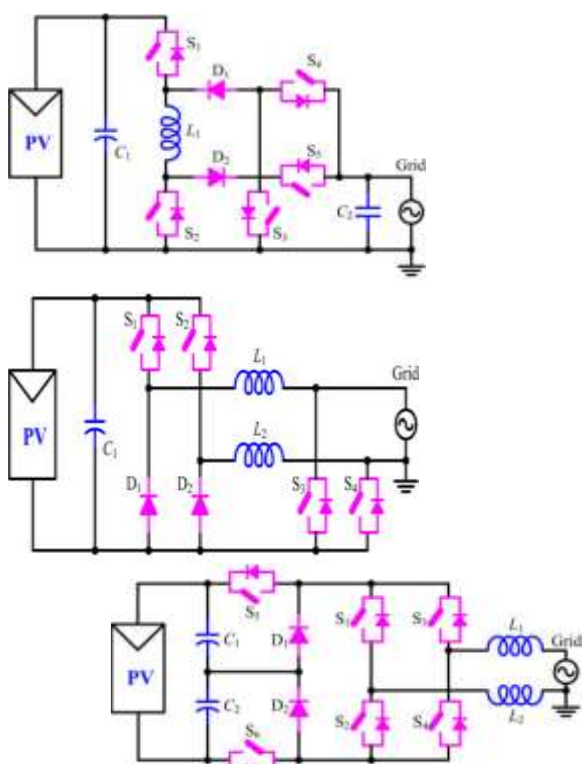


Fig 7

### DERIVED TOPOLOGY AND MODULATION STRATEGY

Based on the virtual dc bus concept, a novel inverter topology is derived as an example to show the clear advantages of the proposed methodology. It consists of five power switches  $S_1$ – $S_5$  and only one single filter inductor  $L_f$ . The PV panels and capacitor  $C_1$  form the real dc bus while the virtual dc bus is provided by  $C_2$ . With the switched capacitor technology,  $C_2$  is charged by the real dc bus through  $S_1$  and  $S_3$  to maintain a constant voltage. This topology can be modulated with the unipolar SPWM and double-frequency SPWM. The detailed analysis is introduced as follows.

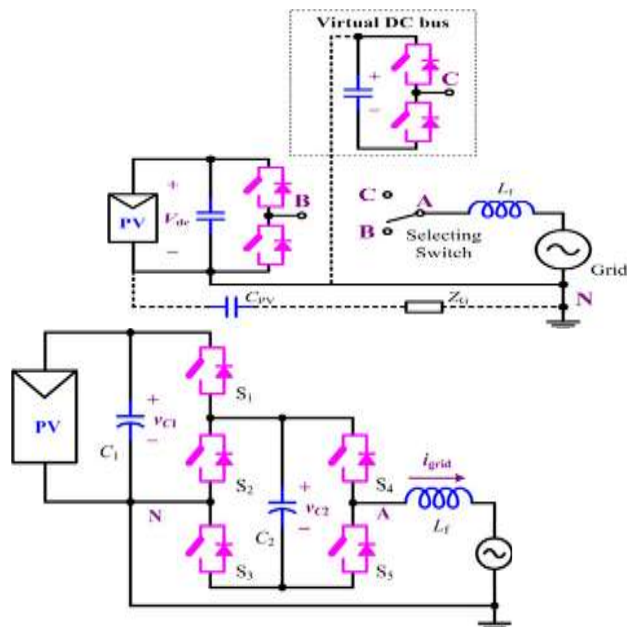


Fig 8

### Unipolar SPWM

The waveform for the unipolar SPWM of the proposed inverter is displayed. The gate drive signals for the power switches are generated according to the relative value of the modulation wave  $u_g$  and the carrier wave  $u_c$ . During the positive half grid cycle,  $u_g > 0$ .  $S_1$  and  $S_3$  are turned ON and  $S_2$  is turned OFF, while  $S_4$  and  $S_5$  commute complementally with the carrier frequency. The capacitors  $C_1$  and  $C_2$  are in parallel and the circuit rotates between states 1 and 2.

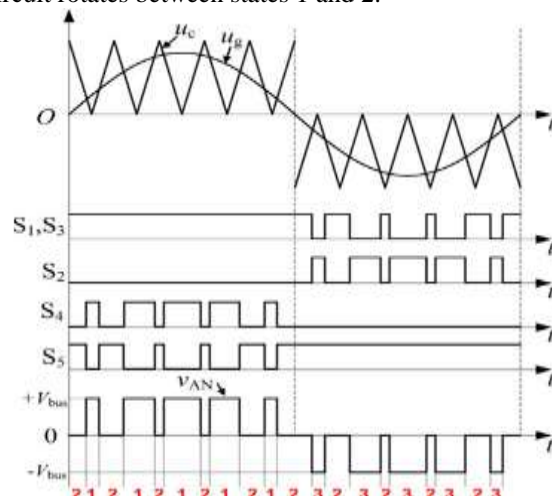


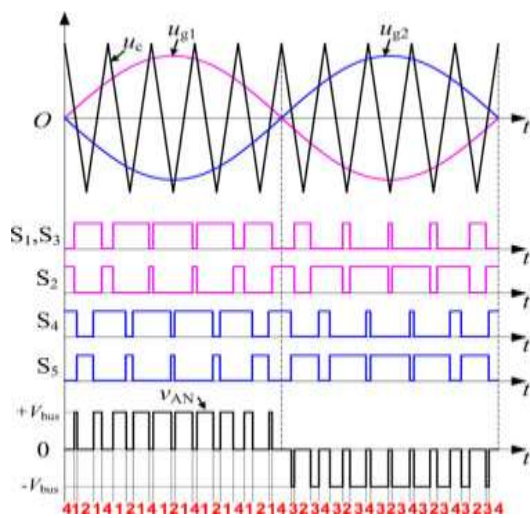
Fig 9. Unipolar Waveform

During the negative half cycle,  $u_g < 0$ .  $S_5$  is turned ON and  $S_4$  is turned OFF.  $S_1$  and  $S_3$  commute with the carrier frequency synchronously and  $S_2$  commutates in complement to them. The circuit rotates between states 3 and 2. At state 3,  $S_1$  and  $S_3$  are turned OFF while  $S_2$  is turned ON. The negative voltage is generated by the virtual dc bus  $C_2$  and the inverter output is at negative voltage level. At state 2,  $S_1$  and  $S_3$  are turned ON while  $S_2$  is turned OFF. The inverter output voltage  $v_{AN}$  equals zero; meanwhile,  $C_2$  is charged by the dc bus through  $S_1$  and  $S_3$ .

### Double-Frequency SPWM

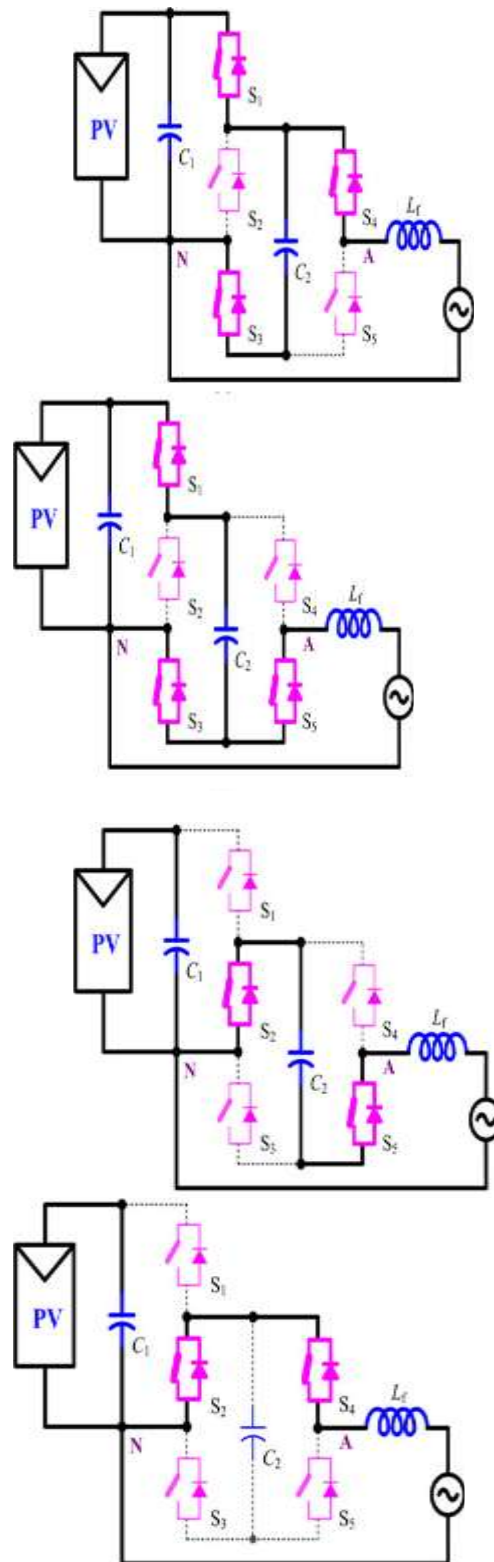
The proposed topology can also work with double-frequency SPWM to achieve a higher equivalent switching frequency, as shown in Fig. 9. In the double-frequency SPWM, the five power switches are separated into two parts, and are modulated with two inverse sinusoidal waves respectively.  $S_1$ ,  $S_2$ , and  $S_3$  are modulated with  $u_{g1}$ , while  $S_4$  and  $S_5$  are

modulated with  $u_{g2}$ . During the positive half grid cycle, the circuit rotates in the sequence of “state 4 – state 1 – state 2 – state 1,” and the output voltage  $v_{AN}$  varies between  $+V_{dc}$  and the zero with twice of the carrier frequency. During the negative half grid cycle, the circuit rotates in the sequence of “state 4 – state 3 – state 2 –state 3,” and the output voltage  $v_{AN}$  varies between  $-V_{dc}$  and zero.



**Fig 10. Double Frequency SPWM**

The aforementioned two modulation strategies both have their own advantages. The double-frequency SPWM can provide a higher equivalent switching frequency so that the size and weight of the filter inductor can be reduced. On the other hand, the unipolar SPWM can guarantee that the virtual dc bus  $C_2$  is charged by the real bus every switching cycle, so that the current stress on  $S_1$  and  $S_3$  caused by the operation of the switched capacitor can be reduced. In this paper, the unipolar SPWM is chosen as an example for the performance evaluation and experimental verification. For all of the four operation states, there is no limitation on the direction of the output current  $i_{grid}$ , since the power switches with antiparallel diodes can achieve bidirectional current flow. Therefore, the proposed topology has the capability of feeding reactive power into the grid to help support the stability of the power system.

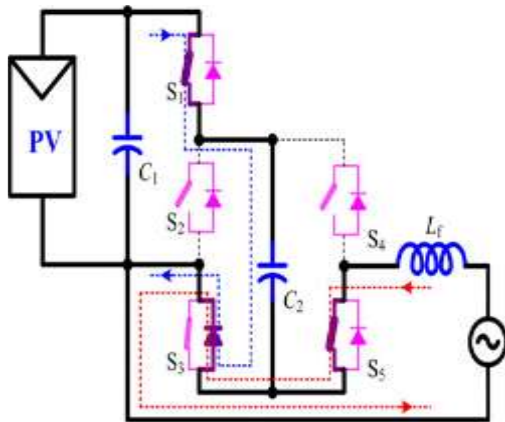


**Fig11**

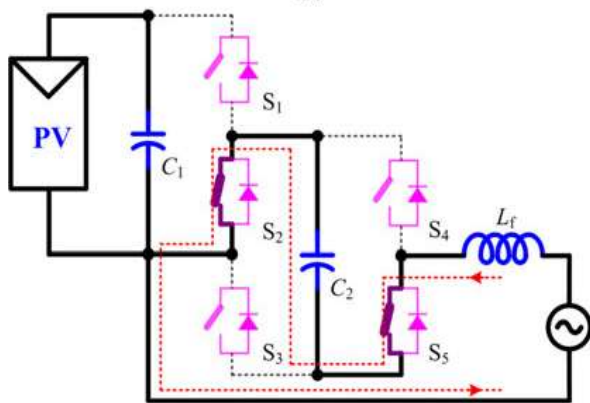
The proposed topology is also immune against transient overvoltage of the grid. During the mains positive voltage spikes, the voltage at point A is clamped at  $V_{dc}$  by  $C_1$  and the antiparallel diodes of  $S_1$  and  $S_4$ . Similarly, during the negative voltage spikes, the voltage at point A is clamped at  $-V_{dc}$  by  $C_2$  and the antiparallel diodes of  $S_2$  and  $S_5$ . Therefore, the mains transient overvoltage does not pose a safety threat for the inverter.

**Switching Losses**

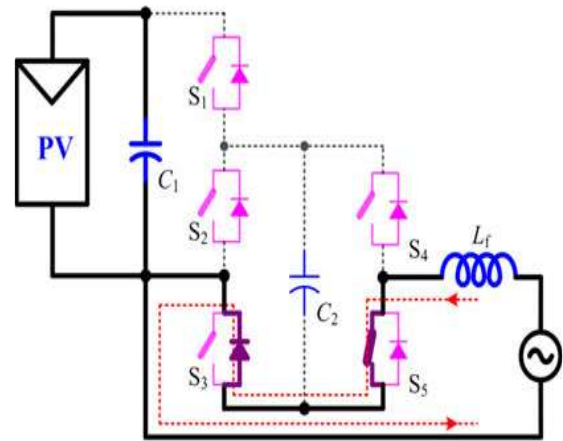
During the positive half cycle, only two switches, namely  $S_4$  and  $S_5$ , commute at the carrier frequency, so the switching losses are the same as the traditional full-bridge inverter. During the negative half cycle,  $S_1$ ,  $S_2$ , and  $S_3$  commute at the carrier frequency. Although the number of high-frequency switches increases to 3, it can be seen from the following analysis that the switching losses almost keep the same.



For convenience of description, the power transistor and the antiparallel diode for the switch  $S_n$  is denoted as  $T_n$  and  $D_n$  respectively, where  $n = 1, 2, \dots, 5$ . At state 2,  $T_1$ ,  $T_3$ , and  $T_5$  are turned ON, while the current actually flows through  $T_1$ ,  $D_3$ , and  $T_5$ . When the circuit switches from state 2 to state 3,  $T_1$  and  $T_3$  are turned OFF first before  $T_2$  is turned ON due to the effect of the dead time. As a result, there will be a transition state between the two states. During this transition state, the inductor  $L_f$  freewheels through  $D_3$ , so the voltage across  $T_1$  and  $T_3$  may not rise immediately after turned OFF, so that the switching losses can be neglected. When the dead time is passed,  $T_2$  is turned ON. The inductor current is forced to commute from  $D_3$  to  $T_2$ , and the circuit changes into state 3.



When the circuit rotates from state 3 to state 2, it also enters the transition state first. Because of the dead time,  $T_2$  is turned OFF while  $T_1$  and  $T_3$  are not turned ON yet, and the inductor current is forced to commute from  $T_2$  to  $D_3$ . After  $D_3$  is conducting, the voltage across



$S_1$  and  $S_3$  reduces to zero approximately. Therefore, when  $T_1$  and  $T_3$  are turned ON after the transition state, they will not suffer significant switching losses. In summary, only  $T_2$  and  $D_3$  operate in the forced commutation mode during the negative half cycle, and the voltage and current commutated are  $V_{dc}$  and  $i_{grid}$ , respectively. Therefore, the operation of the switched capacitor does not cause the increase in switching losses. Similar analysis can be performed on the H5 circuit. It can be seen that the number of forced commutation for the transistors is doubled for the H5 circuit, while the commutation voltage reduces to  $V_{dc}/2$ , so the resultant switching losses can be assumed to be at the same level.

### Conduction Losses in Switched Capacitors

The operation of the switched capacitor also increases the conduction losses in the capacitor due to its equivalent series resistance (ESR). The ESR losses are evaluated to give further guidelines on the capacitor design. For the proposed topology, the conduction losses in ESR can be divided into two parts. The first part is caused by the ripple current which is intrinsic to all voltage source inverters, including the traditional full-bridge and half-bridge circuits and the newly developed topologies such as H5, HERIC, etc. The second part is caused by the inrush current during the charging of the switched capacitors. These additional losses only occur at state 2 in the negative half cycle.

### Losses in the Filter Inductor

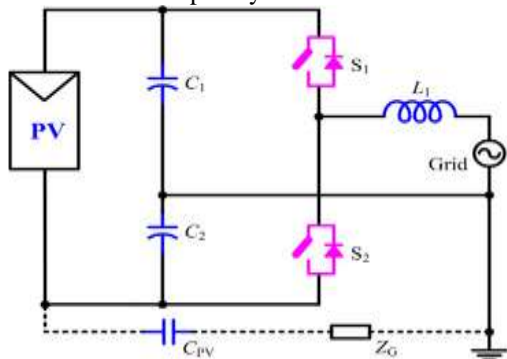
Under the same switching frequency, the output voltage waveforms of the proposed circuit and the H5 circuit are identical to each other. This results in similar output current ripple and magnetic losses, if the same filter inductor configurations are used. Nevertheless, the H5 circuit has to employ two inductors with separated iron cores, while the proposed circuit only needs one. This may lead to a reduction in the size of the iron core, although the total inductor value is still the same.

### CM Current Elimination

As explained previously, the key point for the full-bridge based solutions, including H5 and HERIC, is to insert extra switches into the traditional full-bridge inverter to disconnect the line side with the dc side, when the inverter output voltage is at zero voltage level. Unfortunately, this disconnection is incomplete because of the parasitic capacitance on the power switches. As a result, high-frequency CM current may still flow through these capacitors. Therefore, it is necessary to add extra filters into these topologies to absorb this CM current. As for the proposed topology, the stray



capacitance between the PV panels and the ground is directly bypassed. Due to the configuration of the virtual dc bus, the CM current is eliminated completely.



In conclusion, the conduction and switching losses in the power devices of the proposed topology are quite similar to those of the H5 circuit. The main drawback is that larger capacitors are needed to reduce the ESR losses in the capacitor and ensure their life time. This issue can be alleviated by adding a thin film capacitor in parallel to the aluminum electrolyte one to absorb the high-frequency pulsating current. Fortunately, the clear advantage of the proposed topology is that it has better performance in eliminating the CM current. The solution with virtual dc bus concept provides a new idea for developing the transformerless inverter for the PV applications.

## Conclusion:

### EXPECTED INPUT AND EXPECTED OUTPUT

Given I/P & Expected O/P

Simulation

- Vdc=400V
- Vac=(230V)
- THD< 1% under SPWM Technique

### Hardware

- Vdc=12-17V from solar panel
- Vac=230V using a 5W lamp load

### Advantages

- High efficiency and Unity Power Factor (UPF)
- Reduced size and Low cost
- Common-Mode (CM) ground leakage current is reduced to zero
- Much safety
- Low O/P Current harmonics and Less EM

**Applications:** Grid-tie inverters ,Stand-alone Inverters ,UPS

**FUTURE SCOPE:** The system can be extended to connecting more hybrid sources. And we can implement the grid tie inverter as multi level inverter so that we can improve the circuit efficiency with reducing the distortion. As we use more hybrid sources the voltage level will be improved. As the inverter's name define what it is. So we can imply in grid, home power supply, in industries for low load application such as lighting and we extend to desire of consumer in future

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## Author Profile



**Dr V. Balakrishna Reddy**, received B.Tech ,M.Tech from JNTUH. In 2004 and 2009 respectively and Ph.D Degree from SVU, Uttara Pradesh in 2004. Now he is working as *Professor*, Department of EEE, Vijay Rural Engg College, Nizambad, Telangana state, India., He is interest in research of power system and power electronics . His mail.I.D is - vbkreddy12@gmail.com