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Implementation of High speed and Low power 6T SRAM cell using FinFET at 22nm technology

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Abstract

Static Random Access Memory (SRAM) comprises considerable proportion of total area and total power for almost all VLSI chips as cache memory for the System on Chip (SOC) and it is considered to be more intense in upcoming time in both handy devices and high-performance processors. Static Random Access Memory (SRAM) plays a most significant role in the microprocessor world, but as the technology is scaled down in nanometers, leakage current, leakage power and delay are the most common problems for SRAM cell which is basically designed in low power application. By using low-power FinFET based SRAM cell, we can accomplish higher steadfastness and enhanced battery life for handy devices. Our objective of this work is to improve delay and power consumption in proposed nanoscale 6T FinFET SRAM cell structure. The total leakage of FinFET SRAM cell is reduced by 23% after applying self controllable voltage level technique. The power consumption and write delay as well as read delay of proposed 6T FinFET based SRAM cell structure improves on CADENCE VIRTUOSO tool at 22nm technology scale.

Keywords: FinFET, 6T SRAM cell design, Power consumption, Low power.

I. INTRODUCTION

Static random-access memory (SRAM) constitutes an expansive rate of Mobile zone to framework on chip (SOC) plans. Because of secondary number for transistors to a absolute SRAM Mobile [1]. Thus, SRAM Mobile commonly uses base measure transistor in place should understand higher thickness. Metal-oxide semiconductor field-effect-transistor (MOSFET) innovation scaling need been used to decrease size from claiming SRAM Mobile in those previous three decades for those diminishment from claiming entryway length. Downscaling enhances SRAM execution for higher transistor exchanging speed furthermore lessens force utilization. However, similarly as those engineering scaled Past 22 nm, traditional planar MOSFETs start on neglect because of the edge voltage variety also short channel impact.

Read/Write memory or random access memory hold instructions for the time being. Memory array storage is required for central processing unit to process the function and permit alteration of data bits. The SRAM cell comprises of a latch, it does not require any refresh process, as the cell transistor holds the data as long as the power supply is not disconnect. Large sum of power consumption in handy electronics devices is an concern of serious distress. Supplementary packaging and cooling fans becomes compulsory to minimise the heat dissipation associated with high power consumption, this results in increment of overall chip area [2]. Due to this excessive heat dissipation on the chip, battery life also reduces. Static power dissipation caused due to standby leakage currents, is a vital factor of total power dissipation.

II. FinFET

FinFET may be an gadget which bring “fin” comparative of the fish that is it need hotspot also channel as a balance with respect to whichever Side of the entryway what's more it is show up likewise a “fin” . It will be principal. Presented Eventually Tom's perusing berkeley scientists

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about college about. California also portrayed the FinFET as a Non-Planer free entryway transistor fabricated for an SOI (Silicon on insulator) in view of absolute entryway structure.

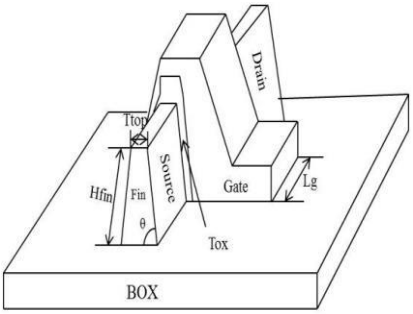

Figure 1: Basic design of FinFET

As we stated before that FinFET has "fin" like structure is clearly shown in the above figure. Here H_{fin} is the height of the Silicon fin, L_g is the physical Gate Length of the FinFET, T_{top} is the thickness of the silicon fin and T_{ox} is the thickness of Gate Oxide. In single gate devices as the channel length reach a specific value and after that if we reduce the channel length the short channel effect come into play and the performance of the device start degrading due to the short channel effect. This is the major drawback of the single gate devices. To overcome the Short Channel Effect First Double Gate FinFET is introduce which successful reduce the Short Channel Effect but it required double power supply for both the Gate. Than Short Gate FinFET is introduce which show great reduction on Short Channel Effect and also require single power supply.

III. CONVENTIONAL 6T SRAM CELL

The conventional 6T SRAM cell consists of two cross coupled inverters and two access transistors shown in Fig 1; these cross coupled inverters are called as a latch. The two cross coupled inverters have four transistors (M3, M4, M5, and M6); each bit in an SRAM is stored on four transistors. The drain terminal of access transistors (M1 and M2) are connected to the latch inputs and source terminals are connected to the bit line (BL) and bit line bar (BLB) . When the word line is low (WL = 0), access transistors are OFF and bit lines are isolated from latch. In this state, the latch can hold the bit as long as the voltages remain at and . When the word line is high (WL = 1), access transistors are ON and bit lines (BL and BLB) are connected to latch, these bit lines (BL and BLB) are used to transfer the data for both write and read operations.

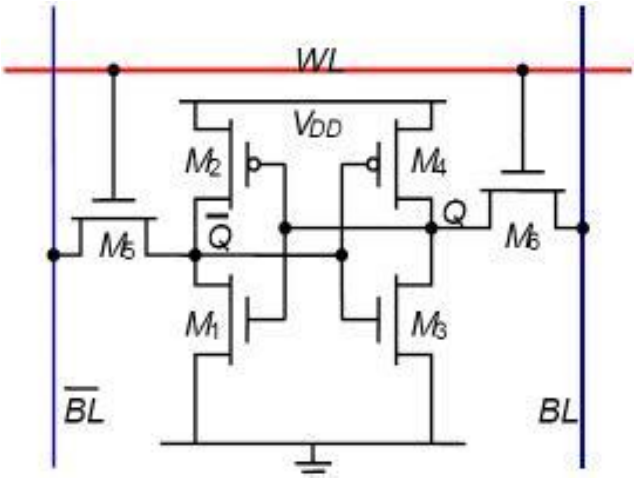

Figure 2: The Conventional 6T SRAM Cell

Write Operation:

To perform either of the operations the access transistors (M1 and M2) must be activated first. For this, we must pull the word line high (WL='1') to activate the access transistors (M1 and M2). Now we can perform the write operation. The required data to be written is given to bit line (BL) and its complement is applied on bit line bar (BLB). That means if we want to write '1' to SRAM cell, we must provide '1' to bit line (BL) and '0' to bit line bar (BLB). This would make the cell to change its state accordingly. When state of latch is changed the word line is deactivated (WL='0') and thus the required data is written to the cell.

Read Operation:

Similarly, to read the data from the SRAM cell, the word line is first asserted to high (WL='1') which activates the access transistors (M1 and M2) to access the latch. Now to perform read operation, both the bit lines are pre-charged to '1'. Now one of the bit line would remain pre-charged and the bit line would be discharged to ground, depending on the state of the latch. Thus if bit line (BL) remains charged, the bit line bar (BLB) must be discharged or vice versa as the case may. At this stage both the bit lines are applied at the inputs of sense amplifier which finally gives the information of the stored bit by amplifying the data to a significant level.

IV. PROPOSED SRAM USING FinFET

The FinFET SRAM cell structure is superior choice due to the self- alignment of both gates and the fabrication compatibility with the existing standard CMOS fabrication technology [3]. It also consists of WL to enable access N type FinFET transistors. Two FinFET inverters are connected

back to back same as the bulk CMOS SRAM. FinFET reduces the SCE, leakage c urrent and leakage power, but delay in the 6T SRAM is increased by using FinFET to some extent during the operation[4]. The structure of 6T SRAM designed by FinFET is shown in Fig 3.

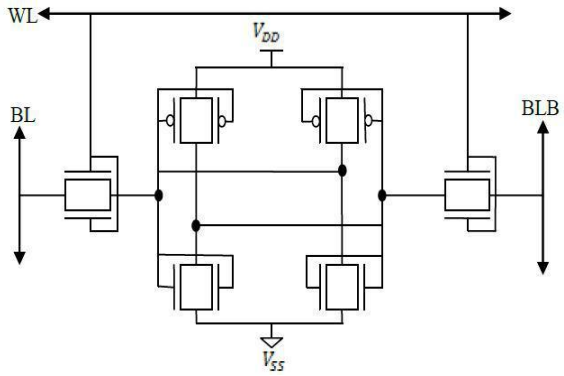

Figure 3: FinFET based 6T SRAM cell

To hold single bit data simply we are using SRAM and for large applications we can use array of SRAM. The noise immunity, leakage power, leakage current is the main issue in SRAM so to avoid this FinFET based SRAM is used. FinFET based SRAM has same working as conventional based SRAM and the power dissipation, leakage is less in FinFET based SRAM.

In the proposed work, self-controllable voltage technique is applied on the FinFET SRAM cell to further reduce the leakage in the cell. A circuit containing two NMOS transistors connected in series and a PMOS connected parallel to those two NMOS transistors, is connected below which provides ground during active mode and an increased ground voltage (virtual ground) during standby mode.

Another circuit consisting of two PMOS transistors connected in series and a NMOS connected parallel to those two PMOS transistors, is connected above the SRAM cell which provides a full supply voltage in active mode and voltage level is reduced at standby mode. Both circuits connected at upper end and lower end of the FinFET SRAM are termed as USVL (upper SVL) and LSVL (lower SVL) respectively which together provides the reduced leakage to the FinFET SRAM cell. The operation of SVL can be easily understood using CMOS inverter as shown in Fig 4. When "clk=1" and "clkbar =1" Thus, the USVL and LSVL circuits respectively generate a slightly lower supply voltage and a relatively higher "ground-level" therefore the leakage in OFF transistor reduces. Similarly, this technique reduces the leakage current in the FinFET SRAM cell.

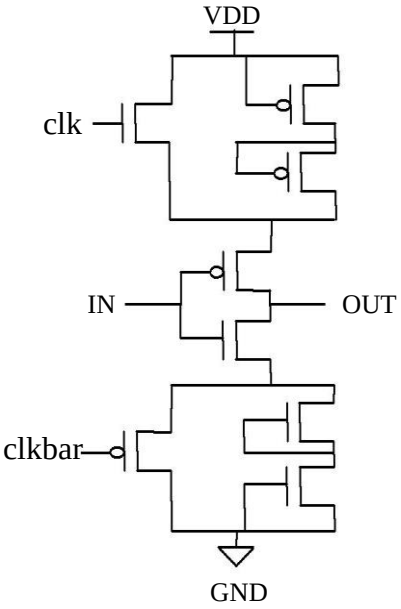

Figure 4: Schematic of inverter implementation of SVL technique

Leakage Current

Sub-threshold leakage is the drain source current of the transistor when the VGS < VTH [5]. In the weak inversion (or sub-threshold) regime, the drain current depends exponentially on the gate-source voltage given by equation (1).

$$I_d \ \alpha \ \exp\left(\frac{Vgs}{Vt}\right) \qquad (1)$$

Where Vt = kT/q

Vt indicates threshold voltage, 'k' indicates the Boltzmann constant, T indicates the absolute temperature, and q indicates the charge of electron. Leakage current is the flow of electrons through the gate that flows when the transistor is in OFF state.

Write Delay

For a write operation, the write delay is defined as the time between the activation 50% of WL to when Qbar is 90% of its full swing [6]. Propagation delay of inv2 and inv l determines the write delay of the cell. Data to be written into the cell is applied to the bit lines (BL and BLB). The access transistors are activated by applying the signal voltage to the gates of access transistors or we can say by applying logic "1" to word line WL. In write operation for the SRAM cell, a reasonable write-trip point is equally important [7] to guarantee the write ability of the cell without the expenditure of too much power in shifting down the bit-line voltage to 0 V. The write-trip point defines the maximum voltage on the bit-line, essential to flip the cell content.

V. SIMULATION RESULTS

A.6T SRAM cell Structure:

The routine six-transistor (6T) SRAM will be fabricated up of two cross coupled. Inverters also two get transistors, interfacing the Mobile of the bit lines. The inverters make up the stockpiling component and the right transistors need aid used to convey with the outside. The cell will be symmetrical also need a generally vast range.

No uncommon methodology steps need aid required and it is fully perfect with standard CMOS procedures.

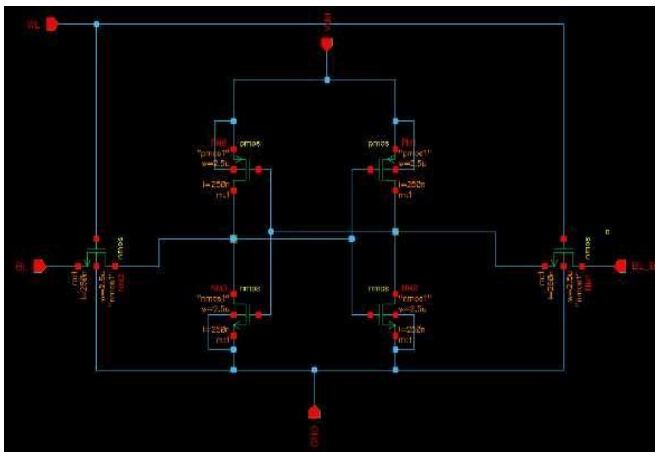

Figure 5: 6T SRAM cell design.

B. Read Operation:

The 6T SRAM cell need a differential peruse operation. This implies that. Both those saved worth and its opposite would utilize within assessment to determine. The saved worth. When those onset of a peruse operation, the wordline may be. Held low and the two bit lines associated with the cell through. Transistors M5 what's more M6 would precharged secondary to VCC. Since the entryways of M5 and M6 are held low, these entry transistors are off and the cross-coupled lock is disengaged starting with those bit lines.

Though a ’0’ may be put away on the exited capacity node, those entryways of the lock of the. Right would low that implies that transistor m3 will be at first transformed off. In the same way, m2 will additionally make off at first since its entryway. Is held helter skelter, this brings about a rearranged model demonstrated , for perusing a saved ’0’ [8].

C. Write Operation:

For A standard 6T SRAM cell, composing will be carried out by bringing down a standout amongst the Bitlines on ground same time attesting the wordline.

On compose a ’0’ BL is. Lowered, same time composing a ’1’ obliges BL to make brought down. The reason is this? Let’s detract a closer take a gander at the Mobile The point when composing a ’1’.

Concerning illustration in the past sample of a read, the Mobile need a ’0’ saved also for Straight forwardness those schematic need been diminished in the same lifestyle likewise in front. That principle distinction not withstanding may be that those bitlines no more need aid discharged.

Table 1. Simulation Result

SRAM Cell	Leakage Current	Average Delay
Conventional	859.3 pA	5.8540 ns
FinFET	758.9 pA	4.9810 ns
FinFET with SVL	584.2 pA	4.5430 ns

VI. CONCLUSION

In this postulation another methodology will a fully static six-transistor(6T) SRAM. Conventional 6T SRAM and FinFET 6T SRAM are analyzed through cadence virtuoso tool in 22 nm technology. It is seen that sub-threshold and gate leakage, both effects the operation of the SRAM cell. In this paper FinFET is used to simulate the 6T SRAM cell and it is concluded that FinFET increases the performance of SRAM cell. The considerable change in the sub-threshold leakage is observed in comparison with the gate leakage. Total leakage in the SRAM cell can be reduced to 10% using FinFET. Further SVL technique is applied in FinFET SRAM cell in which LSVL provides increased ground voltage and USVL provides reduced supply voltage during standby mode which reduces the leakage by 23%. Therefore, results in reduced power dissipation and increased performance.

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