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Design and Analysis of Low Power Pulse Triggered Flip-Flop

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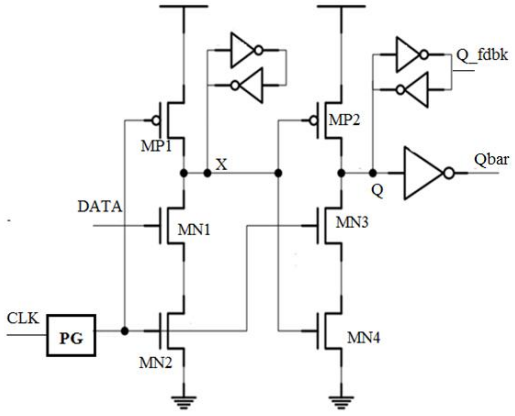
Abstract*: This explicit pulse triggered flip flop consist of a pulse generator and a true single phase clock latch based on a signal feed through scheme. The pulse generator is built with two CMOS inverters along with transmission gate logic which reduces the complexity of the circuit. The Pulse generation logic used in the explicit mode by a single pulse generator is shared for many number of flip flop at a time result in reduction of power not only this overall transistor count and delay can also been reduced.. And this flip flop can achieve better D-Q delay and by using this explicit pulse triggered flip flop a synchronous counter is constructed and power dissipated is very less.

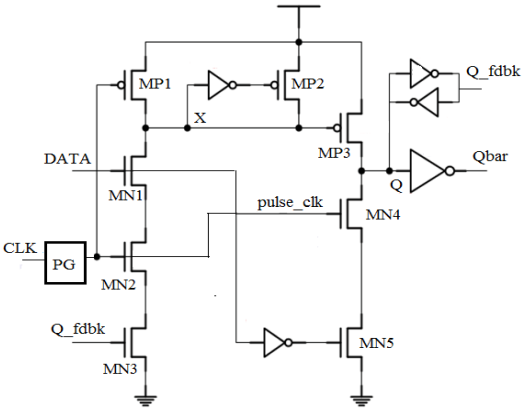
***Keywords— flipflop , to reduce no:of transistor , delay, power*.**

I. INTRODUCTION

In current scenario the requirement of portable equipment is increasing rapidly so that development of VLSI design places a major role in the complex systems. Where the complex system consists of analog, digital as well as memory elements. Where all this can be integrated on a single chip. For designing a circuit we come across many design metrics like low power, high speed and reduced the area of chip by considering the above design metrics a novel explicit Pulse triggered flip flop is designed. Flip flop are extensively used as a basic storage elements in a digital systems. There are many type of flip flop designed basing of their operation like master and slave based flip flop, conventional transmission gate flip flop and pulse triggered based flip flop. In this design a pulse triggered flip flop is preferred compare with other two flip flop because pulse triggered flip flop is one which can execute in a single stage instead of two stages and sometimes the pulse triggered flip flop acts like an edge- triggered flip flop when there is a sufficient narrow latch is present. Pulse triggered flip flops are classified into two types based on their pulse generator used .They are implicit and explicit type pulse triggered flip flops. In implicit type of pulse triggered flip flop the pulse generator is present inside the flip flop where as in the explicit pulse triggered flip flop the pulse generator is present outside the flip flop [1], [2]



(a)



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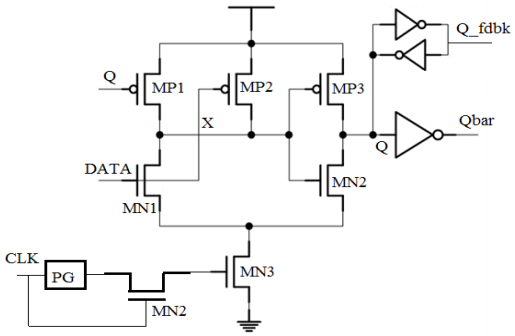

(c)

Fig. 1. Flip Flop Design (a) ep-DCO , (b) CDFF and (c) MHLFF

A. Some Explicit Type Pulse Triggered Flipflop

In this paper I have took some flip flop which exist already these designs are done in 130n meter technology and compare with other design which are done by changing the pulse generator Fig 1(a) shows a classic explicit pulse triggered flip flop . In this design pulse generator is designed in a such way that four inveters are taken along with a Nand gate and a tspc latch.This design face a problem of switching power dissipation .To over come this problem another flip flop is designed . Fig 1(b) show that CDFF design in this same type of pulse generator is taken by little change in the latch design .By keeping the problem in the mind a new design of CDFF is designed with some of the remedial measure like conditional precharge,conditional capture and conditional discharge and conditional pulse enhancement scheme have been proposed [3],[4],[5],[6],[7] to over come the problem of above design in the CDFf an extra transistor of nmos is taken and given to the Q-fdbk which controls the discharge and make the input data remains constant but this design face a problem of worst delay so to over come this problem another pulse triggered flip flop is designed .First a weak pmos transistor is taken and gate of pmos transistor is is connected to the ground and second a nmos pass transistor is used whichcontrolled by the pulse clock is included so that input data can drive node. The node level can thus be quickly pulled up to shorten the data transition delay [8]. The modified hybrid latch flipflop (MHLFF) Fig 1(c) also uses a static latch. The keeper logic at node *X* is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node *X* when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node *X* is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one V_T) is applied to the discharging transistor MN3. Second, node *X* becomes floating in certain cases and its value may drift causing extra dc power [7].

II. PROPOSED MODEL

A novel explicit pulse triggered flip flop is designed. This flip flop consist of a pulse generator and a transmission gate.

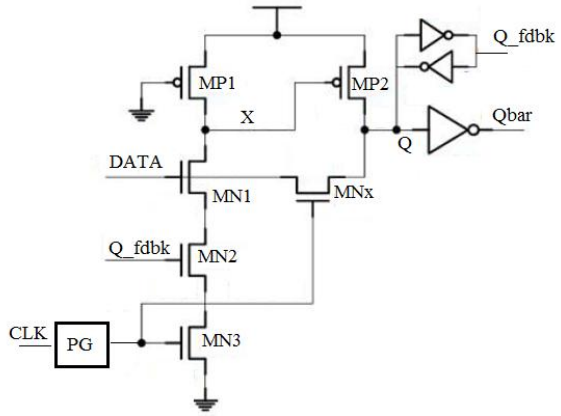

Fig.2. Schematic Of The Proposed P-FF Design

Referring to Fig.2 the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node *X* can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X* [9], [10]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feedthrough. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays.

A. Principles Of FF Operations

When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node *X* is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node *X* is discharged to turn on transistor MP2, which then pulls node Q high.this corresponds to the worst case timing of the FF operations as the discharging path conducts only for a pulse duration. However, with the signal feedthrough scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened. Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case

because MNx conducts only for a very short period. when a "1" to "0" data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

III.SIMULATION RESULTS

The proposed pulse triggered flip fliop is designed against existing flipflop design and this design is designed in Tanner 90n meter technology and simulated both in pre-layout.After simulation delay, number of tansistor and power is less compare to existing flip flop this is shown in table1 and Fig 3 show the circuit and fig 4 shows waveform of new explicit pulse triggered flip flop .

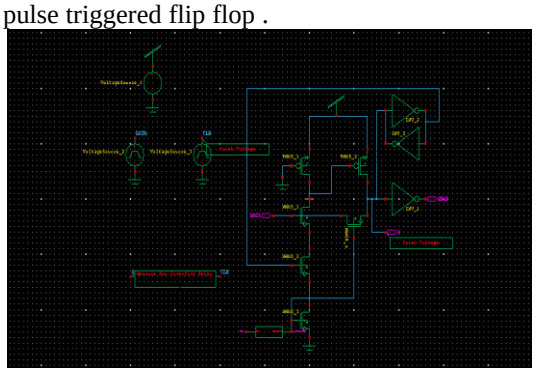

Fig. 3. Proposed P-FF Design

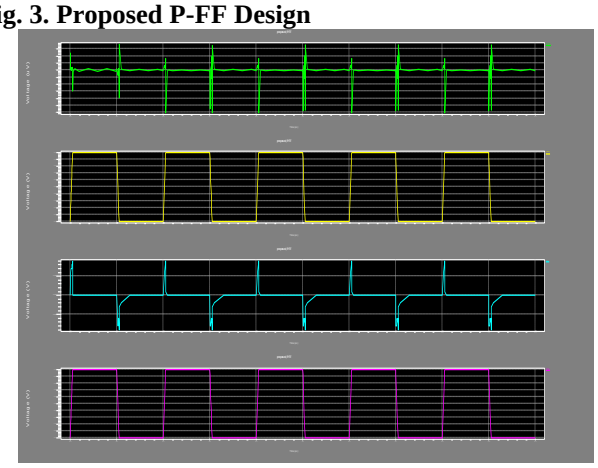

Fig. 4. Simulation Waveform

Table1
Comparison Of Flipflop Design

CIRCUIT NAME	POWER IN WATTS	DELAY
CDFF	4.2786	5.180
EP-DCO	4.8076	5.250
MHLFF	5.3449	5.250
PROPOSED P_FF	3.8147	5.180
STATIC_CDFF	9.7723	5.250

IV.CONCLUSION

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to provide a signal feedthrough from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspect.

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