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Data Encoding And Decoding Techniques For NOC Applications

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Abstract: In this paper we present the data encoding and decoding schemes are used to reduce the power dissipation of the communication system in a Network-on-Chip (NoC). In NoC the main source of power dissipation by the network on chip links. The self-switching and coupling-switching activities are caused for link power dissipation. In this paper we present a set of data encoding and decoding schemes are mainly operating at flit level and on an end-to-end basis, which allows us to minimize the both self and coupling switching activities. The self-switching is reduce by checking the switching transition and then the coupling technique is included with the wormhole routed network, that is flits are encoded by the network interface before they are entered in to the network and are decoded they are focused on reducing hardware.

Keywords: Coupling switching activity, data encoding, interconnection on chip, low power, network-on-chip(NoC),power analysis by the destination NI (network interface)

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1. Introduction

As the number of IP modules in System-on-Chip (SoC) increases, bus-based interconnected architectures may prevent these systems to meet the performance by more applications. For systems with intensive parallel communication needs buses are not provide the needed bandwidth, latency and power consumption. To overcome such a communication bottleneck is the use of switching network, called Network-on-chip (NoC). NoC is an on chip packet based communication system between blocks connected via routers. However, in recent years research has shown that Network-on-Chip (NoC) is likely to replace buses.

Network-on-Chip architectures development comes directly from the improving the interest around System-on-Chip (SoC) and Multi-Processor-System-on-Chip (MPSoC) technologies. In a SoC oriented approach the designer is to integrate in the same chip with different IP cores, with different functionalities.The designing philosophy oriented to the concept of MPSoC is even more up-to-date and definitely supports engineers to study and to develop the interconnect technologies available present days.

To known the requirements of the NoCs, it is useful to consider the challenges faced by SoC and MPSoC. Technological modifications in the field of silicon technology open the road for large performance improvements. Unfortunately these technological improvements to be fully exploited needed a rethought of present VLSI design flow. There is a one possible solution to these problems needs a heavy adoption of hardware reuse methodologies that becomes the way to the generation of flexible platforms, while reducing the design effort for design a new systems. Tomorrow complex on-chip systems are always generates designing a large number of IP modules, to build a house as well as by the third party partners. Further the improvements of the number of elements that requires to be interconnected is starting to raise the negative side effects of classical "shared bus" architectures, and presents the required for an interconnection of a system that allows the one IP to use the communication resources at a time. Network on chip topology is designed by an arbitrary number of elements and they are three basic kinds of functional blocks.

- Network Interfaces
- Switches
- Links

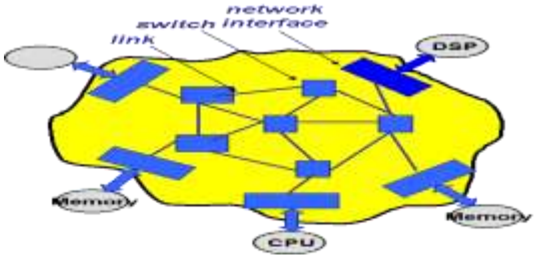


Fig 1: Network on chip topology

Network Interfaces: NIs connected to total IP cores to the network and mapping the bus type transition directly comes from the IPs into the packets that can be transmit inside of the Network on chip and, on the other side, designing the bus transactions that belong to packets that required to exit the NoC.

Switches: Switches carry out the task of leaving packets inside the network, based on the specific routing scheme. The number of ports based on the designing topology of the network. Usually they are having buffers inside that are used for storing information tokens, in order to reducing the problem of loosing data due to congestion problems.

Links: Links connects to the switches with network interfaces or with switches. Links are latency insensitive and can also contain buffering resources if required by a particular application

This paper is organized as follows. We briefly discuss Previous Work in Section II, while Section III discuss an overview of the proposed encoding technique. The advanced data encoding schemes along with possible hardware implementations and their analysis are described in Section IV. The results for the hardware overhead, power and performance of the proposed encoding schemes these are discuss in Section V.

2. Related works and Motivation

Several data encoding techniques for low power have been proposed in literature. Almost all of them have been defined to be applied in the context of bus-based architectures with the primary goal of minimizing transition activities on buses while ignoring cross-coupled capacitance. Bus invert method [6] can be applied to encode randomly distributed data patterns. Highly correlated access pattern exhibit spatiotemporal locality which is exploited by Gray code [8], T0 method [9] and the working-zone encoding [10]. Application specific approaches based on a priori knowledge of the traffic patterns have been proposed [11]–[13]. Other encoding techniques have been defined to take into consideration the contribute of cross-coupled capacitance [7], [14].However, all the above proposals have been applied in the context of bus-based architectures .In the context of NoCs, Jantsch et al. [5]analyze the use of partial bus invert coding as link level low power encoding technique with the conclusion that it spends several times more power than no encoding at all, if normalized for the same performance, which is done by adjusting supply voltage and frequency. However, differently from how we propose in this paper, they consider point-to-point encoding in which every router in the NoC decodes the incoming flits and encodes the outgoing flits. In addition [5] does not take advantage of the pipelined nature of the flow of flits through the links of the routing path which is guaranteed by the wormhole switching technique generally used in NoCs. Conversely, the data encoding scheme that will be presented in the following is designed to exploit the wormhole switching technique making it possible to operate an end-to-end encoding which does not determine any overhead in terms of routers and links.It only requires the upgrade of the network interface which is augmented with the encoding decoding logic leaving the underling network as is.

3. Overview of the proposal

The basic idea of the proposed technique is the packets are transferred through the network after that the bits are encoded. This technique is more helping to reduce the switching activity and coupling switching activity in the links traversed by the packets. This self-switching activity and coupling switching activity are responsible for the link power dissipation. Here we refer to end-to-end scheme. Based on the end to end scheme we are having a better advantage. The advantage is a pipeline nature of the wormhole switching technique [18]. Since the same sequence of all the packets passes through all the links of the routing path. The NI may provide the same power saving for all the links. The advanced scheme, an encoder and decoder block are added to the NI. The gray input is applied for all the three scheme encoders. The gray coding technique is used for the error correction application. The encoder encodes all the leaving bits of the packets other than header bit such that the power dissipated by the inter router and point-to-point link is minimized [19].

4. Proposed encoding schemes

The main aim of the proposed encoding scheme is to reduce the power dissipation by minimizing the coupling transition activities on the links of the interconnection network. In the table specifies that they are four types of coupling transitions. A Type I occurs when one of the line is switches and remaining one is unchanged. A Type II occurs when one of the lines switches from low to high and another one is switches from high to low. A Type III occurs both the lines switches simultaneously. A Type IV occurs when both the lines are remains unchanged.

In this paper we are introducing three different types of schemes which are extension of Scheme-I encoder. The proposed encoder will transforms type1 transitions into type2, 3 and 4 transitions by making, odd and even inversions to the input binary data. In odd inversion odd bit positions in the binary data are inverted and in even inversion even bit positions in the binary data are inverted.

General power equation:

In general dynamic power consumed by the interconnects and drivers is P consume =

[T0->1 (Cs + Cl) + TcCc]Vdd2 F clk (1)

Here, T0->1 is the no. of 0 to 1 transitions in the binary data, Tc is the number of correlated transitions, Cs is the line to substrate capacitance, Cl is the load capacitance, Vdd is the supply voltage and F clk is the clock frequency.Here Tc is the weighted sum of coupling types of transitions and is given by

Tc = K1T1 + K2T2 + K3T3 + K4T4 (2)

On substitution of equation (2) in (1) and neglecting Cl we can rewrite equation (1) as P consume α

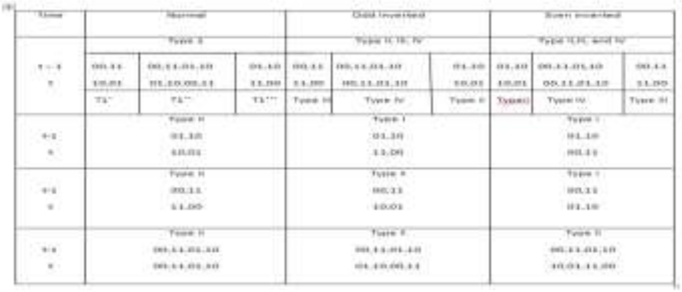
T0->1Cs + (T1 + 2T2) Cc (3)

By using the above equation we can estimate general power consumed by the input data.

A. Scheme I

In scheme 1, our main target is to reducing the number of Type 1 transitions and Type 2 transitions. Type 1 transitions is converted into Type III and Type IV transitions and Type II transitions is converted into Type I transitions. This scheme compares the two data‘s based on to reducing the link power reduction by doing odd inversion or no inversion operation.

Table 1: Effect of Odd and Even inversion on change of Transition Types



Time	Normal			Odd inverted			Even inverted		
	Type I			Type II, III, IV			Type II,III, and IV		
t - 1 t	00,11 10,01	00,11,01,10 11,10,00,11	01,10 11,00	00,11 11,00	00,11,01,10 00,11,01,10	01,10 10,01	01,10 10,01	00,11,01,10 00,11,01,10	00,11 11,00
	T1'	T1''	T1'''	Type III	Type IV	Type II	Type II	Type IV	Type III
t-1 t	Type II 01,10 10,01			Type I 01,10 11,00			Type I 01,10 00,11		
t-1 t	Type II 00,11 11,00			Type II 00,11 10,01			Type I 00,11 01,10		
t-1 t	Type II 00,11,01,10 00,11,01,10			Type II 00,11,01,10 01,10,00,11			Type II 00,11,01,10 10,01,11,00		

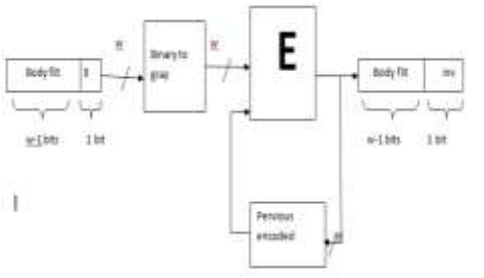


Fig 2.Scheme 1(a) Block diagram of encoder

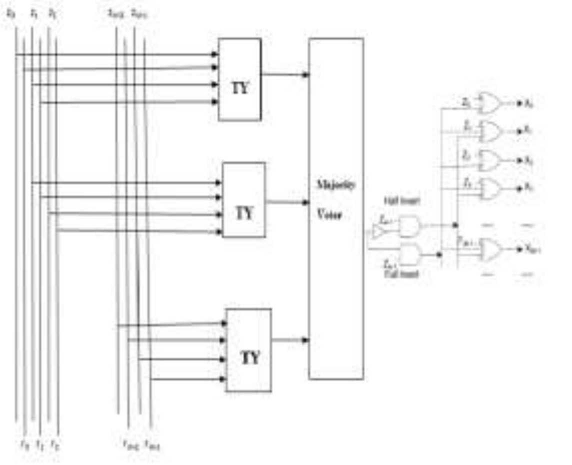


Fig 2.Scheme 1(b) Architecture for encoder block

when the input data is odd inverted the dynamic power consumed by the link (fromtable1 and equation1) is given by P odd α

$$[T0\text{->}0(odd)+T0\text{->}1(even)]Cs+ [K1(T2+T3+T4)+2T1''']Cc \quad (4)$$

Here, T0->0(odd) is the total number of 0 to 0 transitions in odd bit positions of the binary data and T0->1(even) is the number of 0 to 1 transitions in the even bit positions. If P consume > P odd i.e., power consumption due to transmission of original data is greater than the power consumption due to odd inversion of input data, it is better to odd invert the input data before transmission. On substitution of equation (3) and (4) in above condition we can obtain

$$T\,b > T\,a \quad (5)$$

here,

$$T\,b = T2+T1-T1''',$$
$$T\,a = T3+T4+T1''' \text{ and}$$
$$T\,a + T\,b = w-1 \quad (6)$$

If the above condition is true, odd inversion is done else the data is transmitted without any inversion.

Architecture:

The Fig2 shows the scheme-I encoder architecture ,Here the TY block this takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs, whether more number of type 1 and type 2 transitions is occurring means it set the output state to 1, otherwise it set the output to 0. The odd inversion is performed for these type of transitions. Then the next block is the Majority code it checks the state, if the number of one‘s is greater than zeros or not and it implemented using a simple circuit. The last stage using the XOR circuits, this circuit is used to perform the inversion on odd bits. The decoding is performed by simply inverts the encoder circuit when the inverting bit is high.

B. Scheme II

In scheme II, our main goal is to reducing the number of Type II transitions. Type II transitions are converted into Type IV transitions. This scheme compares the two data‘s based on to reducing the link power reduction by doing full inversion or odd inversion or no inversion operation.

Let us consider P odd, P full P even and P consume, as the power consumed by odd inversion, full inversion, even inversion and no inversion respectively. Amount of power consumed by the link when the input is even inverted is given by,

P even α [T 0->1(odd) + T 0->0(even)]Cs + [(T2 + T3 + T4) + 2T1']Cc (12)

Condition for even inversion based on first encoder can be obtained by using P even < P consume and is given by

$$T\,v > (w-1)/2 \quad (13)$$

Where T v = T2 + T1 – T1

Based on condition P even < P odd (second encoder) we can obtain

$$T\,v > Tb \quad (14)$$

Based on P even < P full we can obtain a condition

$$2(T2 – T4'') < 2Tv – w + 1 \quad (15)$$

Where,

$$Tr = T3 + T4 + T1' \text{ and } Tr + T\,v = w-1 \quad (16)$$

The power consumption due to even inversion can be minimized when P even < P consume, P even < P odd and P even < P full. From the equations (13), (14) & (15) we obtain v > (w-1)/2, T v > Tb, 2(T2 –T4”) < 2Tv – w + 1 (17) The power consumption due to full inversion can be minimized when P full < P consume, P full < P odd and P full < P even. Based on equations (11) and (15) we obtain

$$2(T2 – T4'') > 2Tb – w + 1,\ T2 > T4'',$$
$$2(T2 – T4'') > 2Tv – w + 1 \quad (18)$$

Similarly the power consumption due to odd inversion can be minimized when P odd < P consume odd < P full and P odd < P even. Based on equations (10) and (13) we obtain2

$$(T2 – T4'') < 2Tb – w + 1,\ Tb > (w-1)/2,$$
$$T\,v < Tb \quad (19)$$

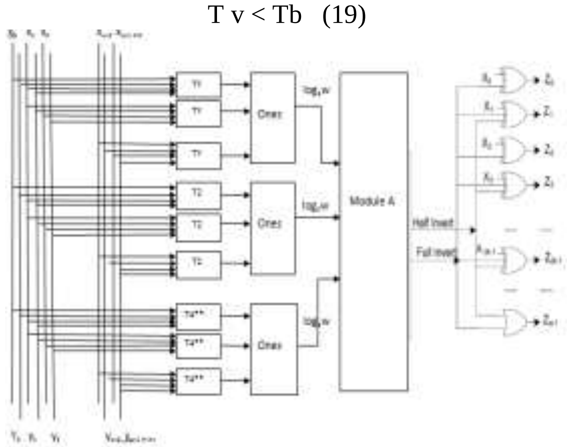


Fig 3. Encoder architecture scheme II

Architecture:

Full and odd inversion based this advanced encoding architecture consist of w-1 link width and one bit for inversion bit which indicate if the bit travel through the link is inverted or not. W bits link width is considered when there is no encoding is applied for the input bits. Here the TY block from scheme 1 is added in scheme 2. This takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs.We have T2 and T4** blocks which determines if any of the transition types T2 and T4**occur based on the link power reduction. The number of ones blocks in the next stage. The output of the TY, T2 and T4** send through the number of one‘s blocks. The output of the ones block is log 2 w. The first ones block is used to determine the number of transitions based on odd inversion. The second ones block determines the number of transitions based on the full inversion and the then another one ones block is used to determine the number of transitions based on the full inversion. These inversions are performed based on the link power reduction. Based on these ones block the Module A takes the decision of which inversion should be performed for the link power reduction. For this module is satisfied means the output is set to _1‘. None of the output is set to _1‘ if there is no inversion is takes place. The module A is implemented using full adder and comparator circuit

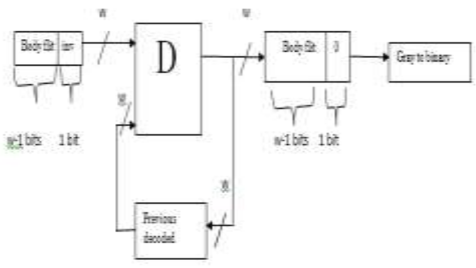


Fig 4. Block diagram for decoder

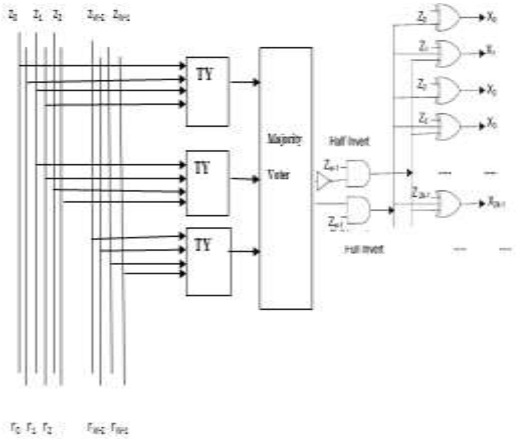


Fig 5. Decoder architecture scheme II

The block diagram of the decoder is shown in Fig 4. The w-1 bits input is applied in the decoder circuit and another input of the decoder is previous decoded output. The decoder block compares the two input data‘s and inversion operation is performed and w-1 bits output is produced. The remaining one bit is used to indicate the inversion is performed or not. Then the decoder output is given to the gray to binary block. This block converts the gray code into original binary input.

In decoder circuit diagram (Fig 5) consist of TY block and Majority vector and Xor circuits. Based on the encoder action the TY block is determined the transitions. Based on the transitions types the majority blocks checks the validity of the inequality given by(2). The output of the majority voter is given to the Xor circuit. Half inversion, full inversion and no inversion is performed based on the logic gates.

C. Scheme III

In scheme III, we are adding the even inversion into scheme II. Because the odd inversion converts Type I transitions into Type II transitions. From table II, T1**/T1*** are converted into Type IV/Type III transitions by the flits is even inverted. The link power reduction in even inversion is larger than the Odd inversion.

Let us consider P odd, P full P even and P consume, as the power consumed by odd inversion, full inversion, even inversion and no inversion respectively. Amount of power consumed by the link when the input is even inverted is given by,

$P\ even\ \alpha\ [T\ 0\text{->}1(odd) + T\ 0\text{->}0(even)]Cs + [(T2 + T3 + T4) + 2T1']Cc$ (12)

Condition for even inversion based on first encoder can be obtained by using P even < P consume and is given by

$$T\ v > (w-1)/2 \quad (13)$$

Where $T\ v = T2 + T1 – T1$

Based on condition P even < P odd (second encoder) we can obtain

$$T\ v > Tb \quad (14)$$

Based on P even < P full we can obtain a condition2

$$(T2 – T4'') < 2Tv – w + 1 \ (15)$$

Where,

$Tr = T3 + T4 + T1'$ and $Tr + T\ v = w-1$ (16)

The power consumption due to even inversion can be minimized when P even < P consume, P even < P odd and P even < P full. From the equations (13), (14) & (15) we obtain,

$$T\ v > (w-1)/2,\ T\ v > Tb,\ 2(T2 – T4'') < 2Tv – w + 1 \quad (17)$$

The power consumption due to full inversion can be minimized when P full < P consume, P full < P odd andP full < P even. Based on equations (11) and (15) we obtain2

$$(T2 – T4'') > 2Tb – w + 1,\ T2 > T4'',2(T2 – T4'') > 2Tv – w + 1 \quad (18)$$

Similarly the power consumption due to odd inversion can be minimized when P odd < P consume,P odd < P full and P odd < P even. Based on equations (10) and (13) we obtain2

$$(T2 – T4'') < 2Tb – w + 1,\ Tb > (w-1)/2,$$
$$T\ v < Tb \ (19)$$

Based on conditions (17), (18) & (19) we designed the encoder.

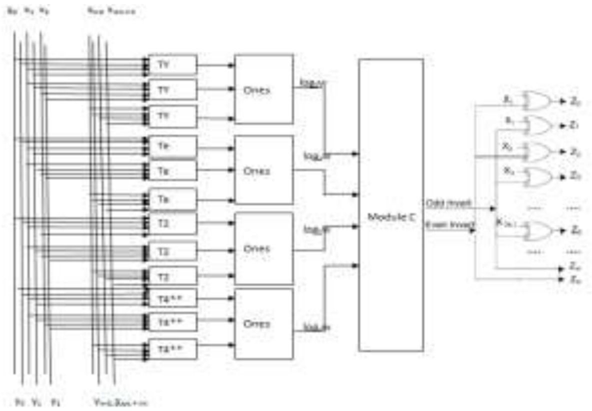


Fig 6. Encoder architecture for scheme III

The encoding architecture (Fig 6) in scheme III is same of encoder architecture in scheme I and II. Here we are adding the Te block to the scheme II. This is based on even invert condition, Full invert condition and Odd invert condition. It consist of w-1 link width input and the w bit is used for the inversion bit. The full, half and even Inversion is performed means the inversion bit is set _1‘, otherwise it set as _0‘.The TY, Te and T4** block determines the transition types T2, Te and T4**. The transition types are send to the number of ones block. The Te block is determined if any of the detected transition of types T2, T1** and T1**. The ones block determines the number of ones in the corresponding transmissions of TY, T2, Te and T4**. This number of one’s is given to the Module C block. This block check if odd, even, full or no invert action corresponding to the outputs _10‘, _01‘, _11‘or _00‘respectively, should be performed. The decoder architecture of scheme II and scheme III are same.

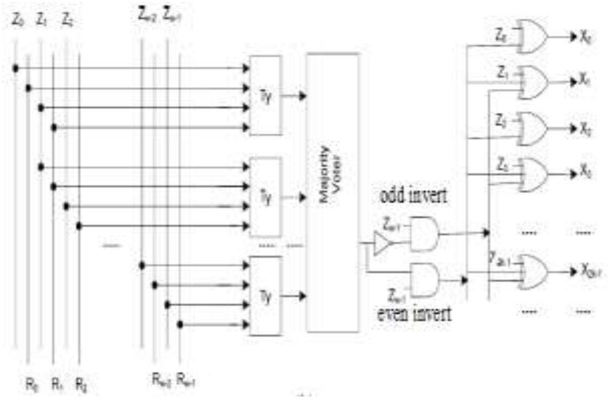


Fig 7: Decoder internal view of scheme

5. Experimental Results

5.1 Simulation Results:

The simulation results are provided by using the power model equations for the schemes.Fig8.shows the simulation result of scheme I reducing Type I and Type II transitions using the encoding techniques. The output of the scheme I reducing the number of Type I and Type II transitions by using the odd invert condition.

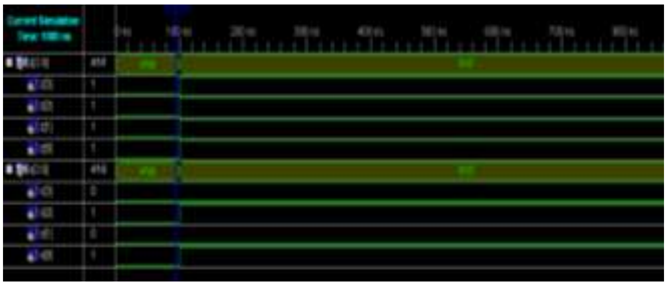


Fig 8.Simulation result of Scheme I Encoder

Fig9.shows the simulation result of scheme II converts Type II transitions into Type IV. In scheme II the number of type II transition is converted into Type IV transitions by using the odd and full inversion condition.Fig.8.shows the simulation results for scheme-III encoding. Here we are performing the odd, even and full inversions in the schemes to reducing the transitions. Their encoder is extension to second and it is extension to firs encoder.

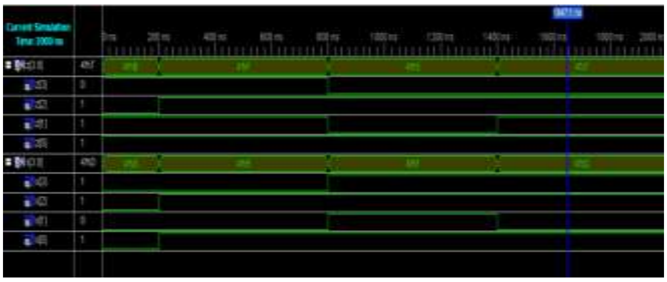


Fig 9.Simulation result of Scheme II Encoder

Fig 10.shows the simulations result of scheme III (Type I converted into Type II) using the gray encoding. The output of the scheme III reducing the number of Type I into Type II transitions by using odd, full and even inversion.

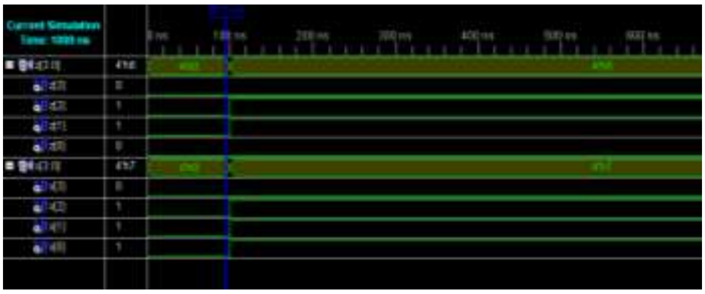


Fig 10.Simulation result of Scheme III Encoder

5.2: RTL (Register Transfer Level) schematic diagrams

RTL Schematic diagrams of Encoder and Decoder of Scheme I, Scheme II and Scheme III are shown in fig 11 .The design was implemented in Spartan-3E kit.

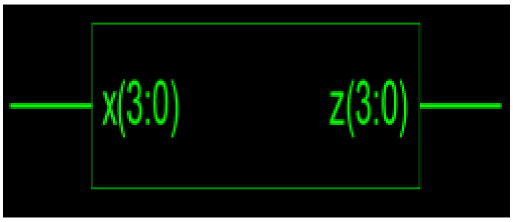


Fig 11: RTL Schematic Encoding and Decoding of scheme I, Scheme II and Scheme III.

5.3: Synthesize Result:

The power utilization of Scheme I, Scheme II and Scheme III are as shown in table 2.

Table 2: Power analysis of Different Schemes

	SCHEME I	SCHEME II	SCHEME III
Total Quiescent Power	0.081	0.081	0.081
Total Dynamic Power	0.005	0.004	0.004
Total Power	0.086	0.085	0.085

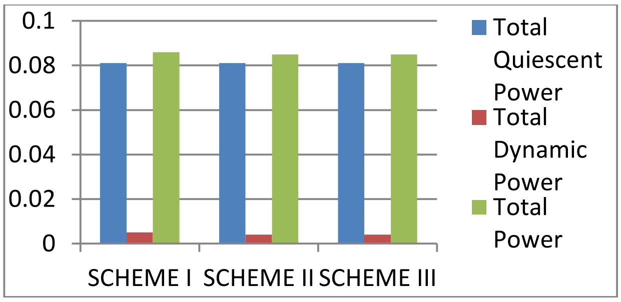


Fig 12: Power analysis of Different Schemes

Advantages

- High power saving.
- Minimize the coupling switching activities.

Applications

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- Routers and link architectures.
- Power hungry wires.

Conclusion

More than 50% of power dissipated by the links of an NoC. So presenting set of Data Encoding and Decoding schemes are used to reducing the power dissipated by the links of an NoC. The Existing Bus-invert encoding to decrease no. of transitions and Gray code encoding method is used reduce the errors & noise. The proposed Encoding and Decoding techniques are used decrease the more than 50% of power dissipation. Especially the decoding techniques are mainly focused on reducing hardware complexity.

Future scope

During transmission of message over a noisy channel, there is a chance to obtain corrupted message. To overcome this and to make the encoder more efficient in transmission we use 'Low Density Parity Check' code. So we can extend our work by using LDPC code which is a linear error correcting code. The LDPC code uses low depth accumulators in parallel, which can encode a small portion of the input frame.

References

[1] International Technology Roadmap for Semiconductors.(2011)[Online].Available: http://www.itrs.net

[2] M. S. Rahaman and M. H. Chowdhury, "Crosstalk avoidance and errorcorrection coding for coupled RLC interconnects," in *Proc. IEEE Int.Symp. Circuits Syst.*, May 2009, pp. 141–144.

[3] W. Wolf, A. A. Jerraya, and G. Martin, "Multiprocessor system-on-chip MPSoC technology," IEEE Trans. Comput.-Aided Design Integr. Circuits *Syst.*, vol. 27, no. 10, pp. 1701–1713, Oct. 2008.

[4] L. Benini and G. De Micheli, "Networks on chips: A new SoC paradigm," *Computer*, vol. 35, no. 1, pp. 70–78, Jan. 2002.

[5] S. E. Lee and N. Bagherzadeh, "A variable frequency link for a poweraware network-on-chip (NoC)," *Integr. VLSI J.*, vol. 42, no. 4, pp. 479–485, Sep. 2009.

[6] D. Yeh, L. S. Peh, S. Borkar, J. Darringer, A. Agarwal, andW. M. Hwu,

"Thousand-core chips roundtable," *IEEE Design Test Comput.*, vol. 25,