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Design and Implementation of Vedic Algorithm using Reversible Logic Gates

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Abstract: ***Multiplication is one of the important operation in most digital signal processing (DSP) applications. Sometimes the performances of DSP applications is dominated by the speed at which a multiplication operation can be executed. The main goal to design the multiplier is to reduce the delay and power dissipation of a multiplier. Hence improved vedic multiplier is designed to increase the efficiency of the system. Implementing this vedic multiplier with reversible logic additional reduces power dissipation. Vedic multiplier is designed using one of the vedic algorithm," Nikhilam Navatascaram Dasatah which is mean by "All from Nine and the last from Ten". This method is implemented using reversible logic gates to reduce the power dissipation and number of logic gates. The synthesis and simulation of Nikhilam Reversible algorithm is obtained by using Xilinx ISE 13.2, implementation and detailed design analysis results are given in the paper.***

Keywords: Computation, Multiplier, Nikhilam Algorithm, Power dissipation, Reversible logic gates, Vedic mathematics.

1. Introduction

In Digital signal processor (DSP) the operation is performed by various methods such as adder, subtractor, multiplier. The performance of the DSP processor is mainly depends on the multiplier, because the multiplication require more time and area of the device. To improve the speed of the DSP, the digital multipliers such as Array Multiplier, Wallace tree multiplier and booth multiplier are designed. These multipliers are implemented using the VLSI technology. The low power and high speed VLSI can be implemented with different methods. The three main concerns for VLSI design are power, area and delay.

In an array multiplier the multiplication of two binary numbers is done by using a combinational circuit that gives the product bits all at once thus making it a fast way of multiplying two numbers since the only delay is the time for the signals to propagate through the gates that form the multiplication array. The disadvantage of array multiplier is it needs a large number of gates and hence it is less economical [1]. The efficiency of the multiplier is improve by using the arrangement of adders, this arrangement can be done by two methods such as a carry save array (CSA) method and a Wallace tree method. But these multiplier also have some drawback such as, the CSA multiplier cannot achieve the high speed operation because the execution time depends upon the number of bits of the multiplier and in the Wallace tree multiplier, the circuit layout is difficult though the speed of operation is high meanwhile the circuit is somewhat unbalanced [1].

The another improvement in the multiplier is by the Booth recording multiplier which reduces the numbers of partial products; this multiplier can scan the three bits at a time to reduce the number of partial products. This method also reduces the number of adders and hence the delay necessary to produce the partial sums by examining three bits at a time. This high performance Booth multiplier have drawback of power consumption, because of the large number of adder cells (15 cells for 8 rows-120 core cells) which consumes more power. The conclusion is that all these multiplier leads to more consumption of power and reduction in efficiency[1][2] .

To reduce the power dissipation and improve the speed and efficiency of the multiplier, the new technique is used which is called as the vedic multiplier. This vedic multiplier is based on ancient Indian vedic mathematics. Vedic mathematics consists of 16 vedic formulae or sutras, from these 16 sutras the multiplier is designed by using two sutras, such as the "Urdhva-tiryakbhyam" sutra which mean "vertically and crosswise" and another one is "NikhilamNavatas' caramam Dasatah" which mean "All from 9 and the last from 10".

This paper proposes an implementation of "Nikhilam Navatas'caramam Dasatah" 8×8 multiplication algorithm by using reversible logic gates. Reversible logic is one of the promising field for future low power design technologies. Since one of the requirements of all DSP processors and other hand held devices is to minimize power dissipation multipliers with high speed and lower dissipations are critical.

2. Vedic Mathematics

The founder of vedic mathematics the great saint and mathematician 'Shri Bharati Krisna Thirthaji Maharaja',introduced the Vedic Sutras (formulae). Vedic mathematics includes 16 different formulae for various

computation, the complex multiplier design using one of the vedic formula for high speed performance and low power application is presented in this paper.The multiplier is implemented with the "Nikhilam Sutra" using reversible logic gate is described in this paper.

2.1 Nikhilam Algorithm

The "Nikhilam Navatascaram Dasatah literally means All from Nine and the last from Ten. The sutra basically means start from the left most digit and begin subtracting 9 from each of the digits; but subtract 10 from the last digit [2]. The following examples illustrates the way in which this Sutra could reduce the number of iterations to reduce the whole Multiplication.

Case 1: When both the numbers are less than the base

92 × 96

Nearest Base = 100

Table 1: Multiplication for the two numbers less than the base.

Multiplicand	92	(100 - 92)= 8
Mulitiplier	96	(100- 96)= 4
	(92-4) or (96-8) = 88	8× 4 = 32
Result	8832	
RHS : Multiplication result = 32 **LHS :** Common difference = 88 **Final Result :** 92 × 96 = 8832		

Case 2: When two numbers are higher than the base

103 × 109

Nearest Base = 100

Table 2: Multiplication for the two numbers higher than the base.

Multiplicand	103	(100+3) = 3
Mulitiplier	109	(100+9)= 9
	(103+9)or (109+3) = 112	3× 9 = 27
Result	11227	
RHS : Mutiplication result = 27 **LHS :** Here we calculate the common addition, which is 103+ 9=112 and 109+3=112. **Final Result** = 11227		

Case 3:When one number is higher and one number is lower than the base.

93×105

Nearest Base is 100

Table 3: Multiplication of the two numbers higher and lower than the base.

Multiplicand	93	(100-93) = 7
Mulitiplier	105	(100+5)= +5
	(93+5) or (105-7) = 98	-7× 5 = -35
Result	9765	
RHS : Multiplication result is -35, then subtract 35 from the base 100, hence the result = 65 **LHS** : Common difference is 98, but subtract 1 from 98, hence the result = 97 **Final result** = 9765		

After this illustration, now we discuss the operational principle of Nikhilam Sutra. Suppose we take two numbers for multiplication x and y. p is the product of x and y. mathematically it is expressed as,

$$p = xy \quad (1)$$

the result of this number is taken as,
At RHS,

First we subtract two numbers from the base a = 10n–x and b = 10^n – y respectively.
Then multiply these two numbers,

$$RHS = ab \quad (2)$$

Now for LHS,

$$LHS = (x-b) = (y-a) \quad (3)$$

Now the final result is

$$p = xy + 10^{2n} - 10^n(x+y) - 10^n(x+y) \quad (4)$$

$$p = 10^n\{x-b\} + \{ab\} = 10^n\{y-a\} + \{ab\} \quad (5)$$

Hence the multiplication of two numbers can be done by reducing the number of steps. As less number of steps required to perform the multiplication, the delay required is also minimum and it also reduces the power dissipation. This is the reason that Nikhilam multiplier is efficient for the large number multiplication.

3. Reversible Logic Gates

Nowadays, it is necessary to design a complex digital system which dissipates a low power because, because as the complexity of system increases it will increase the problem of heat dissipation. This complexity of digital system gives rise to the development of new computing hardware which dissipates the less heat to increase the computing power. In 1961,Landauer introduced that losing of bit in circuits causes the smallest amount of heat in computation and the theoretical limit of energy dissipation for losing of one bit computation is KTln2[4]. Where K is a Boltzmann's constant equals to $1.3807\times10^{-23}JK^{-1}$ and T is the temperature at which the computation is performed[4]. At T=300K, this limit is 4×10^{-21}Joules.

Reversible logic has received great attention over the irreversible circuits due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design as well as the computing system. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. Irreversible hardware computation results in energy dissipation due to information loss. Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. Garbage outputs are those which do not contribute to the reversible logic realization of the design. Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate

There are some important constraint for reversible logic circuits as follows:

- Fan-out is not allowed in the reversible logic circuits[7].
- Minimum number of constant inputs must be use[8].
- Reversible circuits can be optimized to obtain minimum number of garbage output[9].
- Quantum cost should be minimum for reversible logic circuit[9].

3.1 Basic Reversible Logic Gates:

Some of the basic reversible logic gates are proposed such as Toffoli gate(TG) [12], Fredkin gate (FRG)[13], Feynman gate (FG)[14],Peres gate (PG),HNG gate. In the proposed system we uses the Peres Gate (PG) and HNG gate. Here we are reviewing the logic circuit and quantum implementation of these reversible gates.

3.1.1Feynman Gate :

The Feynman gate is a 2×2 gate and its logic circuit is as shown in the figure[14]. It is also known as Controlled Not (CNOT) Gate. It has quantum cost 1 and is generally used for Fan Out purposes.

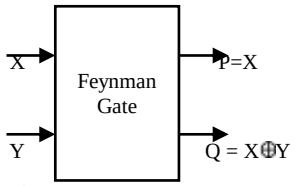

Figure 1: Fynman Gate

3.1.2Peres Gate :

Peres gate is a 3x3 gate and its logic circuit is as shown in the figure [15]. It has quantum cost 4. It is used to realize various Boolean functions such as AND, XOR.

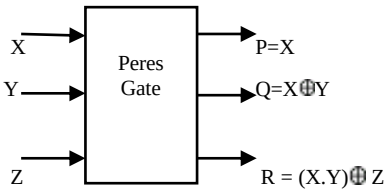

Figure 2: Peres Gate

3.1.3Fredkin Gate :

It is a 3x3 gate and its logic circuit is as shown in the figure [13]. It has quantum cost 5. It can be used to implement a multiplexer.

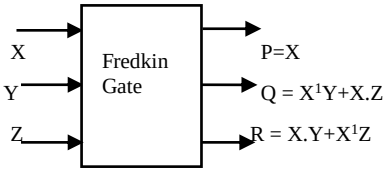

Figure 3: Fredkin Gate

3.1.4Toffoli Gate :

The Toffoli Gate is a 3×3 reversible gate with 3 inputs and 3 outputs. It has Quantum cost 5 [12].

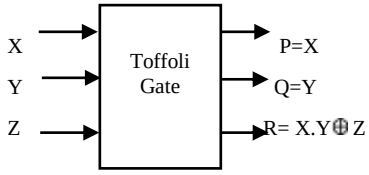

Figure 4: Toffoli Gate

3.1.5HNG Gate :

HNG gate is a 4×4 gate and its logic circuit is as shown in the figure. It has quantum cost 6. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.

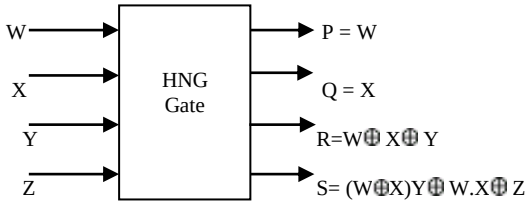

Figure 5: HNG Gate

4. System Architecture

The block diagram of proposed system consists of the basic blocks such as Base selection Module (BSM), 8 bit reversible multiplier and 8 bit Adder. Block diagram of the system is given in Fig.7 :

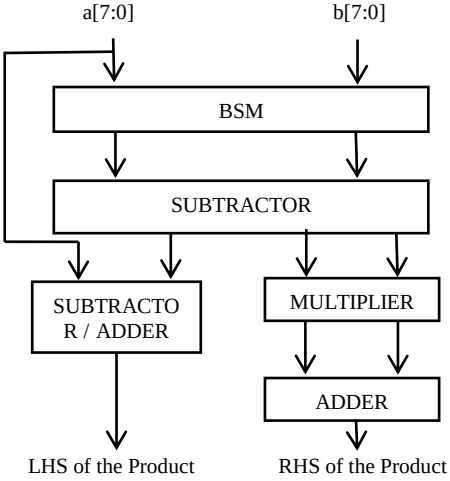

Figure 6: System Architecture

First block of the proposed system is Base Selection Module(BSM), which selects the base of the inputs “a” and “b”. The output of the BSM is given to the Subtractor. In subtractor block the inputs "a" and "b" are subtract from the Base and the output is given to the multiplier and the adder or subtractor block. The main Block of this proposed system is 8 bit reversible multiplier.

4.1 Multiplier

Multiplier performs the important computation of the proposed Nikhilam Vedic multiplier. This multiplier is reversible multiplier because the multiplication operation is performed by the two reversible logic gates. These two reversible logic gates are HNG Gate and Peres Gate (PG). The block diagram of the multiplier is shown below :

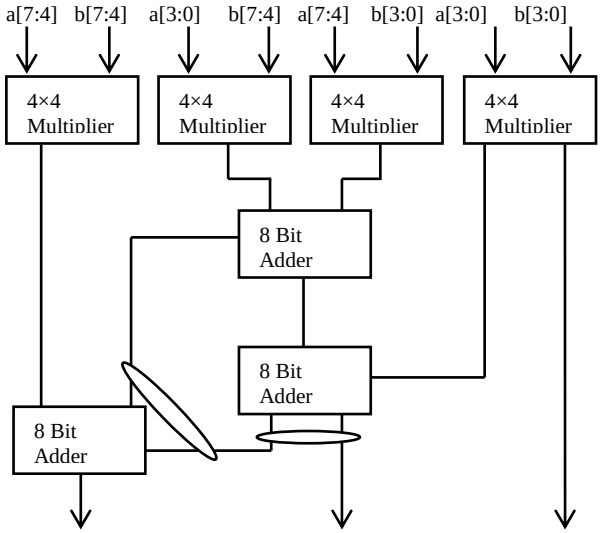

Figure 7 : Block Diagram of Reversible Multiplier

The 4×4 multiplier is the block made up of the two reversible gates such as HNG gate and PG gate.

HNG gate is a 4×4 gate It is used for designing ripple carry adders. It can give both sum and carry in a single gate thus minimizing the garbage and gate counts. The logic circuit of this gate is shown in section 3. Peres gate(PG) is a 3x3 gate. It is used to realize various Boolean functions such as AND, XOR. The logic circuit of this gate is also shown in section 3. Due to the use of reversible gates in multiplier minimum number of gates are utilize in the system. It should require minimum quantum cost and reversible gate does not allows Fan-out.

5. Simulation Results and Design Analysis

After the sytem design, the code is verified using a simulation software i.e. Xilinx ISE Simulator 13.2 for different inputs to generate outputs .The simulation is done by the behavioral simulation. The code is synthesized using Spartan 3 FPGA. The different inputs are given using the VHDL test bench. The RTL schematic and simulation results are shown below:

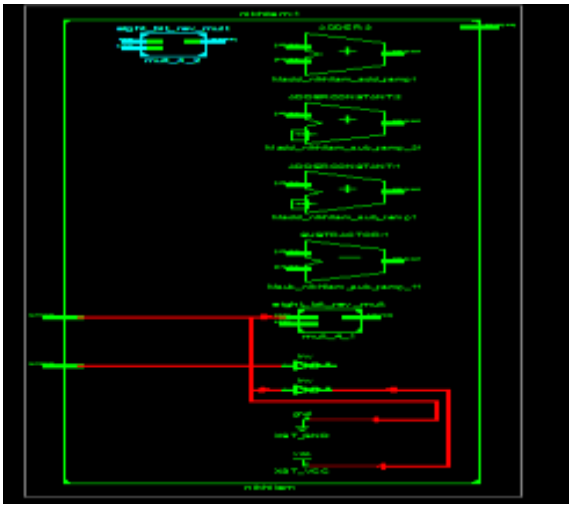

Figure 8: RTL Schematic

Design analysis contains the report of delay and device utilization summary.

Table 4: Timing Summary

Speed Grade	-4
Combinational Path Delay	8.73ns

Table 5: Device Utilization Summary

	Used	Available	Utilization
Number of Slices	193	4896	3%
Number of 4 input LUTs	204	4896	4%
Number of bonded IOBs	32	66	48%

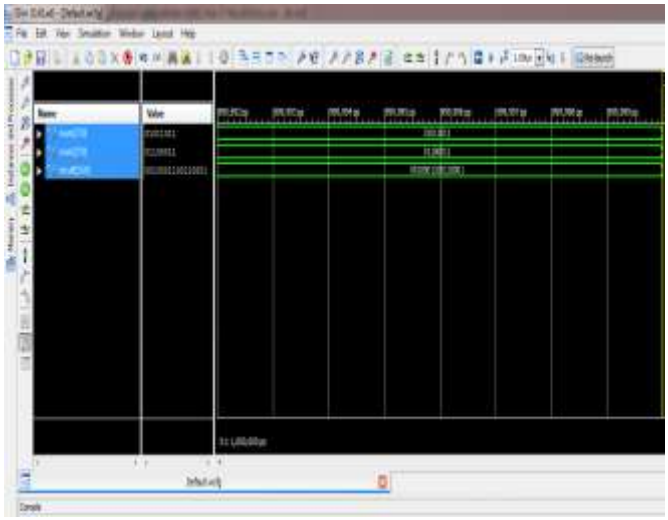

Figure 9: Simulation Waveform for 8×8 multiplication

6. Conclusion

The objective of developing the vedic multiplier is to increase the speed of the operation and reduce the propagation delay and power consumption. From the vedic formulae Nikhilam formula, is used for the multiplication of large numbers. In proposed system the multiplier is implemented by using the reversible logic gates to minimize the utilization of logic gates and reduce the power consumption. Nikhilam multiplier is implemented and simulated in Xilinx 13.2 ISE simulator. The simulation waveform and delay results are given in the paper. In future this system can be implement for the ALU as well as for designing of FFT to reduce the number of logic gates and delay of the system.

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