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Design & Simulation of Turbo Decoder for BER Calculation

Wazir

Assistant Professor, ECE Department, PMCE, Kami, Sonipat

Abstract

Turbo decoders applied in wireless communications are complex and dissipate large amount of power. In this paper, we investigate design & simulation of Turbo algorithm for wireless communications applications, including our proposed Simulink model of Turbo decoder. The schemes employed in our low-power design are clock-gating and toggle filtering. We described the behavior of Turbo decoders in Matlab Simulink Model and synthesized using a Simulink Communication tool. The analyzing circuits were replaced and routed in the standard cell design environment. BER estimation obtained through different simulations indicates that the proposed design reduces the BER of an original Turbo decoder design by 55%.

Key Words: - BER, BMU, Turbo algorithm, Simulink Model.

Introduction

The channel codings are a mostly used in communications systems due to the improvements that they can contribute to the system, such as better performance of Bit Error Rate (BER), power reduction, even increase the transmission rate while maintaining the same link quality. In addition, this type of technique is a significant improvement without involving high costs of specialized hardware, is acceptable to all types of communication schemes because of its various properties and corrective capabilities, so that for each channel there is one or several options available [1] . One kind of channel coding that is still in use, although it has been long time since its appearance, are convolutional codes[2].Since this kind of codes are in use, many variants and adaptations have been made in order to get better performance in certain applications. This has created the need to optimize the time of their development, so some convolutional codes generators for various platforms have been discussed [3, 4].In this paper , we test a model in Matlab that uses the vectors that describe the adders of a convolutional code; this can be generated using a set of basic blocks implemented as VHDL entities. These blocks are used to create Add-Compare-Select (ACS) cells that will be interconnected to create that decoder. The complexity of the decoders created is also described. Turbo decoders are widely used for forward error correction in many communication and multimedia devices such as modem, cellular phones, digital audio and video broadcasting (DAB and DVB) systems. For wireless communications, transmission channels are prone to various impediments such as fading, interference etc. Channel coding is indispensable in wireless communication for error free data transmission and reception. Many communication standards such as Wi-Fi IEEE802.11, Wi-Max IEEE 802.16e/m, specify Turbo Decoding as mandatory error correction code. Most of the satellite communication systems use Convolutional Code (CC) as the channel coding technique and Turbo Decoders as the decoder. Turbo decoders are also used in modems of ADSL and VDSL systems .

The state-of-the-art mobile devices provide more than one functionalities in a single device. Among the most popular functionalities, access to multiple radio environments, or alternate access to different wireless standards using a single device is a growing trend. Current mobile equipment show that there is a growing need to build such systems that can operate across multiple standards. Different standards specify different coding and decoding parameters within a same coding scheme.

Conventionally, realization of flexible Turbo Decoding is done by use of software or DSP implementations. However, a hardware solution is significantly more cost effective and capable of producing higher decoding throughput than

software or conventional DSP based implementations. Since hardware implementation is always efficient in terms of speed, power and throughput, in comparison to its counterpart software based implementations, a dynamically reconfigurable Turbo Decoder is an ideal candidate in the context of future multitier networks, software defined radios (SDR) or cognitive radio applications.

The rest of the paper is organized as follows. Section II outlines the complete design of Turbo Decoder. Proposed Algorithm to analyzed BER is discussed in Section III. Section IV is concentrated on the simulated result of Turbo Decoder. The conclusions are given in Section V.

Earlier Research Work

Amrata J. Mandwale (2015) presented different implementation of Turbo decoder with their performance analysis. Power dissipation is less & area of power dissipation is also less covered. Ashish Kumar Pradhan et.al (2014) used variable code rate along a particular constraints length & arbitrary truncation length. Gate Diffusion Input circuits for asynchronous design and compared the designs with CMOS asynchronous design. Luis Alberto (2013) discussed the implementation of a Turbo decoder based on ACS cell which are created with VHDL Code [3]. Mohender Veshala proposed a scheme based on Verilog language for the implementation of high-speed and low power consumption bi-directional Turbo decoder. It uses Modified Turbo Algorithm (MVA) [4].

Abukeker (2013) presented a low power design for Turbo decoder based on modifying decoding process offering 30-35% better than Viterbi. Anuradha et al (2013) presented a low-power trace-back (TB) scheme for high constraint length Turbo decoder.

D. Chakroborty et al (2013) discussed a high speed Turbo decoder which was based on pipelining mechanism and it operate at 64.516 MHz frequency. K. Cholan (2012) presented an efficient implementation method for parallel/pipeline processing Turbo decoders. It operates on FPGA based on EDA tool.

Turbo Decoder Design

The Turbo decoder design is a straightforward implementation of the basic processes of the Turbo algorithm. The block diagram design consists of three functional units, as shown in

Fig 1.

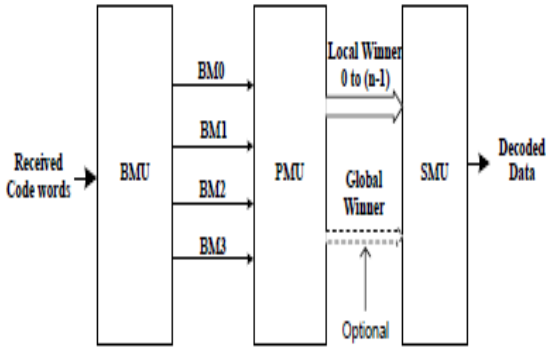

Fig.1 Classical three functional block of a rate 1/2 Turbo decoder design

BMU: Branch Metric (BM) is a measure of likelihood of transmission given noisy observation. BMs are computed as the normalised distances between every possible symbols in the code and the received symbols.

PMU: Branch metrics are accumulated along a path of trellis diagram to form a path metric. A path metric unit accumulates branch metrics to get the metric for all the paths, and selects the smallest among the PMs called the survivor PM.

The process is repeated for all the states in a single time step in the trellis. PMU computes PMs and updates the survivor PMs for all the states in survivor memory unit or SMU. The process usually repeats for 5*(K-l) times, where K denotes the constraint length of the encoder.

SMU: Once the trace back depth is reached, i.e 5*(K- 1), trace back operation begins. Trace back unit restores a maximum-likelihood path from the decision made by PMU.

The path with smallest path metrics is chosen while tracing backward in time. A unique path is identified. While tracing back through the trellis, the decoded output bits, corresponding to the traced branch, is generated in a reversed order.

Turbo Algorithm

Based on the indication of a zero Hamming distance path, a new adaptive Turbo algorithm and decoder can be proposed. The adaptive algorithm

stops the Turbo decoding process when a zero Hamming distance path occurs and is as follow:

1. Pre-decode and re-encode the received code words R_t;
2. Compare the re-encoded code word R'_t with the corresponding received code words R_t; if they match, set flag f(t) to '1', otherwise set f(t) to '0';
3. In the case of f(t) = 1, $count_{wards} = count_{wards} + 1$, otherwise $count_{wards} = 0$;
4. If the $count_{wards}$ = 5*L_c, where L_c is the constraint length of the code, set flag Z Path (t-5*L_c) to '1', otherwise set it to '0';
5. If Z Path (t-5*L_c) = 1 select the pre-decoded data $X'_{(t-5*L_c)}$ at time (t-5*L_c)as the decoded output, otherwise apply the Turbo decoding process on the code word $R_t - 5 * L_c$ and select the corresponding output from the Turbo decoder as the decoded data.
6. Repeat steps (1) to (5) to decode all $\{R_t\}$.

Simulink Model

The Turbo Simulink Model is designed below. The input signal is connected bipolar connector with proper gain. Random de interleaver is applied after passing internal decoder.

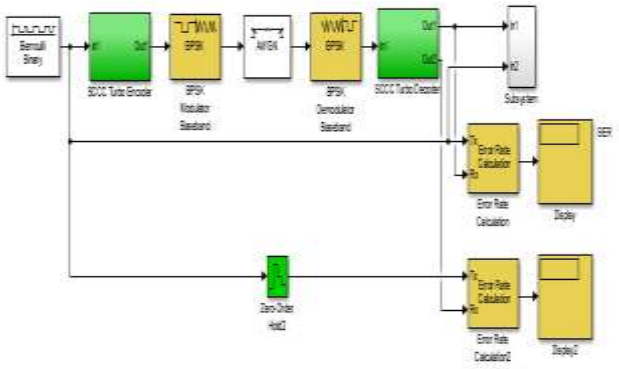

Fig.2 Simulink Internal Model of Turbo Decoder

Outer decoder is applied with zeros input signal. After getting zeros order signal, the proper output comes up from the different ports.

To calculate BER, Convolutional encoder and Turbo decoder is used with proper channel having white Gaussian noise. BPSK modulator & demodulator is applied to transmit and analyzed the signal.

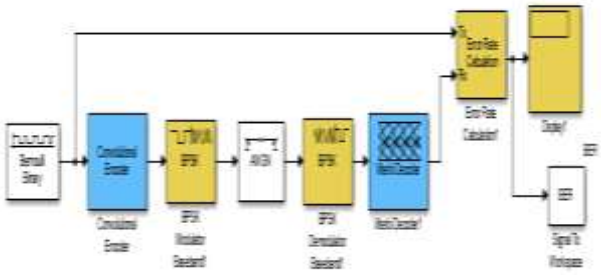

Fig.3 Simulink Model of Turbo Decoder

The signal is analyzed from the workspace and results come in form of Bit Error Rate. These results discussed in next section.

Simulation Result

In this section we introduce the theoretical & simulated decoding performance of various Turbo decoder implementations through a number of simulations performed using Simulink. Bit Error Rate is analyzed as shown in Fig 4.

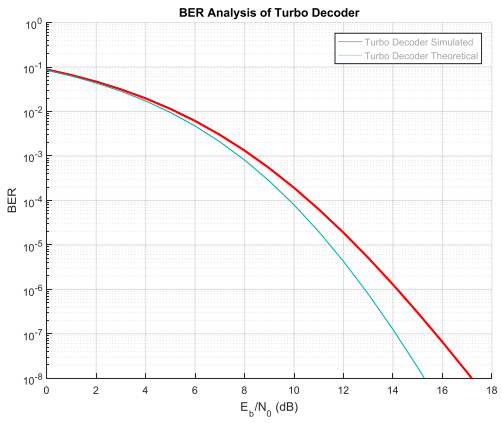

Fig 4 Comparison of Theoretical & Simulated BER.

Conclusion

This paper represents the research work of developing new approaches for implementing Turbo decoder designs to minimize computation complexity and bit error rate. This work examines the decoding process of the Turbo algorithm, the design of the Turbo decoder, and simulated the result. This enables the design problems to be discovered. Then a new algorithm is proposed to the decrease bit error rate. Then simulated result is better than theoretical result.

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